LC1046A Digital Signaling Interface

Features

- Fully-integrated DS1/DS1C line interface
- Complies with *Compatibility Bulletin 119* (*CB119*) and *PUB 43802* specifications
- On-chip transmit equalization
- Monolithic clock recovery
- Pin-selectable B8ZS encoder and decoder
- Loopback modes for fault isolation
- Multiple link status and alarm features
- Minimal external circuitry required

Description

The LC1046A Digital Signaling Interface (DSI) is an integrated circuit that provides a line interface between the DS1 or DS1C cross-connect (DSX) and terminal equipment circuits for cable distances of up to 655 feet for 22-gauge plastic insulated cable (PIC). It performs receive pulse regeneration, timing recovery, and transmit pulse shaping and equalization functions. The LC1046A DSI device is manufactured using 1.75-micron CMOS technology and is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting. The digital circuitry is shown in Figure 1. The analog circuitry is shown in Figure 6.

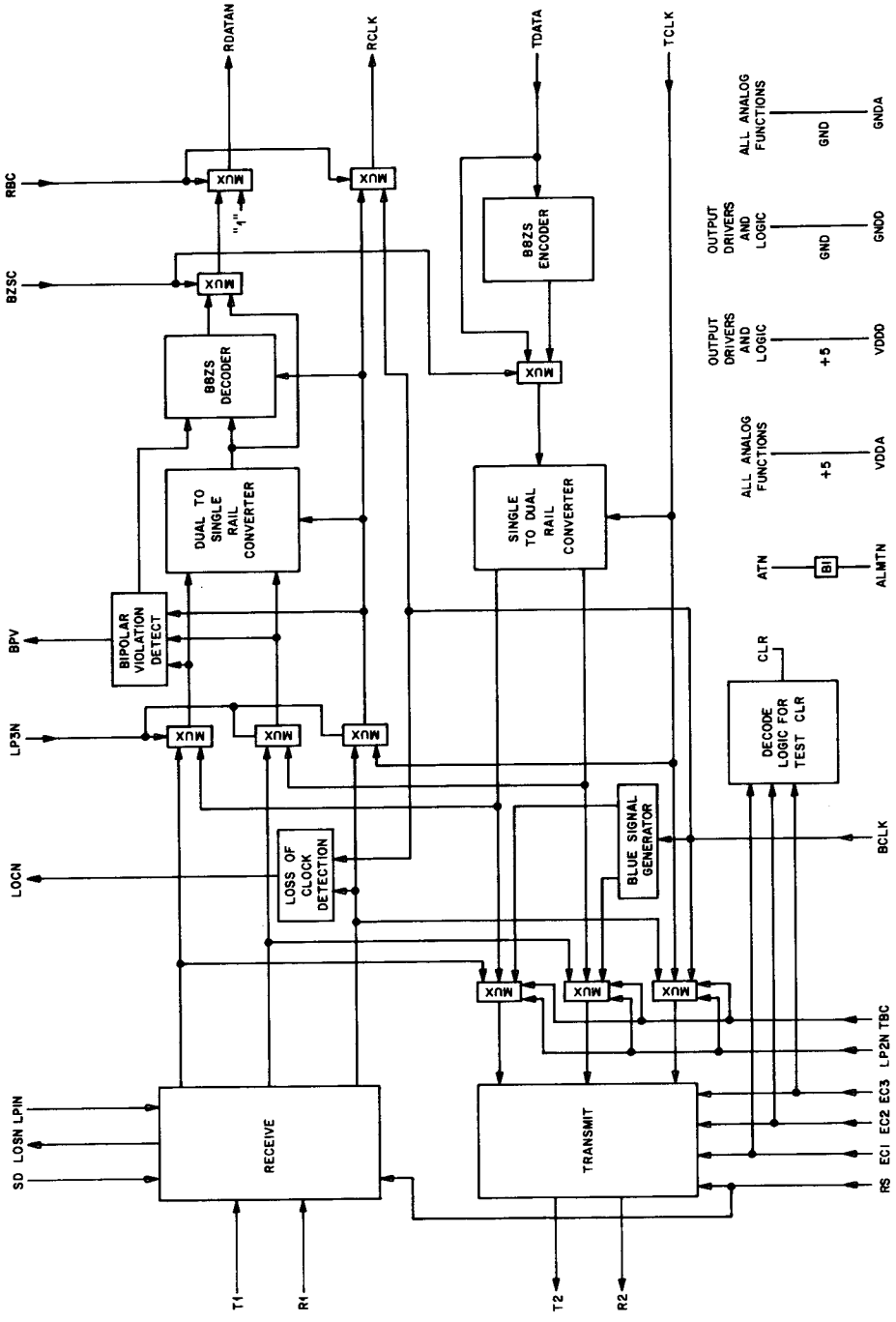


Figure 1. Block Diagram

User Information

Pin Descriptions

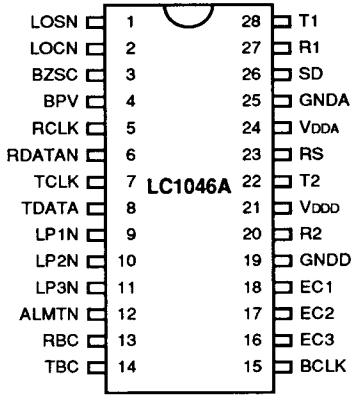


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	LOSN	O	**Loss-of-Signal Not.** This pin is cleared (0) upon loss of the data signal at the receiver inputs.
2	LOCN	O	**Loss-of-Clock Not.** This pin is cleared when SD = 1 and LOSN = 0, indicating that a loss of clock has occurred. When LOCN = 0, no transitions occur on RCLK and RDATAN outputs. A valid clock must be present at BCLK for this function to operate properly.
3	BZSC	I	**B8ZS Enable.** This pin is set (1) when inserting a B8ZS substitution code on the transmit side and when removing the substitution code on the receive side.
4	BPV	O	**Bipolar Violation.** This pin is set upon detection of a bipolar violation on the receive-side input after removal of the legal B8ZS substitution code.
5	RCLK	O	**Receive Clock.** Output receive clock signal to the terminal equipment.
6	RDATAN	O	**Receive Data Not.** 1.544-Mb/s inverted unipolar output data (DS1) or 3.152-Mb/s data (DS1C). This data has a 100% duty cycle.
7	TCLK	I	**Transmit Clock.** DS1 input clock signal (1.544 MHz ± 130 ppm) or DS1C input clock signal (3.152 MHz ± 30 ppm).
8	TDATA	I	**Transmit Data.** 1.544-Mb/s unipolar input data (DS1) or 3.152-Mb/s data (DS1C).

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
9	LP1N	I	**Loopback 1 Enable Not.** This pin is cleared for a full local loopback (transmit converter output to receive converter input). Most of the transmit and receive analog circuitry is exercised in this loopback.
10	LP2N	I	**Loopback 2 Enable Not.** This pin is cleared for a remote loopback (DSX to DSX). In loopback 2, a high on TBC (pin 14) inserts the blue signal on the transmit side.
11	LP3N	I	**Loopback 3 Enable Not.** This pin is cleared for a digital local loopback. Only the transmit and receive digital sections are exercised in this loopback.
12	ALMTN	I	**Alarm Test Enable Not.** This pin is cleared, forcing LOSN = 0, LOCN = 0, and BPV = 1 for testing without affecting data transmission.
13	RBC	I	**Receive Blue Control.** This pin is set to insert the blue signal on the receive side.
14	TBC	I	**Transmit Blue Control.** This pin is set to insert the blue signal on the transmit side. This control has priority over a loopback 2 if both are operated.
15	BCLK	I	**Blue Clock.** DS1 blue clock signal (1.544 MHz ± 130 ppm) or DS1C blue clock signal (3.152 MHz ± 30 ppm) input. This clock is independent of the transmit clock.
16	EC3	I	**Equalizer Control 3.*** One of three control leads for selecting transmit equalizers.
17	EC2	I	**Equalizer Control 2.*** One of three control leads for selecting transmit equalizers.
18	EC1	I	**Equalizer Control 1.*** One of three control leads for selecting transmit equalizers.
19	GNDD	—	**Digital Ground.**
20	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit output.
21	V_{DDD}	—	**5 V Digital Supply (± 10%).**
22	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit output.
23	RS	I	**Rate Select.** This pin is cleared for DS1 operation and set for DS1C operation.
24	V_{DDA}	—	**5 V Analog Supply (± 10%).**
25	GNDA	—	**Analog Ground.**
26	SD	I	**Shutdown Enable.** This pin is set, forcing RCLK and RDATAN high and LOCN low if a loss of signal is detected (LOSN = 0).
27	R1	I	**Receive Bipolar Ring.** Negative bipolar receive input.
28	T1	I	**Receive Bipolar Tip.** Positive bipolar receive input.

* See Table 2.

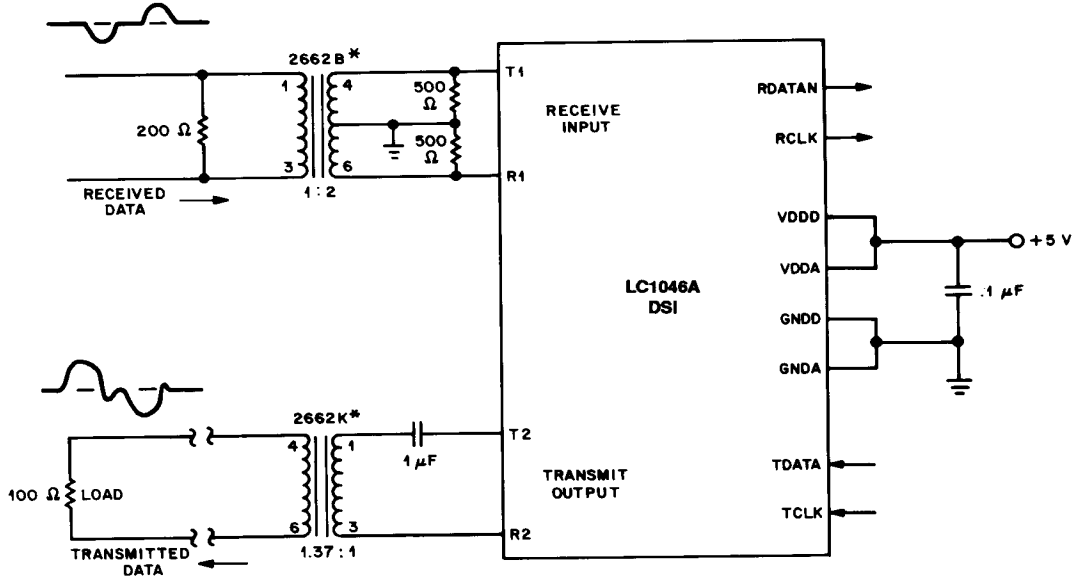
Table 2. Equalizer Control*

Distance to DSX (Ft.)** (Applies only to 22-Ga. PIC (ABAM) Cable)	Maximum Cable Loss (dB at 772 kHz)	EC1	EC2	EC3
0—133	.6	0	0	0
133—267	1.2	0	0	1
267—400	1.8	0	1	0
400—533	2.4	0	1	1
533—655	3	1	0	0
Test clear	—	1	0	1

* Other bit combinations represent test modes – not to be used for normal operation.
** Use maximum loss figures for other cable types.

Overview

The LC1046A is a fully-integrated digital signaling interface (DSI) that requires only two line interface transformers, three input termination resistors, and one capacitor to provide a bidirectional line interface between a DS1 or DS1C cross-connect (DSX) and terminal equipment. A typical application diagram is shown in Figure 3. This device is specified for use with 22-gauge plastic insulated ABAM cable, as well as other cable types. The circuit is divided into three main blocks: transmit converter, receive converter, and logic. The transmit and receive converters process information signals through the device in the transmit and receive directions, respectively; the logic is the control and status interface for the device.



* A step-up transformer is used.

Figure 3. Typical Application Diagram for Bipolar Signal Interfacing

Transmit Converter

The line interface transmission format is return-to-zero, bipolar alternate mark inversion (AMI), requiring transmission and sensing of alternately positive and negative pulses. The transmit converter accepts unipolar data and clock, and converts the signal to a balanced bipolar data signal. Binary 1s in the data stream become pulses of alternating polarity transmitted between the two output rails, T2 and R2. Binary 0s are transmitted as null pulses. All necessary transmit pulse shaping is done on-chip, eliminating the need for external shaping networks. This is done by shaping the pulses at the bipolar output (T2, R2) according to the selected equalizer control (EC1—EC3) inputs (see Table 2).

The output pulse waveform consists of four distinct levels: overshoot, pulse, backswing, and tail. They are produced by a high-speed D/A converter and are driven onto the line by using low-impedance output buffers. There are five different pulse shapes, corresponding to 133-foot increments of cable, that are obtained by setting the appropriate equalizer control inputs. The entire transmit analog path is fully differential, which guarantees symmetrical positive and negative pulses. The resulting pulses meet the amplitude, rise and fall time, overshoot, undershoot, template, and power requirements for the office DSX cross-connect as given in *Compatibility Bulletin 119*. A typical DS1 output waveform at the DSX relative to the *CB119* template is shown in Figure 4, and a typical output waveform at the transformer secondary is shown in Figure 5. The analog circuitry is shown in Figure 6.

The clock multiplier uses a phase-lock loop to produce the high-speed timing waveforms needed by the D/A converter. The clock multiplier also eliminates the need for the tightly controlled transmit clock duty cycle usually required in discrete implementations. Transmitter specifications are given in Table 3.

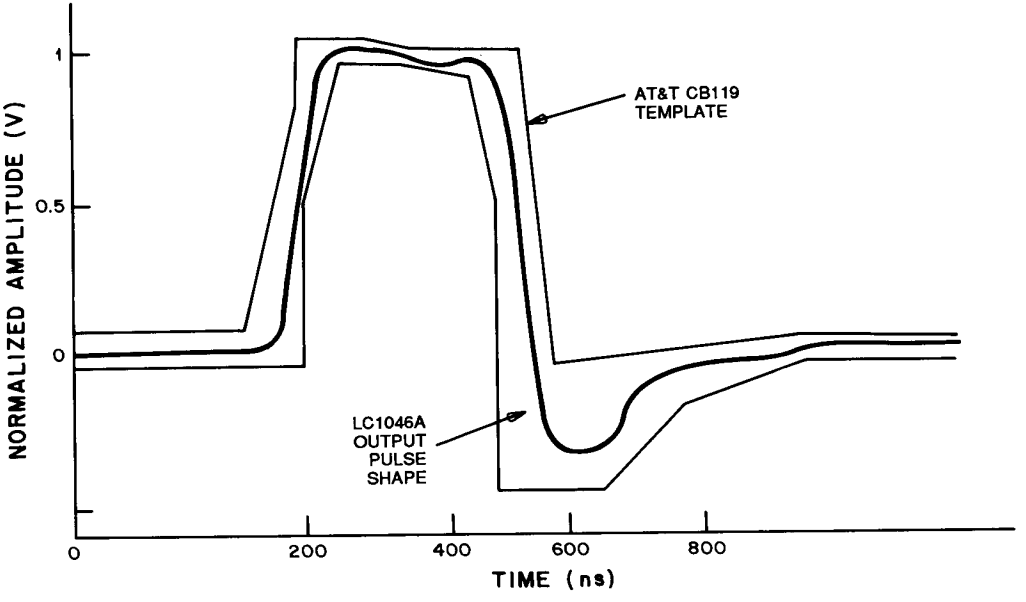
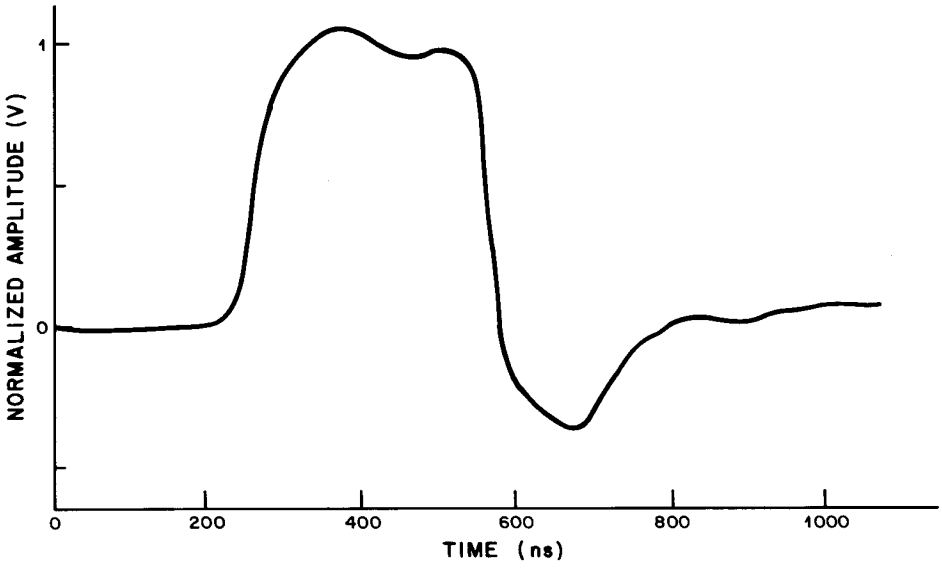


Figure 4. Typical DS1 Output Waveform at DSX



Note: EC1 = 0, EC2 = 1, EC3 = 0.

Figure 5. Typical DS1 Output Waveform at Transformer Secondary

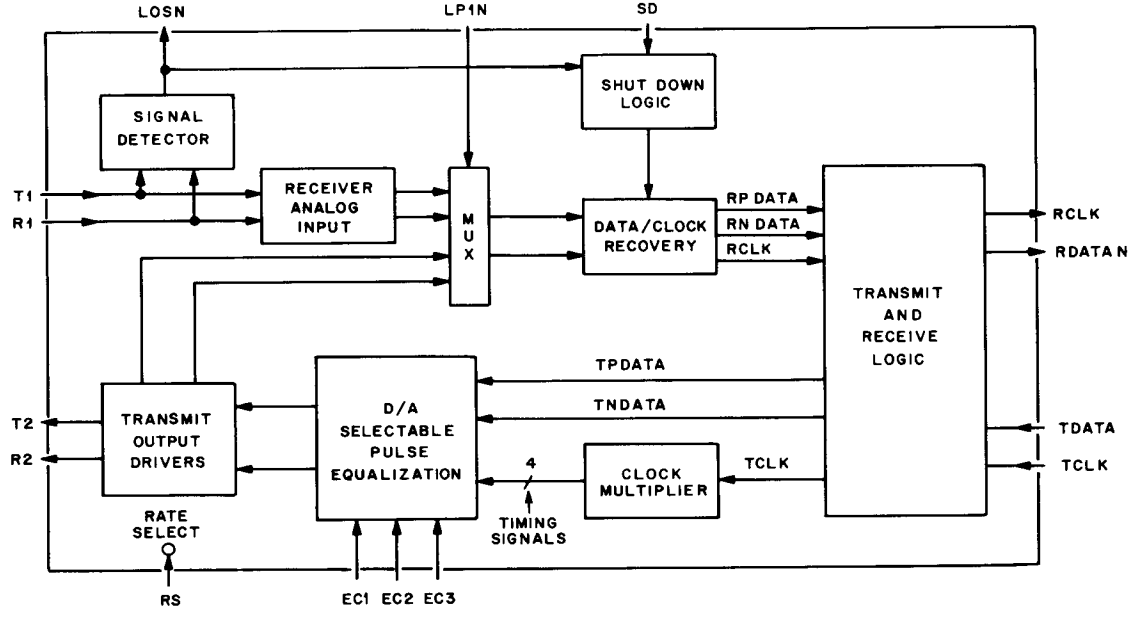


Figure 6. Analog Block Diagram

Table 3. Transmitter Specifications

Parameter	Min	Typ	Max	Unit
Output pulse amplitude (at the DSX):				
DS1	2.4	3.0	3.6	V
DS1C	2.3	3.0	3.7	V
Pulse width (50%):				
DS1	330	350	370	ns
DS1C	139	159	179	ns
Output power levels:				
DS1				
2-kHz band at 772 kHz	12.6	16.5	18.5	dBm
2-kHz band at 1544 kHz	−29	−39	—	dB*
DS1C				
10-kHz band at 1576 kHz	14.5	16.5	18.5	dBm
10-kHz band at 3152 kHz	−29	−39	—	dB**
Positive/negative pulse imbalance	—	—	0.5	dB
Rise/fall time (20%—80%), DS1C	—	—	50	ns
Overshoot, DS1C	—	—	10	%†
Zero level, DS1C	—	—	10	%†
Rise/fall time imbalance, DS1C	—	—	20	ns
Output termination	95	100	105	Ω
Output transformer turns ratio (2662K type)	1:1.30	1:1.37	1:1.44	—

* Below the power at 772 kHz.
** Below the power at 1576 kHz.
† Percentage of the pulse amplitude.

Receive Converter

The receive converter accepts bipolar input signals (T1, R1), coupled through a receive transformer, from the cross-connect over a maximum of 655 feet of 22-gauge PIC (ABAM) cable. The received signal is rectified while the amplitude and rise time are restored. These input signals are peak-detected and sliced by the receiver front-end, producing the digital signals PDATA and NDATA (Figure 6). The timing is extracted by means of phase-locked loop (PLL) circuitry that locks an internal, free-running, current-controlled oscillator (ICO) to the 1.544-MHz (DS1 signal) or 3.152-MHz (DS1C signal) component.

The PLL employs a 3-state phase detector and a low-voltage/temperature coefficient, current-controlled oscillator (ICO). The ICO free-running frequency is trimmed to within ± 2.5% of the data rate at wafer probe, with V_{DD} = 5.0 V and T_A = 25 °C. For all operating conditions (see the Operating Conditions section), the free-running oscillator frequency deviates from the data rate by less than ± 7%, alleviating the problem of harmonic lock.

Due to the clock output of the receive converter being derived from the ICO, a free-running clock can be present at the output of the receive converter without data being present at the input. A shutdown pin (SD) is provided to block this clock if desired, eliminating the free-running clock upon loss of the input signal. Table 4 is a truth table showing the shutdown operation under various conditions.

The PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. Low jitter sensitivity to power supply noise allows compact line card layouts employing many DSIs on one board. The minimum input jitter tolerance, as specified in AT&T *Publication 43802* (*PUB 43802*), and the measured DSI jitter tolerance are shown for both the DS1 and DS1C rates in Figures 7 and 8, respectively. Receiver specifications are shown in Table 5.

Table 4. Shutdown Operation Truth Table

Inputs				Outputs		
LP1N	SD	Input Signal	Loopback Signal*	LOSN	LOCN	Receive Side
1	0	Normal	x	1	1	Normal
1	0	No signal	x	0	1	Free-running VCO
1	1	Normal	x	1	1	Normal
1	1	No signal	x	0	0	No output
0	0	Normal	Normal	1	1	Normal loopback
0	0	Normal	No signal	1	1	Free-running VCO
0	0	No signal	Normal	0	1	Normal loopback
0	0	No signal	No signal	0	1	Free-running VCO
0	1	Normal	Normal	1	1	Normal loopback
0	1	Normal	No signal	1	1	Free-running VCO
0	1	No signal	Normal	0	0	No output
0	1	No signal	No signal	0	0	No output

* x = don't care.

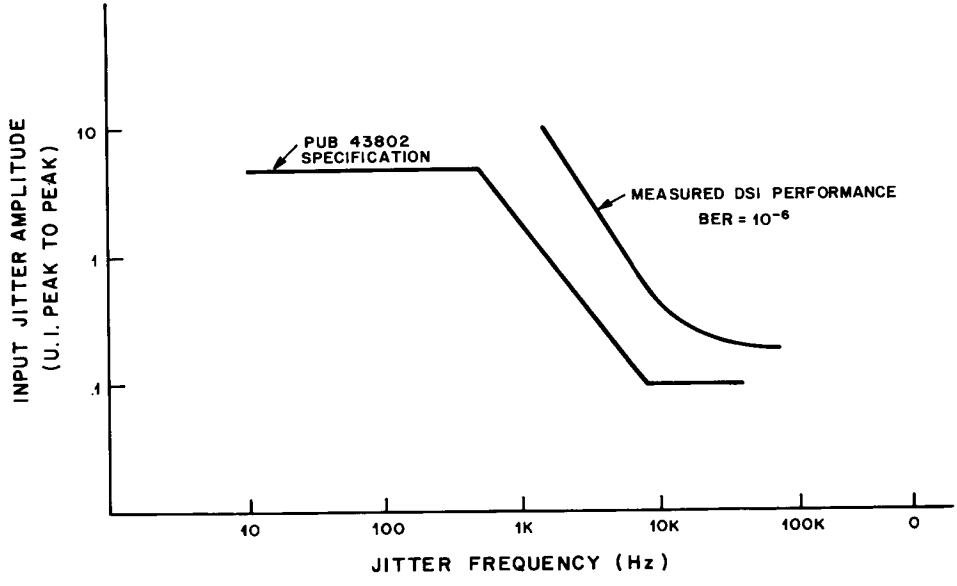


Figure 7. DS1 Jitter Tolerance

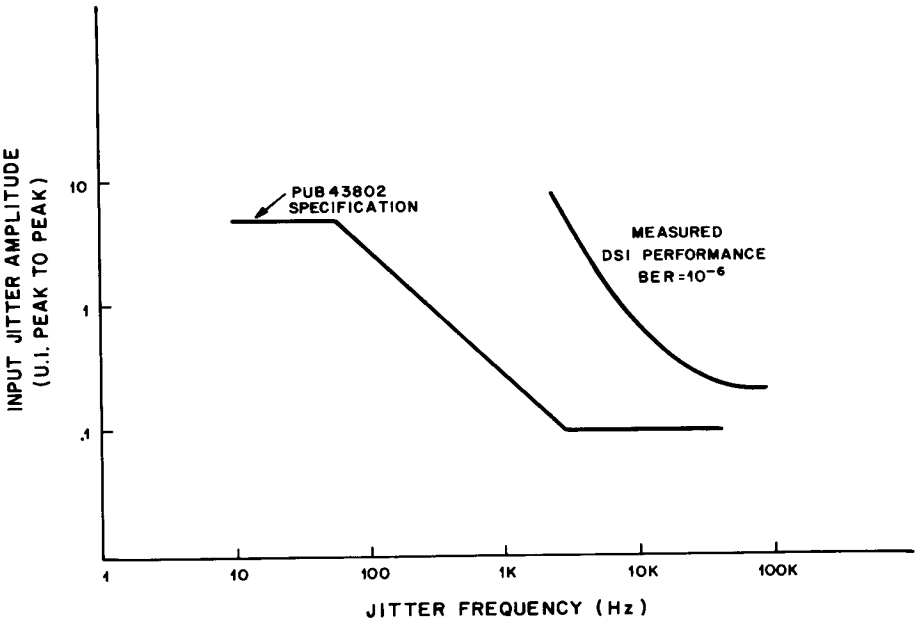


Figure 8. DS1C Jitter Tolerance

Table 5. Receiver Specifications

Parameter	Min	Typ	Max	Unit
Receiver sensitivity (at input of device)	1.0	—	—	Vp
PLL jitter:*				
DS1				
3dB bandwidth	—	20	—	kHz
peaking	—	1.4	—	dB
DS1C				
3dB bandwidth	—	18	—	kHz
peaking	—	1.4	—	dB
V_{DD} noise (BER = 10^{-9})**	—	0.8	—	Vpp
Input density (1s)†	12.5	—	—	%
ICO free-running frequency error	—	—	± 7	%
Input transformer turns ratio (2662B type)	1:1.9	1:2.0	1:2.1	—
Input termination	—	100	—	Ω

* Transfer characteristics (1/8 input).
** The point of maximum sensitivity is a sine wave at 11 kHz (pseudorandom data).
† The maximum number of consecutive 0s = 15.

Digital Logic

The logic provides alarms, optional B8ZS coding, blue signal insertion circuits, and maintenance loopbacks. It also performs dual-rail to single-rail conversion of the data.

Alarms. A loss-of-signal alarm occurs when the input signal amplitude is below the threshold needed for clock recovery. A loss-of-signal indicator in the receive front-end detects the loss of sufficient amplitude at R1 and T1. The LOSN alarm is triggered if the input data is approximately 0.5 V in amplitude. Hysteresis (250mV) is provided to prevent LOSN chattering.

An independent loss-of-clock output (LOCN) is also provided so that loss-of-clock is detected when the shutdown option is in effect. LOSN and LOCN can be wire-ORed to produce a single alarm.

A bipolar violation output is included, giving an alarm each time a violation (two or more successive 1s on a rail) occurs. The violation alarm output is held in a latch for one cycle of the internal clock (RCLK). In the B8ZS mode, bipolar violations within the legal substitution code are not detected and, therefore, do not produce an alarm.

An alarm test pin (ALMTN) is provided to test the alarm outputs, LOSN, LOCN, and BPV. Clearing this pin forces the alarm outputs to the alarm state without affecting data transmission.

B8ZS Option. The LC1046A DSI contains a B8ZS encoder and decoder that can be selected by setting the BZSC pin. This allows the encoder to substitute a zero-substitution code for eight consecutive 0s detected in the data stream, as illustrated in Table 6. A "V" represents a violation of bipolar code and a "B" represents a bipolar pulse of correct polarity. The decoder detects the zero-substitution code and reinserts eight 0s in the data stream.

Table 6. B8ZS Substitution Code

Before B8ZS	00000000
After B8ZS	000VB0VB

Blue Signal Generators. There are two blue signal generators in this device. One substitutes an all-1s blue signal on the RDATAN output toward the terminal equipment. The other substitutes a bipolar all-1s blue signal for the bipolar data out of the transmit converter to keep line repeaters active.

Loopback Paths. The DSI has three independent loopback paths, which are activated by clearing the respective control inputs, LP1N, LP2N, or LP3N. Loopback 1 bridges the data stream from the transmit converter (transmit converter included) to the input of the receive converter. This maintenance loop includes most of the internal circuitry.

Loopback 2 provides a loopback of data and recovered clock from the bipolar inputs (T1, R1) to the bipolar outputs of the transmit converter (T2, R2). The receive front-end, receive PLL, and transmit driver circuitry are all exercised. This loop can be used to isolate failures between systems.

Loopback 3 loops the data stream as in loopback 1 but bypasses the transmit and receive converters. The blue signal can be transmitted towards the DSX when in this loopback. Loopbacks 2 and 3 can be operated simultaneously to provide transmission loops in both directions.

Characteristics

Logic Interface Electrical Characteristics

T_A = −40 to +85 °C; V_{DD} = 5 V ± 10%

Parameter	Symbol	Min	Max	Unit
Input voltage:				
low	V_{IL}	GNDD	0.8	V
high	V_{IH}	2.0	V_{DDD}	V
Output voltage:				
low	V_{OL}	GNDD	0.4	V
high	V_{OH}	2.4	V_{DDD}	V
Input capacitance	C_I	—	20	pF
Load capacitance	C_L	—	40	pF
Source current	Isource	—	80	μA
Sink current	Isink	—	2.0	mA

Internal pull-up resistors are provided on the following input leads: LP1N, LP2N, LP3N, and ALMTN. Internal pull-down devices are provided on the following leads: SD, RBC, BZSC, TBC, RS, EC1, EC2, and EC3. The internal pull-up or pull-down devices require the input to source or sink to be no more than 20 μA.

Operating Conditions

−40 °C ≤ T_A ≤ +85 °C, except as noted

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Power dissipation*	PD	—	300	400	mW

* Measurement conditions with 50% 1s on the transmit side, T_A = 25 °C, and equalizer settings: EC1 = 0, EC2 = 1, EC3 = 0 (V_{DD} = 5 V).

Maximum Ratings

DC supply voltage (V_{DD}) range ..... −0.5 to +6.5 V
Power dissipation (PD) ..... 1 W
Storage temperature (Tstg) range ..... −65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Timing Characteristics

All duty cycle and timing relationships are referenced to a TTL 1.4 V threshold level.

Loss-of-Clock Indication Timing. The clock leaving must be absent 5.18 μs (DS1) or 2.54 μs (DS1C) to guarantee a loss-of-clock indication. However, it is possible to produce a loss-of-clock indication if the clock is absent for 2.59 μs (DS1) or 1.27 μs (DS1C), depending on the timing relationship of the interruption with respect to the timing cycle.

The clock returning must be present 5.18 μs (DS1) or 2.54 μs (DS1C) to guarantee a normal condition on the loss-of-clock pin (LOCN). However, the loss-of-clock indication can return to normal immediately, depending on the timing relationship of the signal return with respect to the timing cycle.

Symbol	Description	Min	Typ	Max	Unit
tTCLTCL	TCLK clock period	*	647.7**	*	ns
tTCHTCL	TCLK duty cycle	40	50	60	%
tTDVTCL	Data set-up time, TDATA to TCLCK	50	—	—	ns
tTCLTDV	Data hold time, TCLK to TDATA	40	—	—	ns
tr	Clock rise time	—	—	40†	ns
tf	Clock fall time	—	—	40†	ns
tRCHRDV	Data hold time, RCLK to RDATAN, BPV:				
	DS1	227	—	—	ns
	DS1C	111	—	—	ns
tRDVRCH	Data set-up time, RDATAN, BPV to RCLK:				
	DS1	187	—	—	ns
	DS1C	113	—	—	ns
tRCLRDV	Propagation delay, RCLK to RDATAN	—	—	40	ns

* A tolerance of ± 130 ppm.
** 317.3 at DS1C rate.
† 20 at DS1C rate.

Timing Diagrams

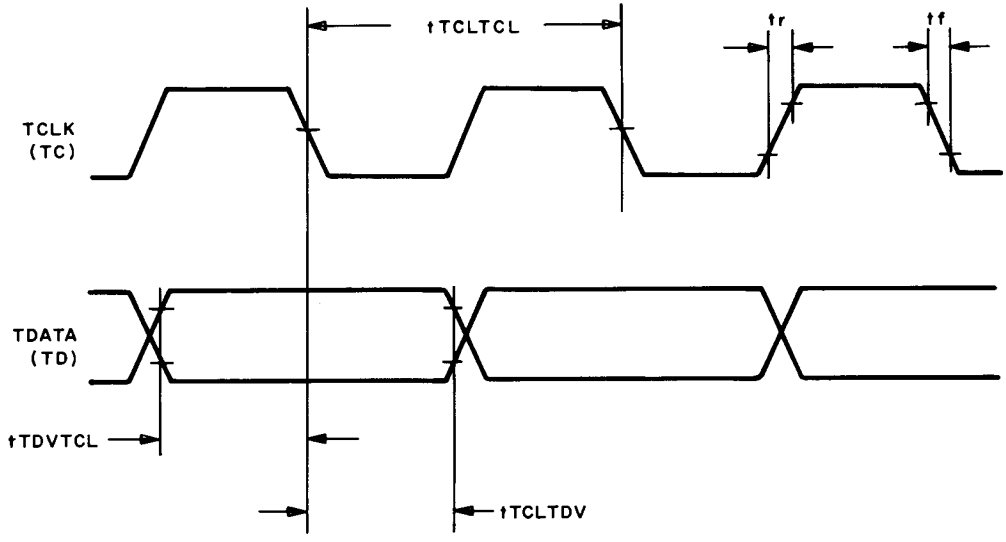


Figure 9a. Timing Diagram

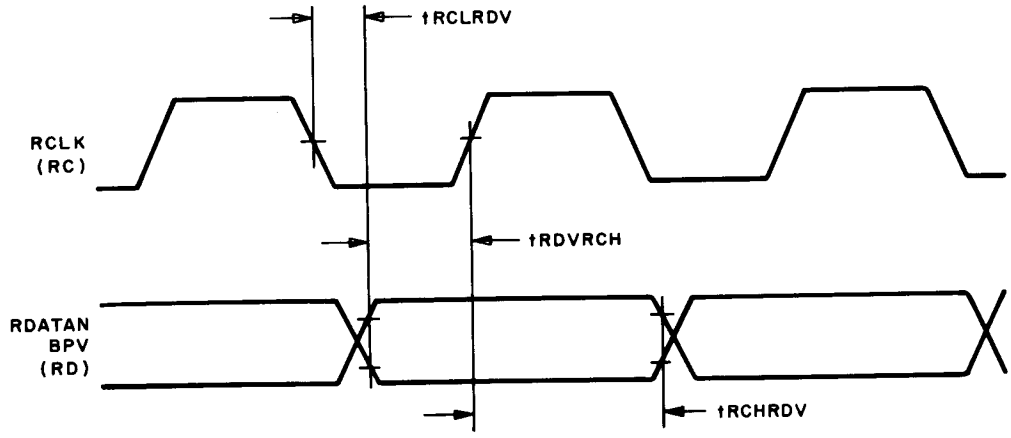


Figure 9b. Timing Diagram