

CYPRESS
SEMICONDUCTOR

CY7C132/CY7C136

CY7C142/CY7C146

2K x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C132/CY7C136 easily expands data bus width to 16 or more bits using slave CY7C142/CY7C146
- **BUSY** output flag on CY7C132/ CY7C136; **BUSY** input on CY7C142/CY7C146
- **INT** flag for port-to-port communication (52-pin LCC/PLCC versions)

Functional Description

The CY7C132/CY7C136/CY7C142/ CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided to permit independent access to any location in memory. The CY7C132/ CY7C136 can be utilized as either a stand-alone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

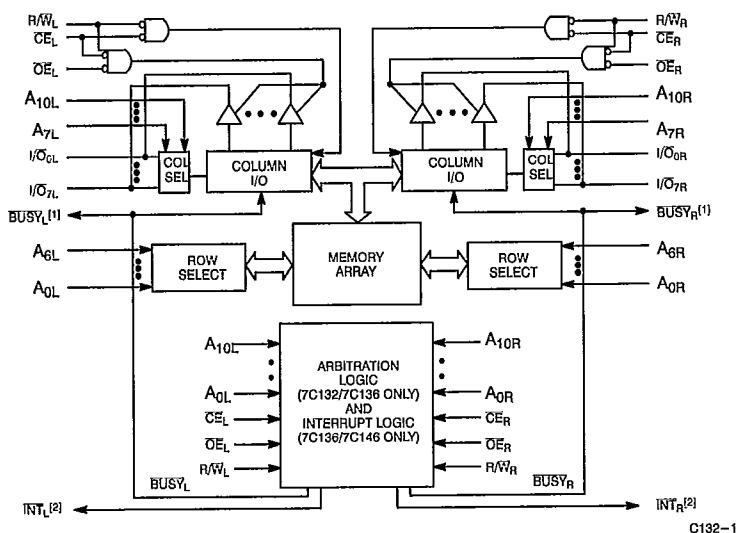
Each port has independent control pins; chip enable ($\overline{CE}$), write enable ($\overline{R/W}$), and

output enable ($\overline{OE}$). **BUSY** flags are provided on each port. In addition, an interrupt flag (**INT**) is provided on each port of the 52-pin LCC and PLCC versions. **BUSY** signals that the port is trying to access the same location currently being accessed by the other port. On the LCC/PLCC versions, **INT** is an interrupt flag indicating that data has been placed in a unique location (7FF for the left port and 7FE for the right port).

An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC.

Logic Block Diagram



Pin Configuration

DIP Top View			
$\overline{CE}_L$	1	48	V_{CC}
$\overline{R/W}_L$	2	47	$\overline{CE}_R$
$\overline{BUSY}_L$	3	46	$\overline{R/W}_R$
A_{10L}	4	45	$\overline{BUSY}_R$
$\overline{OE}_L$	5	44	A_{10R}
A_0L	6	43	$\overline{OE}_R$
A_{1L}	7	42	A_0R
A_{2L}	8	41	A_{1R}
A_{3L}	9	40	A_{2R}
A_{4L}	10	39	A_{3R}
A_{5L}	11	38	A_{4R}
A_{6L}	12	37	A_{5R}
A_{7L}	13	36	A_{6R}
A_{8L}	14	35	A_{7R}
A_{9L}	15	34	A_{8R}
I/O_{0L}	16	33	A_{9R}
I/O_{1L}	17	32	I/O_{7R}
I/O_{2L}	18	31	I/O_{6R}
I/O_{3L}	19	30	I/O_{5R}
I/O_{4L}	20	29	I/O_{4R}
I/O_{5L}	21	28	I/O_{3R}
I/O_{6L}	22	27	I/O_{2R}
I/O_{7L}	23	26	I/O_{1R}
GND	24	25	I/O_{0R}

Notes:

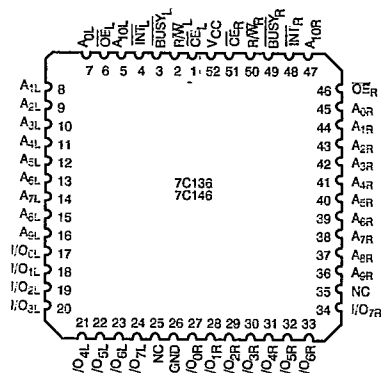
1. CY7C132/CY7C136 (Master): **BUSY** is open drain output and requires pull-up resistor.
2. CY7C142/CY7C146 (Slave): **BUSY** is input.
3. Open drain outputs; pull-up resistor required.



CY7C132/CY7C136
CY7C142/CY7C146

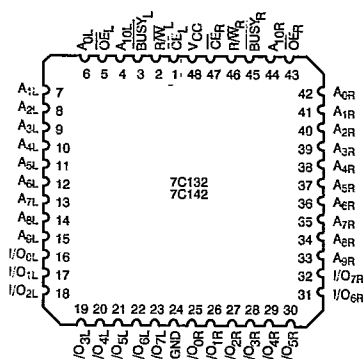
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C132-3

48-Pin LCC
Top View



C132-4

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SRAMS

Selection Guide

		7C132-25 ^[3] 7C136-25 7C142-25 7C146-25	7C132-30 7C136-30 7C142-30 7C146-30	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Com'l/Ind	170	170	120	90	90
	Military			170	120	120
Maximum Standby Current (mA)	Com'l/Ind	65	65	45	35	35
	Military			65	45	45

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with

Power Applied - 55°C to +125°C

Supply Voltage to Ground Potential

(Pin 48 to Pin 24) - 0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.5V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	- 40°C to +85°C	5V ± 10%
Military ^[4]	- 55°C to +125°C	5V ± 10%

Notes:

3. 25-ns version available in LCC and PLCC packages only.

4. T_A is the "instant on" case temperature

CYPRESS
SEMICONDUCTORCY7C132/CY7C136
CY7C142/CY7C146Electrical Characteristics Over the Operating Range^[5]

Parameter	Description	Test Conditions	7C132-25, 30 ^[3] 7C136-25,30 7C142-25,30 7C146-25,30		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45,55 7C136-45,55 7C142-45,55 7C146-45,55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	I _{OL} = 4.0 mA		0.4		0.4		0.4	V
		I _{OL} = 16.0 mA ^[6]		0.5		0.5		0.5	
V _{IH}	Input HIGH Voltage		2.2		2.2		2.2		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 5	+5	- 5	+5	- 5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 5	+5	- 5	+5	- 5	+5	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	CE = V _{IL} , Outputs Open, f = f _{MAX} ^[8]	Com'l	170		120		90	mA
			Mil			170		120	
I _{SB1}	Standby Current Both Ports, TTL Inputs	CE _L and CE _R ≥ V _{IH} , f = f _{MAX} ^[8]	Com'l	65		45		35	mA
			Mil			65		45	
I _{SB2}	Standby Current One Port, TTL Inputs	CE _L or CE _R ≥ V _{IH} , Active Port Outputs Open, f = f _{MAX} ^[8]	Com'l	115		90		75	mA
			Mil			115		90	
I _{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports CE _L and CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0	Com'l	15		15		15	mA
			Mil			15		15	
I _{SB4}	Standby Current One Port, CMOS Inputs	One Port CE _L or CE _R ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, Active Port Outputs Open, f = f _{MAX} ^[8]	Com'l	105		85		70	mA
			Mil			105		85	

Capacitance^[9]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	15	pF
C _{OUT}	Output Capacitance		10	pF

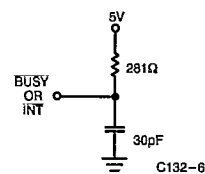
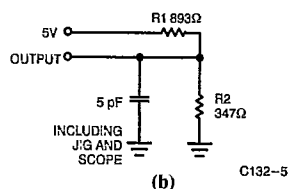
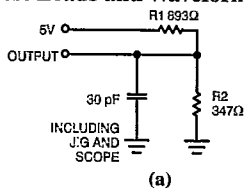
Notes:

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- Duration of the short circuit should not exceed 30 seconds.
- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{rc} and using AC Test Waveforms input levels of GND to 3V.
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
- AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
- At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
- t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



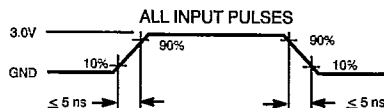
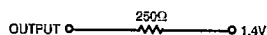
CY7C132/CY7C136
CY7C142/CY7C146

AC Test Loads and Waveforms



BUSY Output Load
(CY7C132/CY7C136 ONLY)

Equivalent to: THÉVENIN EQUIVALENT



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SRAMS

Switching Characteristics Over the Operating Range^[5,10]

Parameter	Description	7C132-25 ^[3]		7C132-30		7C132-35		7C132-45		7C132-55		Unit
		7C136-25	7C136-30	7C136-35	7C136-45	7C136-55						
		7C142-25	7C142-30	7C142-35	7C142-45	7C142-55						
		7C146-25	7C146-30	7C146-35	7C146-45	7C146-55						
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	25		30		35		45		55		ns
t _{AA}	Address to Data Valid ^[11]		25		30		35		45		55	ns
t _{OHA}	Data Hold from Address Change	0		0		0		0		0		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid ^[11]		25		30		35		45		55	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid ^[11]		15		20		20		25		25	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[12]	3		3		3		3		3		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[12]	5		5		5		5		5		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[12, 13]		15		15		20		20		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		25		25		35		35		35	ns
WRITE CYCLE ^[14]												
t _{WC}	Write Cycle Time	25		30		35		45		55		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	20		25		30		35		40		ns
t _{AW}	Address Set-Up to Write End	20		25		30		35		40		ns
t _{HA}	Address Hold from Write End	2		2		2		2		2		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	R/W Pulse Width	15		25		25		30		30		ns
t _{SD}	Data Set-Up to Write End	15		15		15		20		20		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	R/W LOW to High Z		15		15		20		20		25	ns
t _{LZWE}	R/W HIGH to Low Z	0		0		0		0		0		ns


Switching Characteristics Over the Operating Range^[5,10] (continued)

Parameter	Description	7C132-25 ^[3]		7C132-30		7C132-35		7C132-45		7C132-55		Unit
		7C136-25	7C136-30	7C136-35	7C136-45	7C136-55	7C142-25	7C142-30	7C142-35	7C142-45	7C142-55	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING												
t _{BLA}	BUSY LOW from Address Match		20		20		20		25		30	ns
t _{BHA}	BUSY HIGH from Address Mismatch ^[15]		20		20		20		25		30	ns
t _{BLC}	BUSY LOW from $\overline{CE}$ LOW		20		20		20		25		30	ns
t _{BHC}	BUSY HIGH from $\overline{CE}$ HIGH ^[15]		20		20		20		25		30	ns
t _{PS}	Port Set Up for Priority	5		5		5		5		5		ns
t _{WBL} ^[16]	R/W LOW after BUSY LOW	0		0		0		0		0		ns
t _{WHI}	R/W HIGH after BUSY HIGH	20		30		30		35		35		ns
t _{BDD}	BUSY HIGH to Valid Data		25		30		35		45		45	ns
t _{DDD}	Write Data Valid to Read Data Valid		Note 17		Note 17		Note 17		Note 17		Note 17	ns
t _{WDD}	Write Pulse to Data Delay		Note 17		Note 17		Note 17		Note 17		Note 17	ns
INTERRUPT TIMING^[18]												
t _{WINS}	R/W to INTERRUPT Set Time		25		25		25		35		45	ns
t _{EINS}	$\overline{CE}$ to INTERRUPT Set Time		25		25		25		35		45	ns
t _{INS}	Address to INTERRUPT Set Time		25		25		25		35		45	ns
t _{OINR}	$\overline{OE}$ to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
t _{EINR}	$\overline{CE}$ to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns
t _{INR}	Address to INTERRUPT Reset Time ^[15]		25		25		25		35		45	ns

Notes:

15. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.

16. CY7C142/CY7C146 only.

17. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

- BUSY on Port B goes HIGH.
- Port B's address toggled.
- $\overline{CE}$ for Port B is toggled.
- R/W for Port B is toggled during valid read.

18. 52-pin LCC/PLCC versions only.

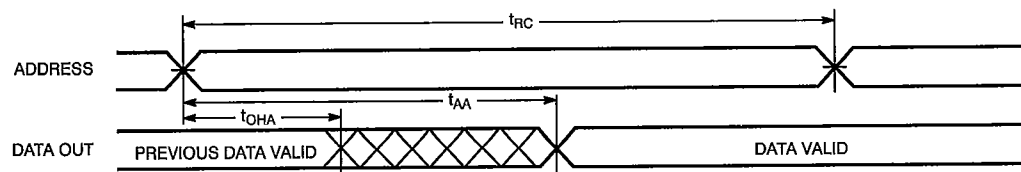
19. R/W is HIGH for read cycle.

20. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.

21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

22. If $\overline{OE}$ is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or t_{HZWE} + t_{SD} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

23. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high-impedance state.

Switching Waveforms
Read Cycle No. 1 (Either Port—Address Access)^[19,20]


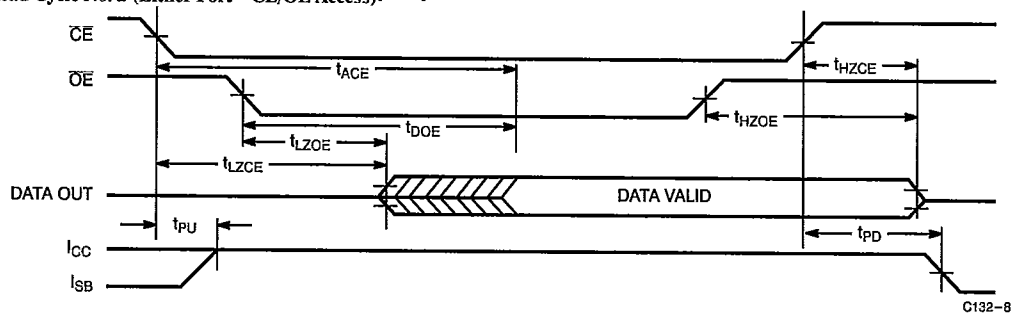
C132-7



CY7C132/CY7C136
CY7C142/CY7C146

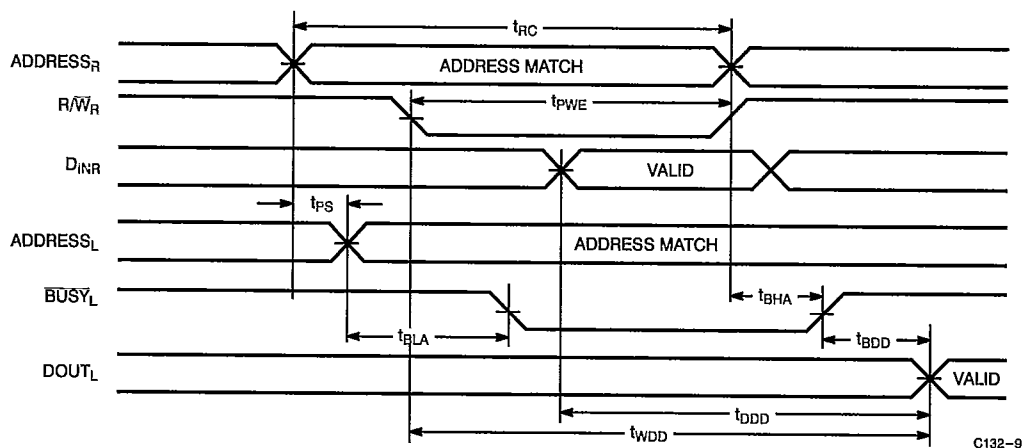
Switching Waveforms (continued)

Read Cycle No. 2 (Either Port— $\overline{\text{CE}}/\overline{\text{OE}}$ Access)^[19, 21]

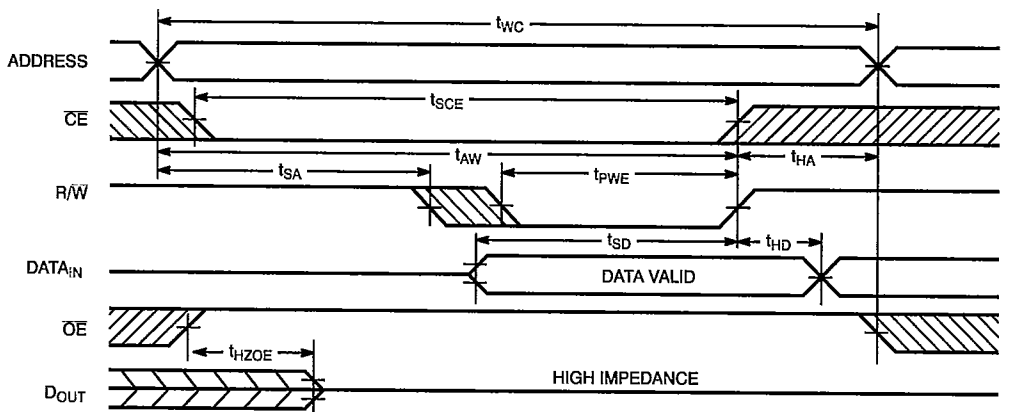


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Read Cycle No. 3 (Read with $\overline{\text{BUSY}}$ Master: CY7C132 and 7C136)^[20]



Write Cycle No.1 ($\overline{\text{OE}}$ Three-States Data I/Os—Either Port) ^[14, 22]

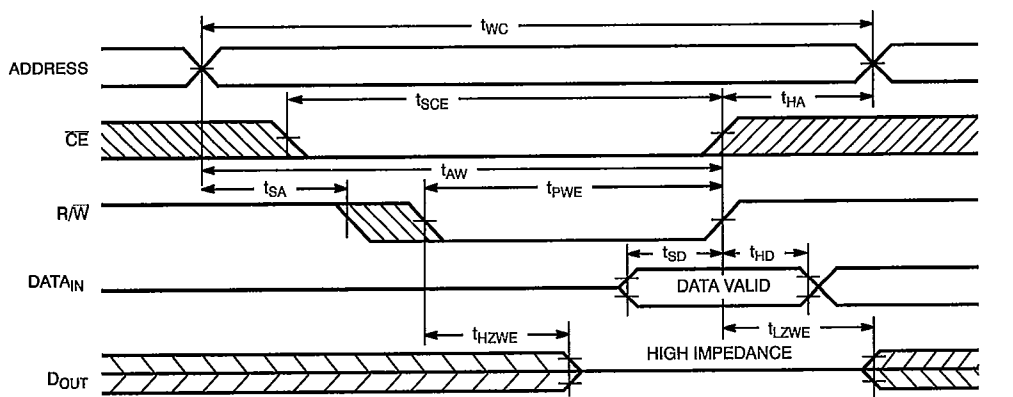




CY7C132/CY7C136
CY7C142/CY7C146

Switching Waveforms (continued)

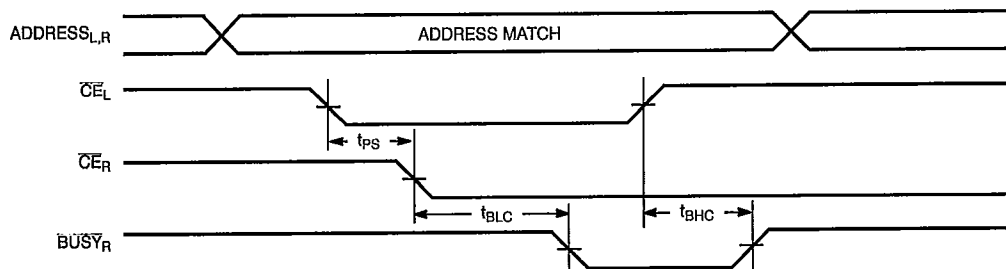
Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port)^[14,23]



C132-11

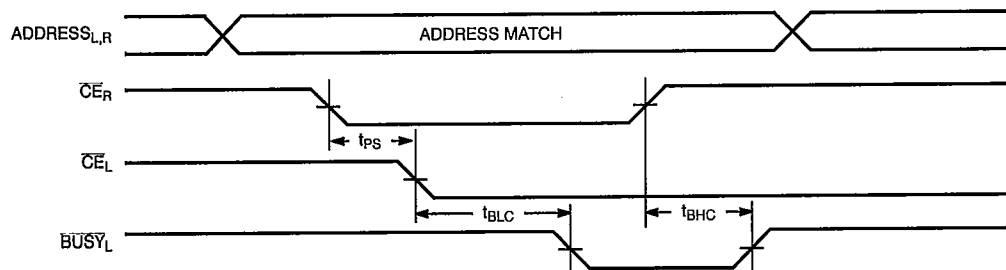
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



C132-12

$\overline{CE}_R$ Valid First:



C132-13



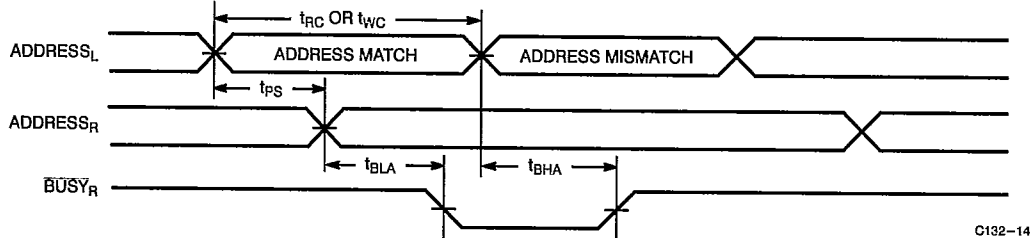
CY7C132/CY7C136
CY7C142/CY7C146

2
SRAMS

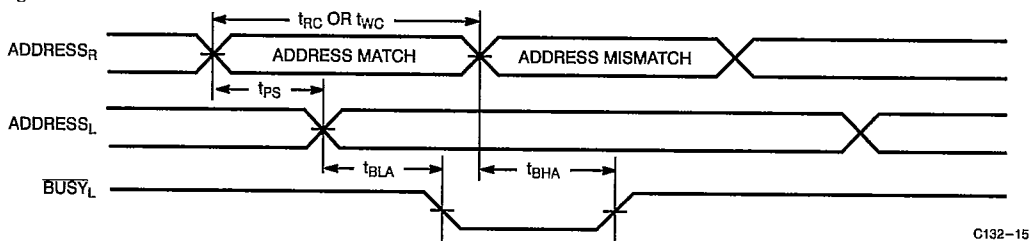
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

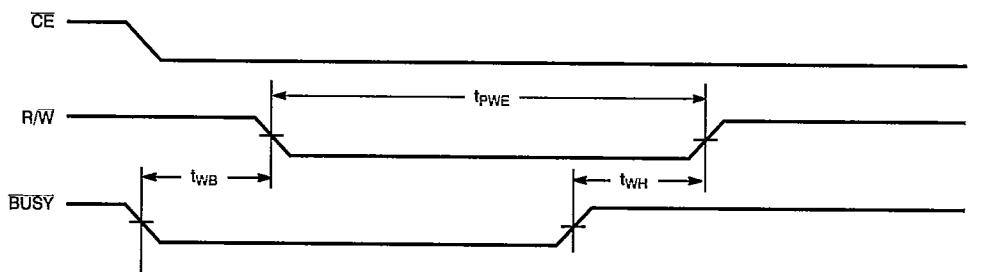
Left Address Valid First:

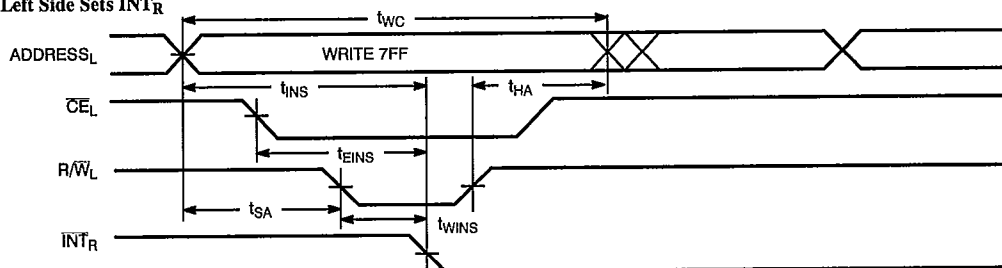


Right Address Valid First:

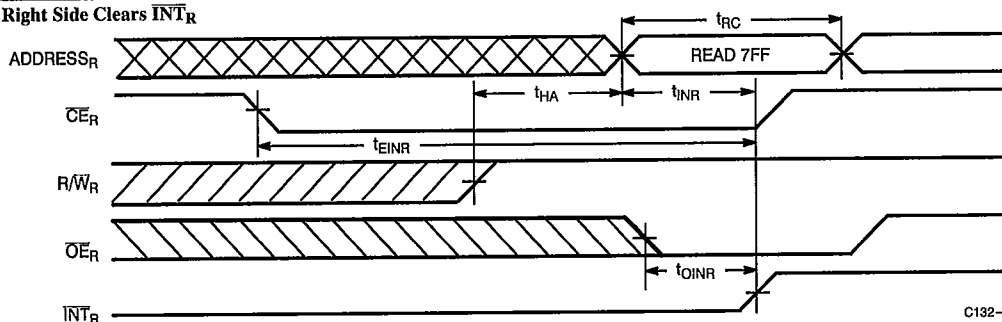


Busy Timing Diagram No. 3 (Write with $\overline{\text{BUSY}}$, Slave: CY7C142/CY7C146)

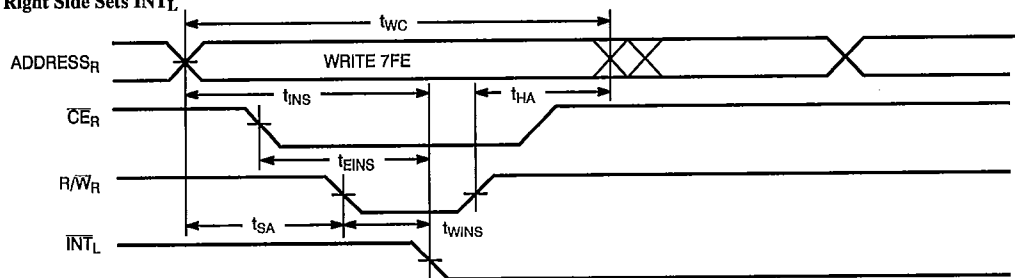


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CY7C142/CY7C146Interrupt Timing Diagrams^[18]Left Side Sets $\overline{INT}_R$ 

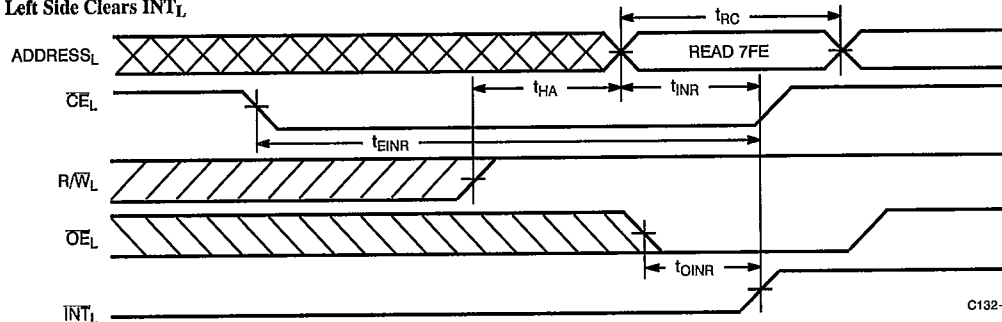
C132-17

Right Side Clears $\overline{INT}_R$ 

C132-18

Right Side Sets $\overline{INT}_L$ 

C132-19

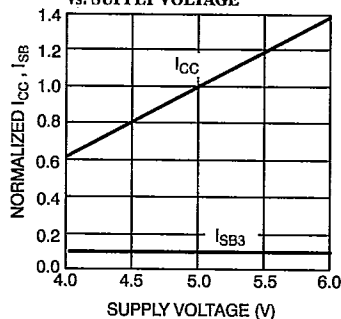
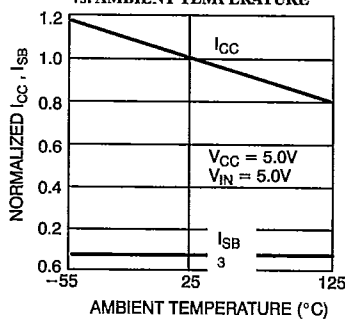
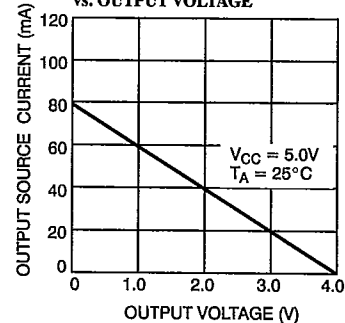
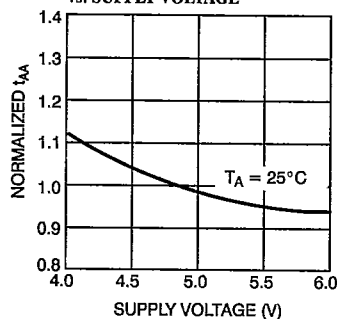
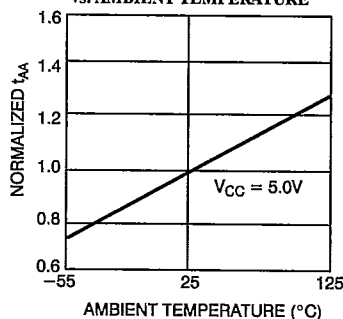
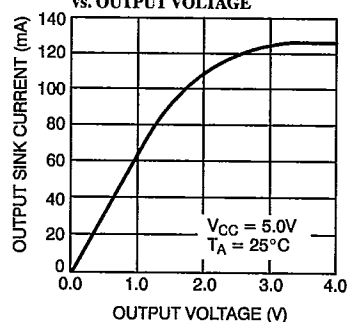
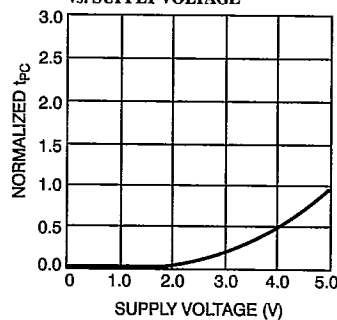
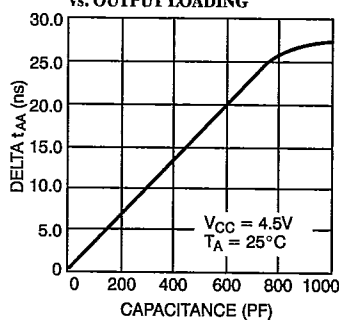
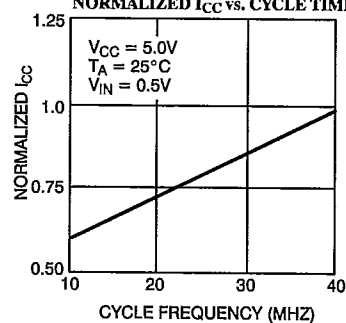
Left Side Clears $\overline{INT}_L$ 

C132-20


Typical DC and AC Characteristics

2

SRAMs

**NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE**

**NORMALIZED SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**

**OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE**

**NORMALIZED ACCESS TIME
vs. SUPPLY VOLTAGE**

**NORMALIZED ACCESS TIME
vs. AMBIENT TEMPERATURE**

**OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE**

**TYPICAL POWER-ON CURRENT
vs. SUPPLY VOLTAGE**

**TYPICAL ACCESS TIME CHANGE
vs. OUTPUT LOADING**

NORMALIZED ICC vs. CYCLE TIME


CYPRESS
SEMICONDUCTOR

CY7C132/CY7C136

CY7C142/CY7C146

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C132-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C132-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C132-35FMB	F78	48-Lead Quad Flatpack	
	CY7C132-35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C132-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C132-45FMB	F78	48-Lead Quad Flatpack	
	CY7C132-45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C132-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C132-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C132-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C132-55FMB	F78	48-Lead Quad Flatpack	
	CY7C132-55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C136-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C136-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C136-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C136-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C136-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C136-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C136-55LMB	L69	52-Square Leadless Chip Carrier	Military



CY7C132/CY7C136
CY7C142/CY7C146

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C142-30PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-30PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
35	CY7C142-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-35DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C142-35FMB	F78	48-Lead Quad Flatpack	
	CY7C142-35LMB	L68	48-Square Leadless Chip Carrier	
45	CY7C142-45PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-45PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-45DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C142-45FMB	F78	48-Lead Quad Flatpack	
	CY7C142-45LMB	L68	48-Square Leadless Chip Carrier	
55	CY7C142-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7C142-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7C142-55DMB	D26	48-Lead (600-Mil) Sidebrazed DIP	Military
	CY7C142-55FMB	F78	48-Lead Quad Flatpack	
	CY7C142-55LMB	L68	48-Square Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C146-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C146-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C146-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-35LMB	L69	52-Square Leadless Chip Carrier	Military
45	CY7C146-45JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-45JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-45LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7C146-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C146-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C146-55LMB	L69	52-Square Leadless Chip Carrier	Military



CY7C132/CY7C136
CY7C142/CY7C146

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3
I _{SB3}	1, 2, 3
I _{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Parameter	Subgroups
BUSY/INTERRUPT TIMING	
t _{BLA}	7, 8, 9, 10, 11
t _{BHA}	7, 8, 9, 10, 11
t _{BLC}	7, 8, 9, 10, 11
t _{BHC}	7, 8, 9, 10, 11
t _{PS}	7, 8, 9, 10, 11
t _{WINS}	7, 8, 9, 10, 11
t _{EINS}	7, 8, 9, 10, 11
t _{INS}	7, 8, 9, 10, 11
t _{OINR}	7, 8, 9, 10, 11
t _{EINR}	7, 8, 9, 10, 11
t _{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t _{WB} ^[24]	7, 8, 9, 10, 11
t _{WH}	7, 8, 9, 10, 11
t _{BDD}	7, 8, 9, 10, 11

Note:

24. CY7C142/CY7C146 only.

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