

SANYO

No.2421

LC3517B-10/12/15, LC3517BL-10/12/15

Asynchronous Silicon Gate CMOS LSI

2048 WORDS x 8 BITS CMOS STATIC RAM

General Description

The LC3517B/BL are fully asynchronous silicon gate CMOS static RAMs organized as 2048 words x 8 bits.

The LC3517B/BL have two control signal inputs: $\overline{OE}$ for high-speed memory access and $\overline{CE}$ for low standby current mode being valid at the time of battery backup usage. The LC3517B/BL have a full CMOS circuit configuration. Since the current dissipation is low at the data retention mode or standby mode, they are especially suited for use in memory systems whose power dissipation must be minimized and battery-powered portable systems.

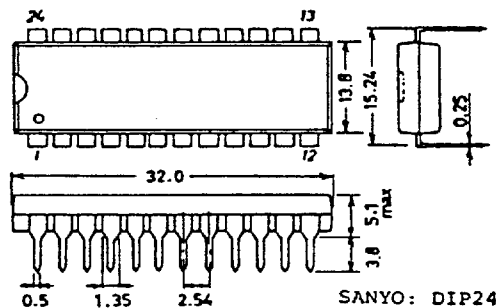
The LC3517BL guarantees a maximum standby current of 1uA at 60°C.

Features

- Address access time (t_{AA})
 - 100ns(max): LC3517B-10/BL-10
 - 120ns(max): LC3517B-12/BL-12
 - 150ns(max): LC3517B-15/BL-15
- Low current dissipation
 - Standby mode
 - 0.2uA(max) / $T_a=25^\circ\text{C}$
 - 1.0uA(max) / $T_a=60^\circ\text{C}$
 - 5.0uA(max) / $T_a=60^\circ\text{C}$
 - 30uA(max) / $T_a=85^\circ\text{C}$
 - Operating mode
 - 9mA(max) (at $f=1\text{MHz}$)
- Single 5V supply: $5V \pm 10\%$
- Data retention supply voltage: 2.0 to 5.5V
- No clock required (Fully static memory)
- Directly TTL compatible: All inputs and outputs
- Common data input and output using 3-state outputs
- 24-pin plastic DIP package

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass-produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

Case Outline 3072-D24NSEC
(unit:mm)

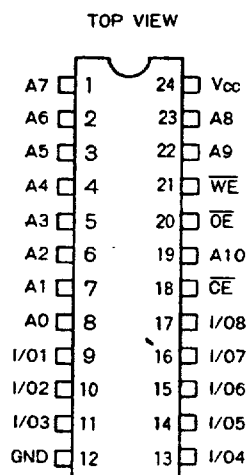


These specifications are subject to change without notice.

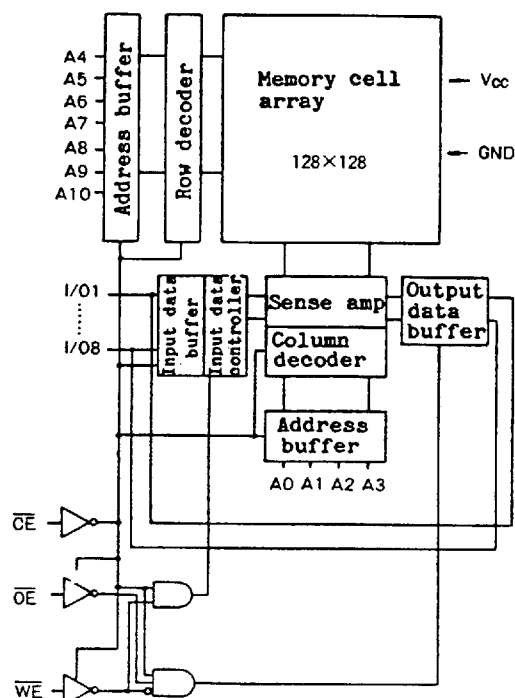
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Pin Assignment

Block Diagram



A0 to A10 Address input
WE Read/write control input
OE Output enable input
CE Chip enable input
I/O1 to I/O8 Data input/output
V_{CC}/GND Power supply pin



Function Table

Mode	CE	OE	WE	I/O	Supply Current
Read Cycle	L	L	H	Data output	I _{CCA}
Write Cycle	L	X	L	Data input	I _{CCA}
Output Disable	L	H	X	High impedance	I _{CCA}
Nonselect	H	X	X	High impedance	I _{CCS}

X:H or L

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits	unit
Maximum Supply Voltage	V _{CCmax}		+7.0	V
Input Pin Voltage	V _{IN}		-0.3 to V _{CC} +0.3	V
I/O Pin Voltage	V _{I/O}		-0.3 to V _{CC} +0.3	V
Operating Temperature	T _{opg}		-30 to +85	°C
Storage Temperature	T _{stg}		-55 to +125	°C

DC Allowable Operating Conditions at Ta=-30 to +85°C

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Input "H"-Level Voltage	V _{IH}	2.2		V _{CC} +0.3	V
Input "L"-Level Voltage	V _{IL}	-0.3		0.8	V

DC Electrical Characteristics at Ta=-30 to 85°C, V_{CC}=5V±10%

Parameter	Symbol	Conditions	min	typ*	max	unit
Input Leak Current	I _{LI}	V _{IN} =0 to V _{CC}	-1.0		1.0	uA
I/O Leak Current	I _{LO}	V _{CE} or V _{OE} =V _{IH} , V _{I/O} =0 to V _{CC}	-5.0		5.0	uA
Supply Current	I _{CCA1}	V _{CE} =0V, V _{IN} =V _{CC} /GND, I _{I/O} =0mA		2	5	mA
	I _{CCA2}	V _{CE} =V _{IL} , V _{IN} =V _{IH} /V _{IL} , I _{I/O} =0mA		5	15	mA
	I _{CCA3}	min cycle, duty=100%, I _{I/O} =0mA			50	mA
	I _{CCA4}	Cycle time=1us, V _{CE} =0V, V _{IN} =V _{CC} /GND, I _{I/O} =0mA		4	9	mA
Standby Supply Current	I _{CCS1}	V _{CE} =V _{CC} -0.2V, V _{IN} =0 to V _{CC}			5.0	uA
		LC3517B Ta=60°C				
		-10/12/15 Ta=85°C			30	uA
	I _{CCS2}	LC3517BL Ta=25°C			0.2	uA
		-10/12/15 Ta=60°C			1.0	uA
Output "H"-Level Voltage	V _{OH}	V _{CE} =V _{IH} , V _{IN} =0 to V _{CC} , I _{OH} =-1.0mA	2.4		3.0	V
Output "L"-Level Voltage	V _{OL}	I _{OL} =2.0mA			0.4	V

* Reference value at V_{CC}=5.0V, Ta=+25°C

Input/Output Capacitance at Ta=+25°C, f=1MHz

Parameter	Symbol	Conditions	min	typ	max	unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V			10	pF
Input Capacitance	C _{IN}	V _{IN} =0V			5	pF

AC Electrical Characteristics at Ta=-30 to +85°C, V_{CC}=5V±10%

AC Test Conditions

Input pulse voltage level: 0.6V, 2.4V

Input rise/fall time: 5ns

Input/output timing level: Input "H" level V_{IH}=2.2V, Output "H" level V_{OH}=2.2V
Input "L" level V_{IL}=0.8V, Output "L" level V_{OL}=0.8V

Output load: 1TTL gate + C_L=100pF
(Including jig capacitance)

Read Cycle

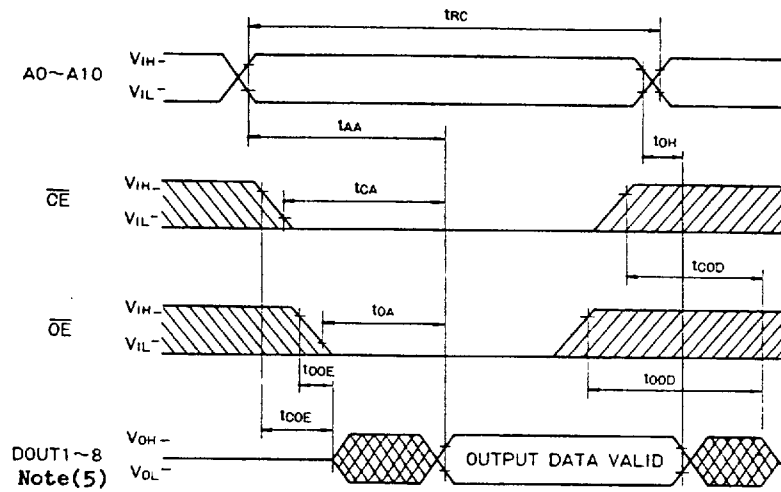
Parameter	Symbol	LC3517B-10 LC3517BL-10		LC3517B-12 LC3517BL-12		LC3517B-15 LC3517BL-15		unit
		min	max	min	max	min	max	
Read Cycle Time	t _{RC}	100		120		150		ns
Address Access Time	t _{AA}		100		120		150	ns
OE Access Time	t _{OA}		60		70		80	ns
CE Access Time	t _{CA}		100		120		150	ns
Output Hold Time	t _{OH}	20		20		20		ns
OE-Output Enable Time	t _{OOE}	5		5		5		ns
CE-Output Enable Time	t _{COE}	10		10		10		ns
OE-Output Disable Time	t _{OOD}		30		40		50	ns
CE-Output Disable Time	t _{COD}		30		40		50	ns

Write Cycle

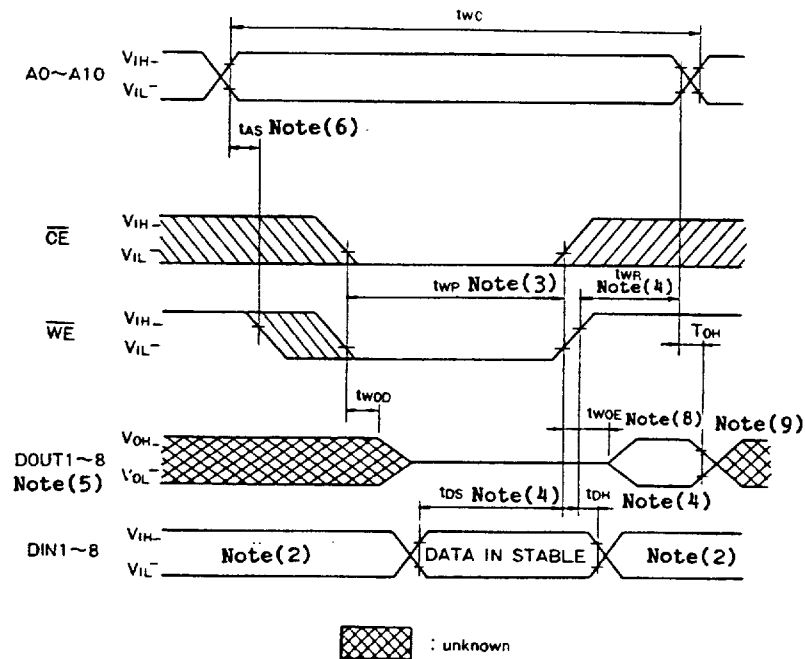
Parameter	Symbol	LC3517B-10 LC3517BL-10		LC3517B-12 LC3517BL-12		LC3517B-15 LC3517BL-15		unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100		120		150		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	80		100		120		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Setup Time	t_{DS}	50		60		70		ns
Data Hold Time	t_{DH}	0		0		0		ns
$\overline{WE}$ -Output Enable Time	t_{WOE}	5		5		5		ns
$\overline{WE}$ -Output Disable Time	t_{WOD}		30		40		50	ns

Timing Chart

[Read Cycle] Note(1)

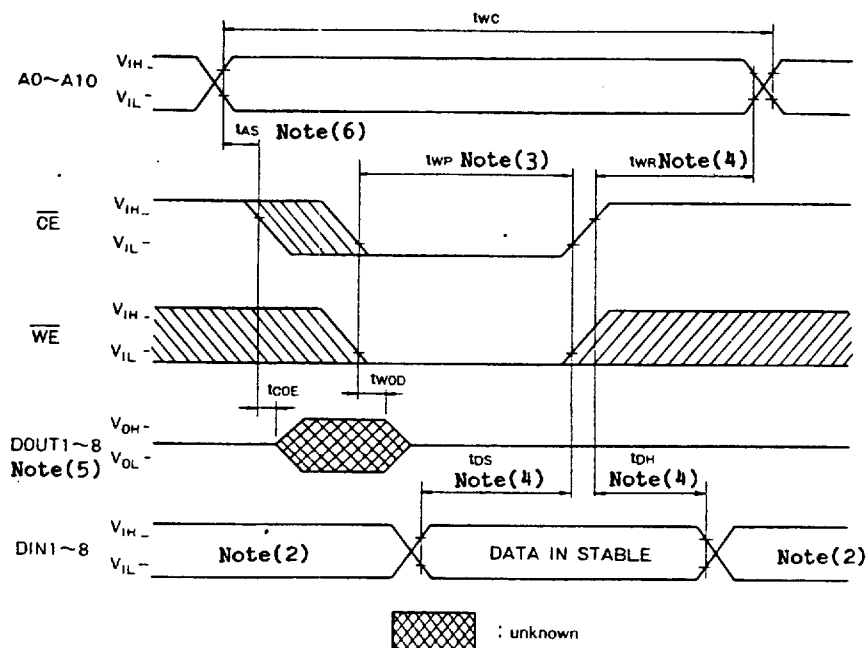


[Write Cycle 1] Note(7)



unknown

[Write Cycle 2] Note(7)



- Note) (1) $\overline{WE}$ must be high during read cycle.
 (2) When D_{OUT} is in the output state, no opposite phase signal must be applied externally.
 (3) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
 (4) t_{WR} , t_{DS} , t_{DH} are referenced to the earlier going high of $\overline{CE}$ or $\overline{WE}$.
 (5) D_{OUT} is in a high impedance state when $\overline{OE}$ is high or $\overline{CE}$ is high or $\overline{WE}$ is low.
 (6) t_{AS} is referenced to the point at which all of $\overline{CE}$, $\overline{WE}$ go low.
 (7) D_{OUT} is in a high impedance state when $\overline{OE}$ is high during write cycle.
 (8) D_{OUT} is the same phase as write data of this write cycle.
 (9) D_{OUT} is the read-out data of the next address.

Data Retention Characteristics at $T_a = -30$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ	max	unit
Data Retention Supply Voltage	V_{DR}	$V_{CE} = V_{CC}, V_{IN} = 0 \text{ to } V_{CC}$	2.0		5.5	V
Data Retention Supply Current	I_{CCDR}	$V_{CE} = V_{CC}$				
		$V_{CC} = 3.0\text{V}$				
		$V_{IN} = 0 \text{ to } V_{CC}$				
$\overline{CE}$ Setup Time	t_{CDR}		0			us
$\overline{CE}$ Hold Time	t_R					us
Note) (1) t_{RC} = Read cycle time.				t_{RC}		us

