512K x 36 / 1M x 18 Flow-Thru SRAM

Features

- **Fast access times: 6.5, 7.5, 8.5 ns**
- **Fast clock speed: 133, 117, 100 MHz**
- **Provide high-performance 2-1-1-1 access rate**
- **Optimal for depth expansion**
- **2.5V ± 5% power supply**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Chip enable for address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down available using ZZ mode or CE deselect**
- **Available in 100-pin TQFP, 119-ball BGA, and 165-ball FBGA Packages**
- **JTAG boundary scan for BGA packaging version**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced single layer polysilicon, three-layer metal technology. Each memory cell consists of six transistors.

The CY7C1381CV25 and CY7C1383CV25 SRAMs integrate 524,288x36 and 1,048,576x18SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable (CE), Burst Control Inputs (ADSC, ADSP, and ADV), Write Enables (BWa, BWb, BWc, BWd, and BWE), and Global Write (GW).

Asynchronous inputs include the output enable (OE) and burst mode control (MODE). The data outputs (Q), enabled by OE, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor (ADSP) or Address Status Controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BWa controls DQ1–DQ8 and DP1. BWb controls DQ9–DQ16 and DP2. BWc controls DQ17–DQ24and DP3. BWd controls DQ25–DQ32 and DP4. BWa, BWb BWc, and BWd can be active only with BWE being LOW. GW being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the next ReaD cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

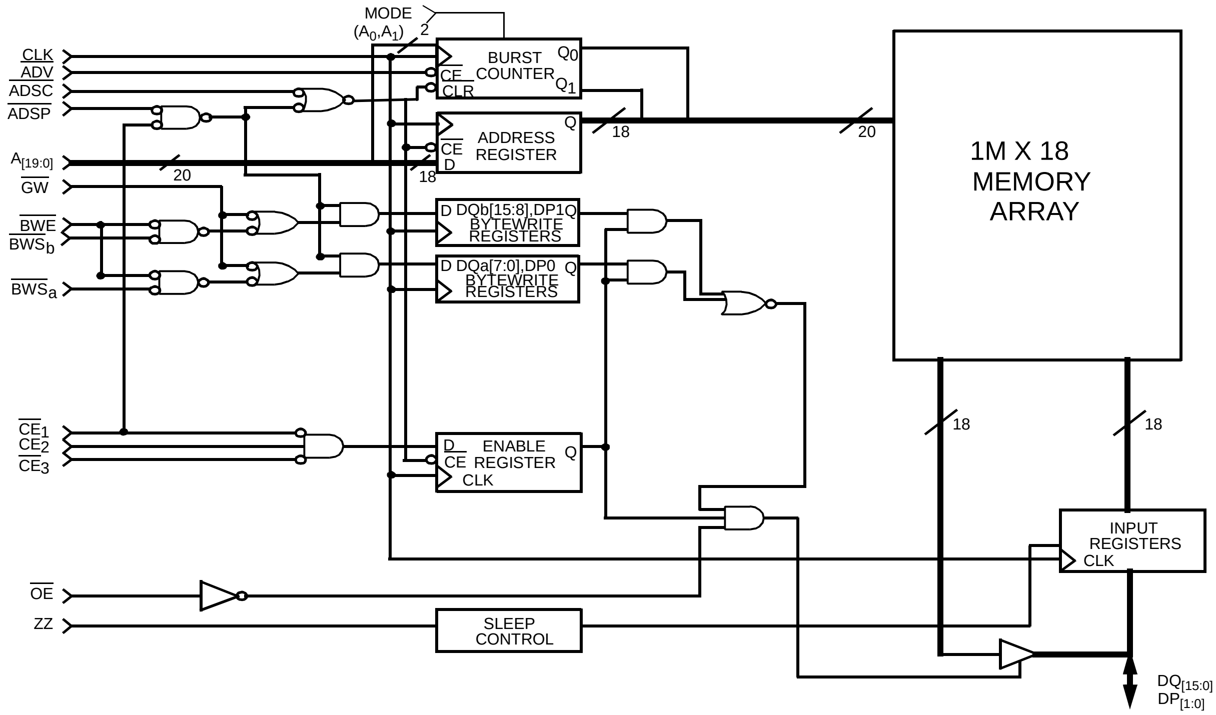
All inputs and outputs of the CY7C1381CV25 and the CY7C1383CV25 are JEDEC standard JESD8-5 compatible.

Selection Guide

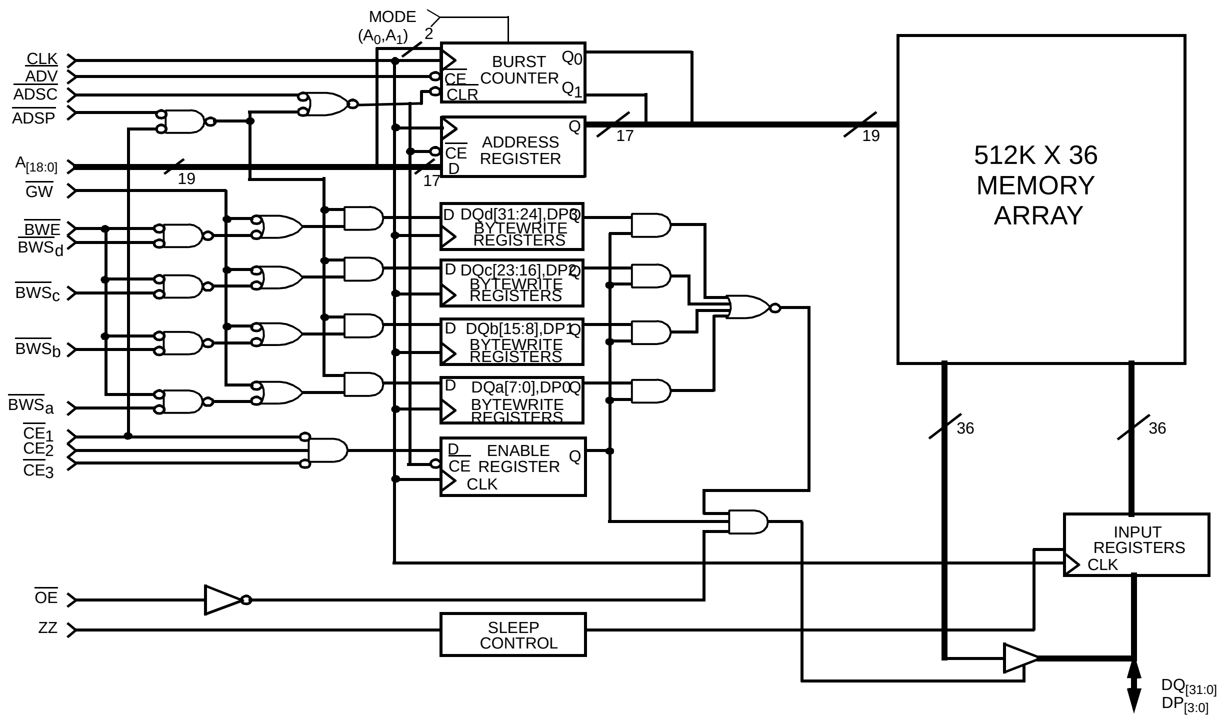
	133 MHz	117 MHz	100 MHz	Unit
Maximum Access Time	6.5	7.5	8.5	ns
Maximum Operating Current	210	190	175	mA
Maximum CMOS Standby Current	70	70	70	mA

Functional Block Diagram

Logic Block Diagram x18

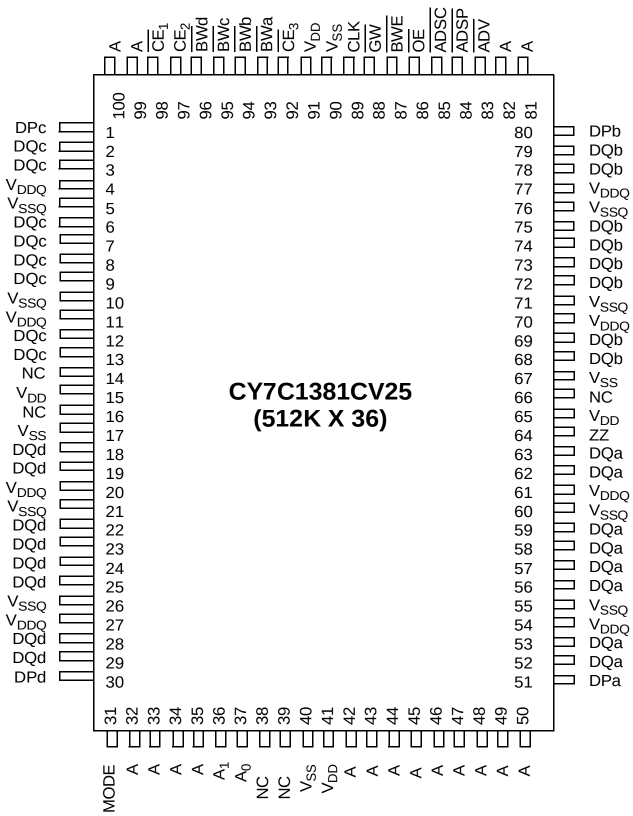


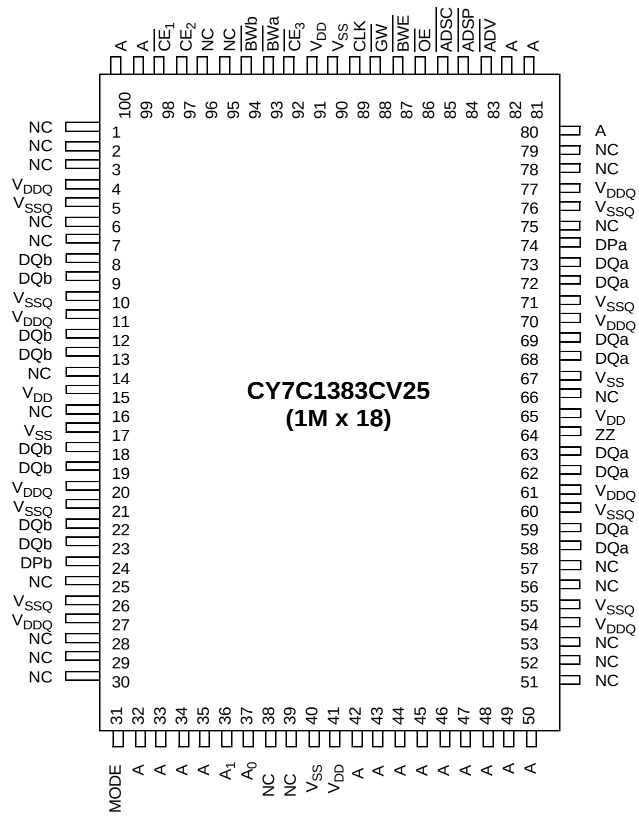
Logic Block Diagram x36:



Pin Configurations

100-Pin TQFP Packages





Pin Configurations (continued)

119-Ball BGA

CY7C1381CV25 (512K x 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE}_1$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	V_{SS}	$\overline{GW}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	CLK	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{BWE}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A1	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A0	V_{SS}	DQPa	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	NC	72M	A	A	A	36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1383CV25 (1M x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	A	A	$\overline{ADSC}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQb	NC	V_{SS}	NC	V_{SS}	DQPa	NC
E	NC	DQb	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{BWb}$	$\overline{ADV}$	V_{SS}	NC	DQa
H	DQb	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQb	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	CLK	V_{SS}	NC	DQa
L	DQb	NC	V_{SS}	NC	$\overline{BWa}$	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	A1	V_{SS}	DQa	NC
P	NC	DQPb	V_{SS}	A0	V_{SS}	NC	DQa
R	NC	A	MODE	V_{DD}	NC	A	NC
T	72M	A	A	36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Pin Configurations (continued)

165-Ball Bump FBGA

CY7C1381CV25 (512K x 36) - 11 x 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC	A	CE_2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	144M
C	DPc	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPb
D	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
E	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
F	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
G	DQc	DQc	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQb	DQb
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
K	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
L	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
M	DQd	DQd	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	DQa
N	DPd	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DPa
P	NC	72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1383CV25 (1M x 18) - 11 x 15 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}_1$	$\overline{BWb}$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
B	NC	A	CE_2	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	144M
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DPa
D	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
E	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
F	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
G	NC	DQb	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQa
H	NC	V_{SS}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
K	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
L	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
M	DQb	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQa	NC
N	DPb	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC	72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A0 A1 A	Input-Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
BWa BWb BWc BWd	Input-Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input-Synchronous	**Global Write Enable Input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $BW_{a,b,c,d}$ and BWE).
BWE	Input-Synchronous	**Byte Write Enable Input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. ADSP is ignored if $\overline{CE_1}$ is HIGH. (TQFP Only)
CE_2	Input-Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. (TQFP Only)
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
OE	Input-Asynchronous	**Output Enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	**Advance Input signal, sampled on the rising edge of CLK**. When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	**Address Strobe from Processor, sampled on the rising edge of CLK**. When asserted LOW, A is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ASDP is ignored when $\overline{CE_1}$ is deasserted HIGH.
ADSC	Input-Synchronous	**Address Strobe from Controller, sampled on the rising edge of CLK**. When asserted LOW, $A_{[x:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
MODE	Input Pin	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
DQa, DPa DQb, DPb DQc, DPc DQd, DPd	I/O-Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[x]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQa–DQd and DQPa–DQPd are placed in a three-state condition. DQ a,b,c, and d are 8 bit wide. DP a,b,c, and d are 1 bit wide.
TDO	JTAG serial output Synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. (BGA and FBGA Only)
TDI	JTAG serial input Synchronous	**Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK.(BGA and FBGA Only)

Pin Definitions (continued)

Name	I/O	Description
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK. (BGA and FBGA Only)
TCK	JTAG serial clock	**Serial clock to the JTAG circuit**. (BGA and FBGA Only)
V_{DD}	Power Supply	**Power supply inputs to the core of the device**. Should be connected to 2.5V power supply.
V_{SS}	Ground	**Ground for the core of the device**. Should be connected to ground of the system.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**. Should be connected to a 2.5V power supply.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**. Should be connected to ground of the system.
NC	-	**No connects**. Pins are not internally connected.
36M 72M 144M		**No connects**. Reserved for address expansion

Functional Description

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) CE_1, CE_2, CE_3 are all asserted active, and (3) the write signals (GW, BWE) are all deasserted HIGH. ADSP is ignored if CE_1 is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. If the OE input is asserted LOW, the requested data will be available at the data outputs a maximum of t_{CDV} after clock rise. ADSP is ignored if CE_1 is HIGH.

Single Write Accesses Initiated by ADSP

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) chip enable asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals (GW, BWE, and BWx) and ADV inputs are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the appropriate data will be latched and written into the device. The CY7C1381CV25/CY7C1383CV25 provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write (BWa,b,c,d for CY7C1381CV25 and BWa,b for CY7C1383CV25) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. All I/Os are three-stated during a byte write.

Because the CY7C1381CV25/CY7C1383CV25 is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQx inputs. Doing so will three-state the output drivers. As a safety precaution, DQx are automatically three-stated whenever a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the write inputs (GW, BWE, and BWx) are asserted active to conduct a write to the desired byte(s). ADSC is ignored if ADSP is active LOW.

The address presented to $A_{[17:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The ADV input is ignored during this cycle. If a global write is conducted, the data presented to the DQx is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. All I/Os are three-stated during a byte write because the CY7C1381CV25/CY7C1383CV25 is a common I/O device, the Output Enable (OE) must be deasserted HIGH before presenting data to the DQx inputs. Doing so will three-state the output drivers. As a safety precaution, DQx are automatically three-stated whenever a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1381CV25/CY7C1383CV25 provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ HIGH places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW. Leaving ZZ unconnected defaults the device into an active state.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{CCZZ}	Sleep mode stand-by current	ZZ $\geq V_{DD} - 0.2V$		60	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq 0.2V$	$2t_{CYC}$		ns

Cycle Descriptions[1, 2, 3]

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	CE_2	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	0	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	0	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	0	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	0	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	0	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	0	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	0	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	0	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	0	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	0	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	0	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	0	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	0	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	0	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	0	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	0	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	0	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	0	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	0	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	0	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	0	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	0	X	X	1	X	1	1	X	Hi-Z	Write
ZZ "sleep"	None	1	X	X	X	X	X	X	X	Hi-Z	X

Note:
1. X = "Don't Care", 1 = HIGH, 0 = LOW.
2. The SRAM always initiates a read cycle when $\overline{ADSP}$ asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}$x. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. $\overline{OE}$ is a "Don't Care" for the remainder of the write cycle.
3. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ = High-Z when $\overline{OE}$ is inactive or when the device is deselected, and DQ = data when $\overline{OE}$ is active.

Write Cycle Description[1, 2, 3]

Function (CY7C1381CV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BWd}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{BWa}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 – DQa	1	0	1	1	1	0
Write Byte 1 – DQb	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 – DQc	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 – DQd	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Function (CY7C1383CV25)	$\overline{GW}$	$\overline{BWE}$	$\overline{BWb}$	$\overline{BWa}$
Read	1	1	X	X
Read	1	0	1	1
Write Byte 0 – DQ_a and DP_a	1	0	1	0
Write Byte 1 – DQ_b and DP_b	1	0	0	1
Write All Bytes	1	0	0	0
Write All Bytes	0	X	X	X

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1381CV25/CY7C1383CV25 incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP)—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a xx-bit-long register, and the x18 configuration has a yy-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the

SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Input and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

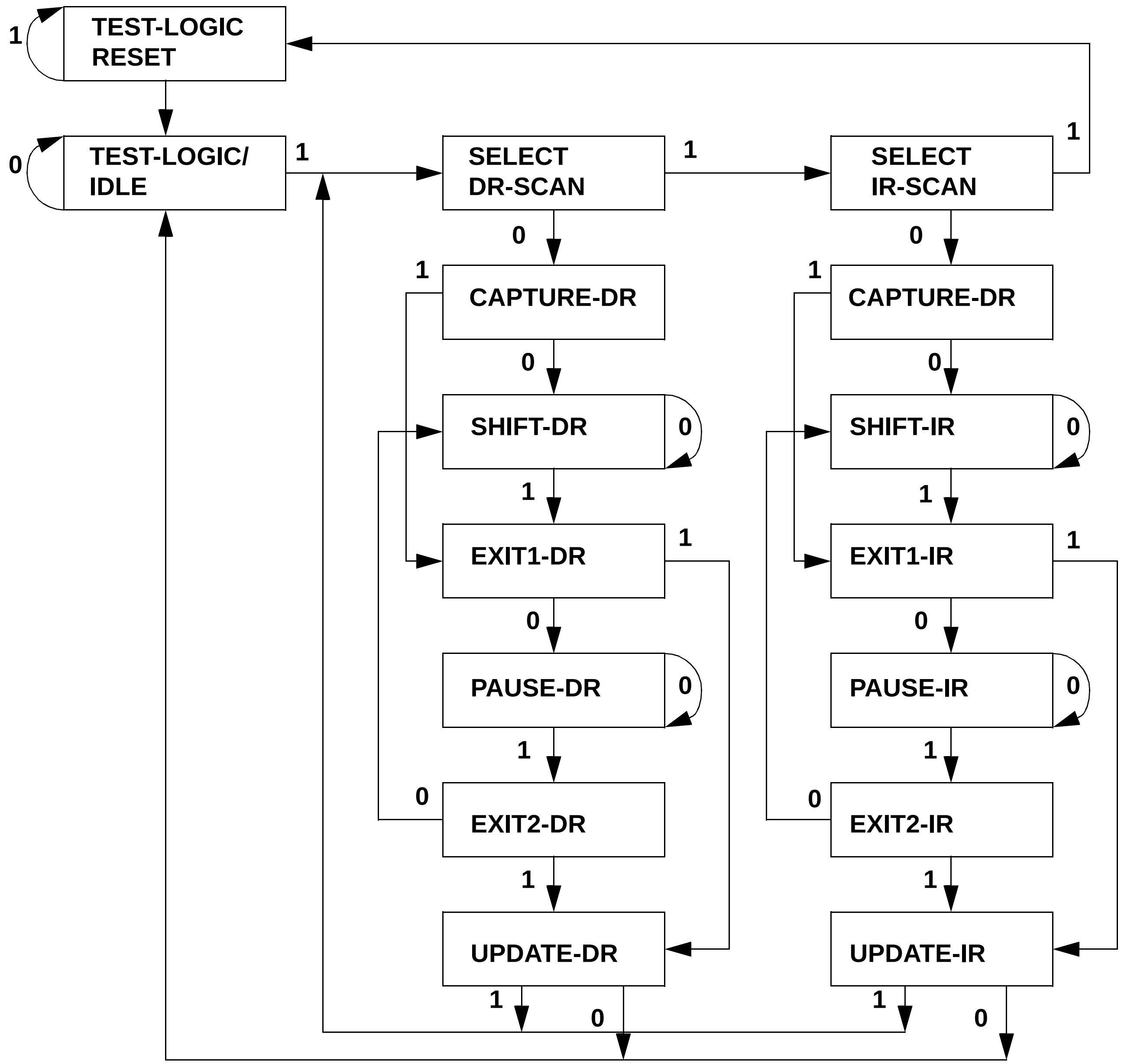
Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

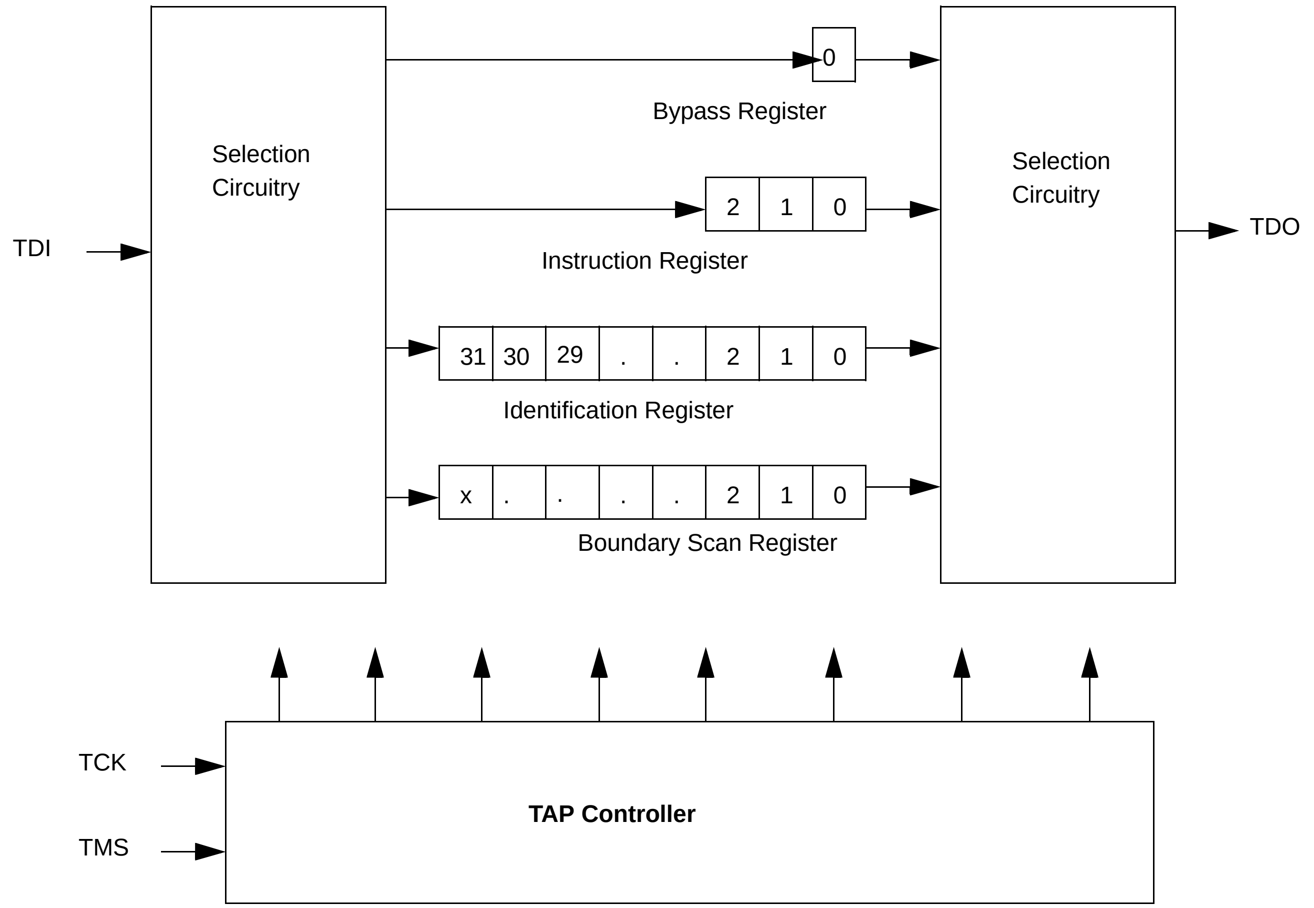
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram



Note: The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	2.1		
V_{OL1}	Output LOW Voltage	I_{OL} = 1.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

Notes:

4. All Voltage referenced to Ground.
5. Overshoot: $V_{IH}(AC) \leq V_{DD}+1.5V$ for $t \leq t_{TCYC}/2$, Undershoot: $V_{IL}(AC) \geq -0.5V$ for $t \leq t_{TCYC}/2$.

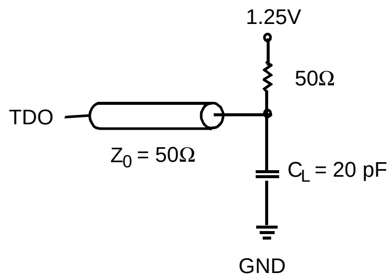
TAP AC Switching Characteristics Over the Operating Range[6, 7]

Parameters	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{CS}	Capture Set-up to TCK Rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after Clock Rise	10		ns
t_{CH}	Capture Hold after Clock Rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

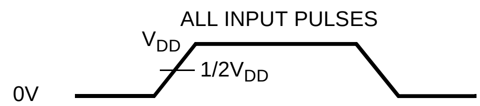
Notes:

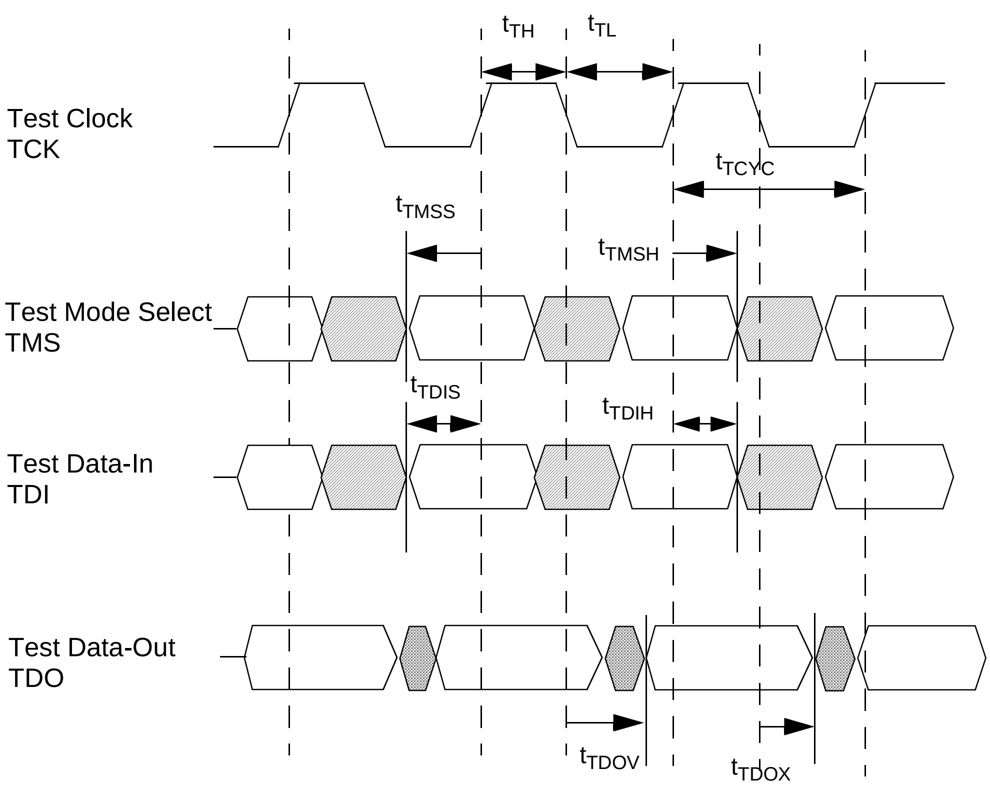
6. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
7. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 V/ ns.

TAP Timing and Test Conditions



(a)





Identification Register Definitions

Instruction Field	512K x 36	1M x 18	Description
Revision Number (31:28)	0100	0100	Reserved for version number
Cypress Device ID (27:24)	1011	1011	Reserved for internal use
Device type (23:18)	000001	000001	Defines memory type and architecture
Device width and density (17:12)	100101	010101	Defines width and density
Cypress JEDEC ID (11:0)	000001101001	000001101001	Allows unique identification of SRAM vendor

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1 compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order (512K X 36)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	TBD	TBD	36	TBD	TBD
2	TBD	TBD	37	TBD	TBD
3	TBD	TBD	38	TBD	TBD
4	TBD	TBD	39	TBD	TBD
5	TBD	TBD	40	TBD	TBD
6	TBD	TBD	41	TBD	TBD
7	TBD	TBD	42	TBD	TBD
8	TBD	TBD	43	TBD	TBD
9	TBD	TBD	44	TBD	TBD
10	TBD	TBD	45	TBD	TBD
11	TBD	TBD	46	TBD	TBD
12	TBD	TBD	47	TBD	TBD
13	TBD	TBD	48	TBD	TBD
14	TBD	TBD	49	TBD	TBD
15	TBD	TBD	50	TBD	TBD
16	TBD	TBD	51	TBD	TBD
17	TBD	TBD	52	TBD	TBD
18	TBD	TBD	53	TBD	TBD
19	TBD	TBD	54	TBD	TBD
20	TBD	TBD	55	TBD	TBD
21	TBD	TBD	56	TBD	TBD
22	TBD	TBD	57	TBD	TBD
23	TBD	TBD	58	TBD	TBD
24	TBD	TBD	59	TBD	TBD
25	TBD	TBD	60	TBD	TBD
26	TBD	TBD	61	TBD	TBD
27	TBD	TBD	62	TBD	TBD
28	TBD	TBD	63	TBD	TBD
29	TBD	TBD	64	TBD	TBD
30	TBD	TBD	65	TBD	TBD
31	TBD	TBD	66	TBD	TBD
32	TBD	TBD	67	TBD	TBD
33	TBD	TBD	68	TBD	TBD
34	TBD	TBD	69	TBD	TBD
35	TBD	TBD	70	TBD	TBD

Boundary Scan Order (1M X 18)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	TBD	TBD	36	TBD	TBD
2	TBD	TBD	37	TBD	TBD
3	TBD	TBD	38	TBD	TBD
4	TBD	TBD	39	TBD	TBD
5	TBD	TBD	40	TBD	TBD
6	TBD	TBD	41	TBD	TBD
7	TBD	TBD	42	TBD	TBD
8	TBD	TBD	43	TBD	TBD
9	TBD	TBD	44	TBD	TBD
10	TBD	TBD	45	TBD	TBD
11	TBD	TBD	46	TBD	TBD
12	TBD	TBD	47	TBD	TBD
13	TBD	TBD	48	TBD	TBD
14	TBD	TBD	49	TBD	TBD
15	TBD	TBD	50	TBD	TBD
16	TBD	TBD	51	TBD	TBD
17	TBD	TBD	52	TBD	TBD
18	TBD	TBD	53	TBD	TBD
19	TBD	TBD	54	TBD	TBD
20	TBD	TBD	55	TBD	TBD
21	TBD	TBD	56	TBD	TBD
22	TBD	TBD	57	TBD	TBD
23	TBD	TBD	58	TBD	TBD
24	TBD	TBD	59	TBD	TBD
25	TBD	TBD	60	TBD	TBD
26	TBD	TBD	61	TBD	TBD
27	TBD	TBD	62	TBD	TBD
28	TBD	TBD	63	TBD	TBD
29	TBD	TBD	64	TBD	TBD
30	TBD	TBD	65	TBD	TBD
31	TBD	TBD	66	TBD	TBD
32	TBD	TBD	67	TBD	TBD
33	TBD	TBD	68	TBD	TBD
34	TBD	TBD	69	TBD	TBD
35	TBD	TBD	70	TBD	TBD

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.........–0.3V to +3.6V

DC Voltage Applied to Outputs
in High Z State[8].....................................–0.5V to V_{DDQ} + 0.5V

DC Input Voltage[8].................................–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temp.[9]	V_{DD}/V_{DDQ}
Com'l	0°C to 70°C	2.5 ± 5%
Ind'l	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

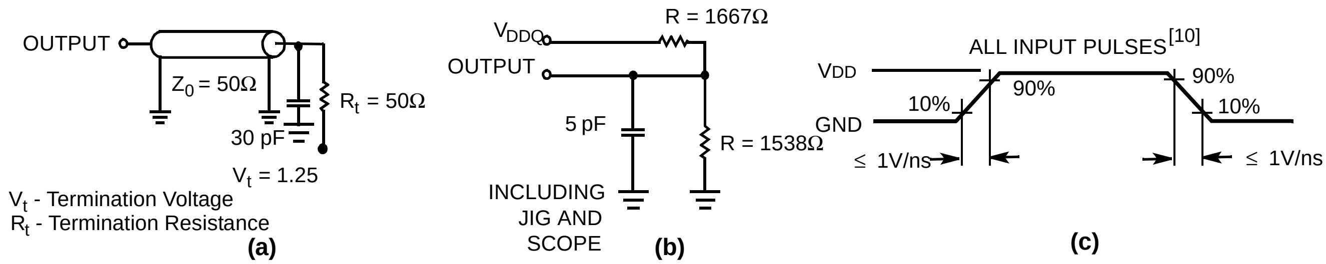
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD} / V_{DDQ}	Power Supply Voltage			2.375	2.625	V
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			1.7	V_{dd} + 0.3	V
V_{IL}	Input LOW Voltage[8]			–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}		-5	5	µA
	Input Current of MODE			–30	30	µA
	Input Current of ZZ	Input = V_{SS}		–30	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ $V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		210	mA
			8.5-ns cycle, 117 MHz		190	mA
			10-ns cycle, 100 MHz		175	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		120	mA
			8.5-ns cycle, 117 MHz		110	mA
			10-ns cycle, 100 MHz		100	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0	All Speed grades		70	mA
I_{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz		105	mA
			8.5-ns cycle, 117 MHz		100	mA
			10-ns cycle, 100 MHz		95	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	All Speed grades		80	mA

Notes:
8. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
9. T_A is the temperature.

Capacitance[10]

Parameter	Description	Test Conditions	Max.			Unit
			100-TQFP	119-BGA	165-FBGA	
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	TBD	TBD	TBD	pF
C_{CLK}	Clock Input Capacitance		TBD	TBD	TBD	pF
$C_{I/O}$	Input/Output Capacitance		TBD	TBD	TBD	pF

AC Test Loads and Waveforms[11]



Thermal Resistance[10]

Description	Test Conditions	Symbol	TQFP	119 BGA	165 FBGA	Units
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch^2, 2-layer printed circuit board	Θ_{JA}	31	45	46	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	6	7	3	°C/W

Note:

10. Tested initially and after any design or process changes that may affect these parameters.
11. Input waveform should have a slew rate of ≤ 1 V/ns.

Switching Characteristics Over the Operating Range[12, 13, 14]

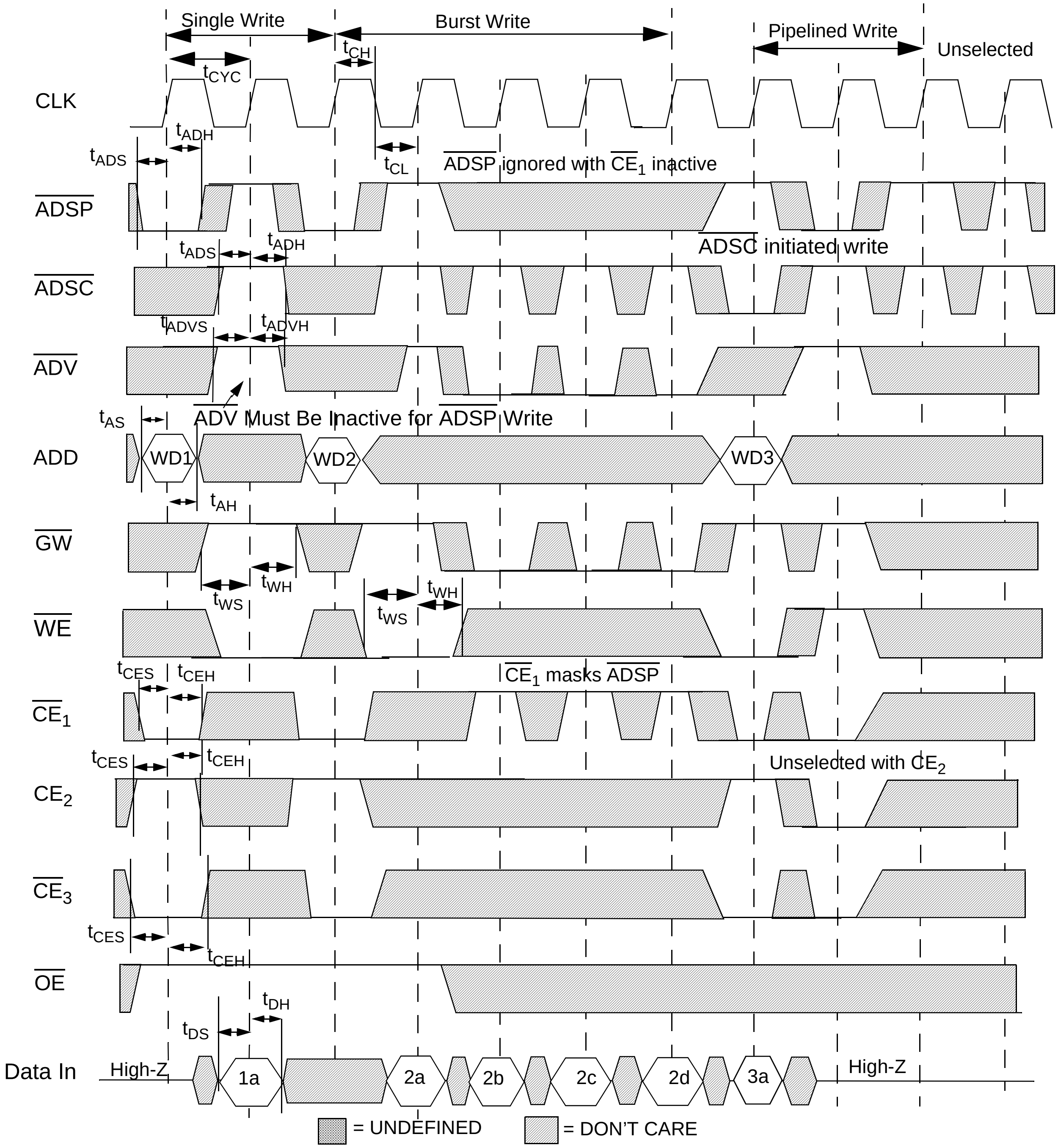
Parameter	Description	133		117		100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	7.5		8.5		10.0		ns
t_{CH}	Clock HIGH	2.1		2.3		2.5		ns
t_{CL}	Clock LOW	2.1		2.3		2.5		ns
t_{AS}	Address Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		6.5		7.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_x$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{WEH}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_x$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.5		1.5		1.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CES}	Chip enable Set-up	1.5		1.5		1.5		ns
t_{CEH}	Chip enable Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[13, 14]		4.0		4.0		5.0	ns
t_{CLZ}	Clock to Low-Z[13, 14]	2.0		2.0		2.0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[13, 14]		4.0		4.0		5.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[13, 14]	0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[13]		3.2		3.4		3.8	ns

Notes:

12. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a), (b) and (c) of AC Test Loads.
13. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
14. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

Switching Waveforms

Write Cycle Timing[15, 16]

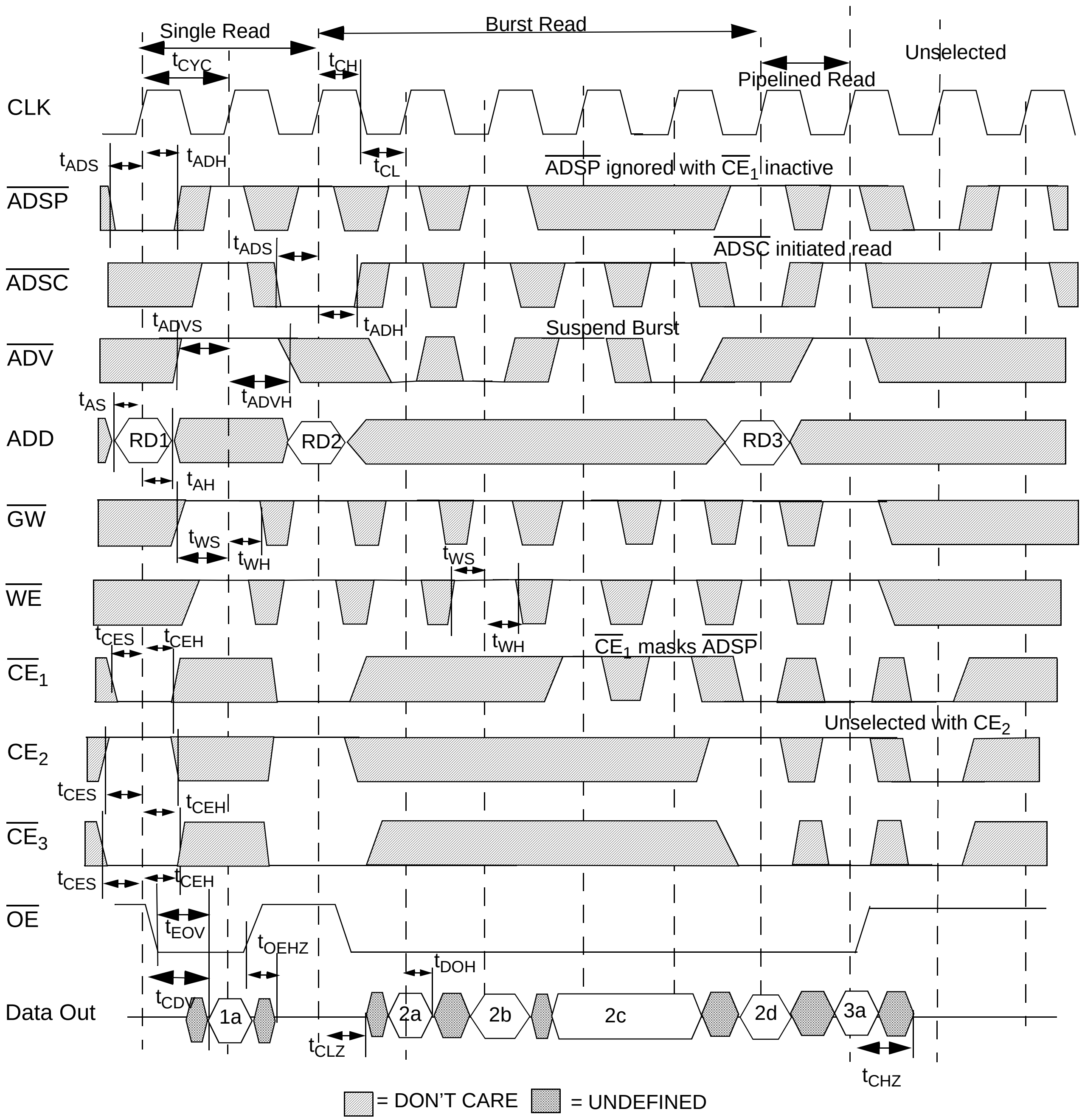


Notes:

15. WE is the combination of BWE, BWx, and GW to define a write cycle (see Write Cycle Descriptions table).
16. WDx stands for Write Data to Address X.

Switching Waveforms (continued)

Read Cycle Timing[15, 17]

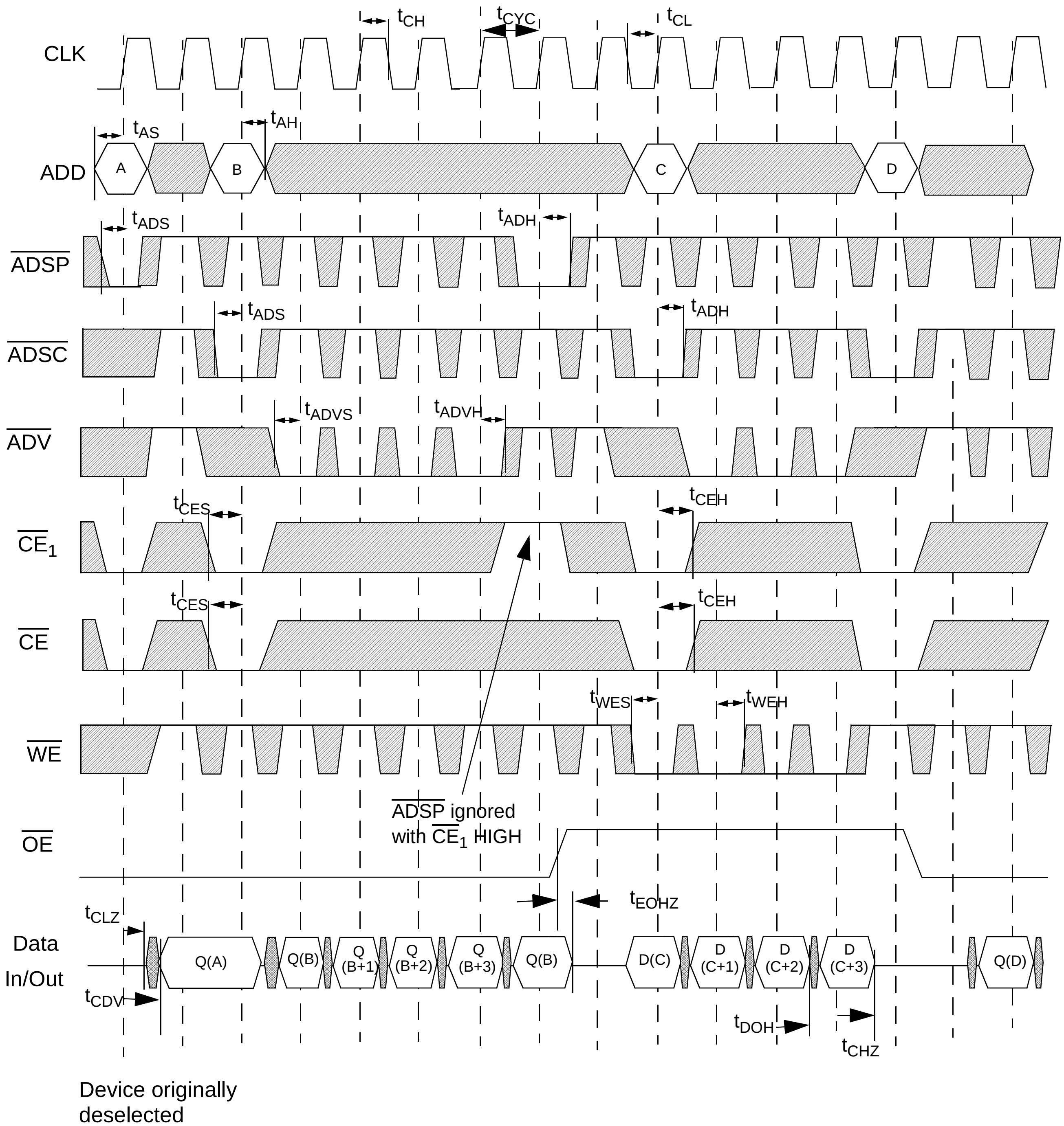


Note:

17. RDx stands for Read Data from Address X.

Switching Waveforms (continued)

Read/Write Cycle Timing[15, 16, 17]

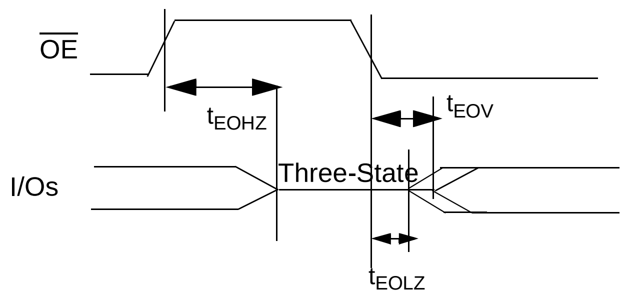


WE is the combination of BWE, BWx, and GW to define a write cycle (see Write Cycle Description table).
CE is the combination of CE_2 and $\overline{CE}_3$. All chip selects need to be active in order to select the device. RAx stands for Read Address X, WAx stands for Write Address X, Dx stands for Data-in X, Qx stands for Data-out X.

= DON'T CARE = UNDEFINED

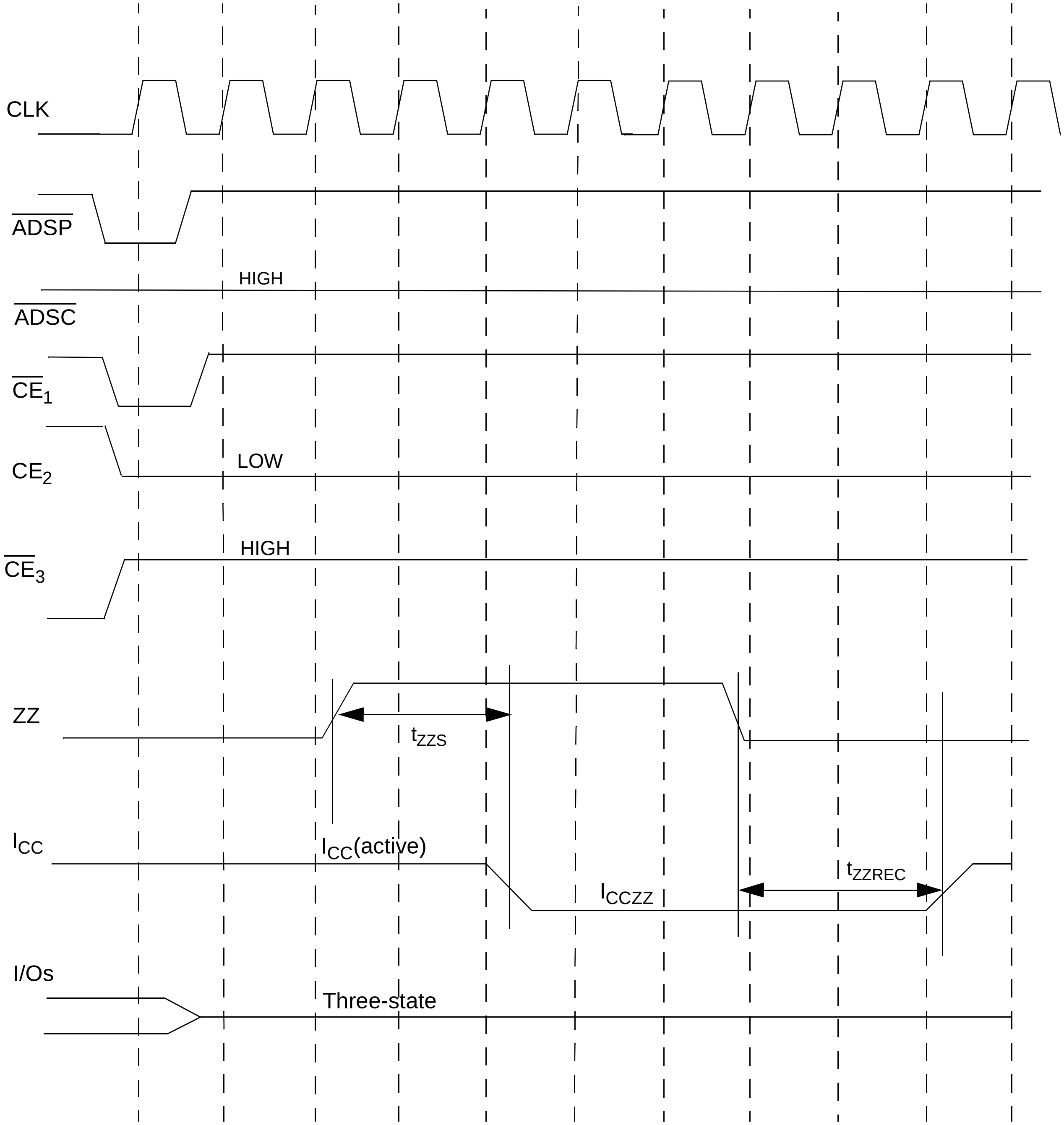
Switching Waveforms (continued)

OE Switching Waveforms



Switching Waveforms (continued)

ZZ Mode Timing [18]



Note:
18. I/Os are in three-state when exiting ZZ sleep mode.

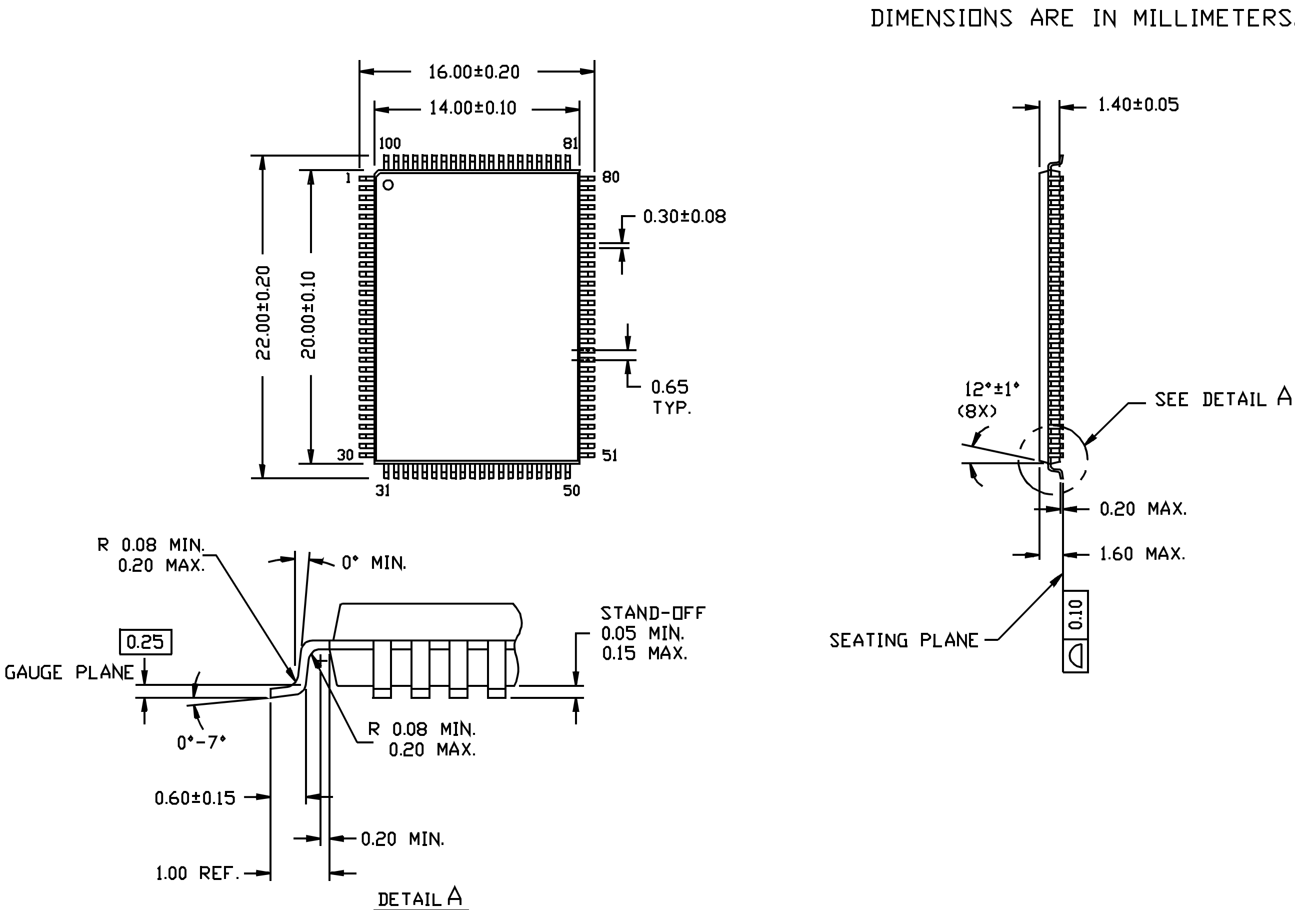
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CY7C1381CV25-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1381CV25-117AC			
100	CY7C1381CV25-100AC			
133	CY7C1383CV25-133AC			
117	CY7C1383CV25-117AC			
100	CY7C1383CV25-100AC			
133	CY7C1381CV25-133BGC	BG119	119 Ball BGA	
117	CY7C1381CV25-117BGC			
100	CY7C1381CV25-100BGC			
133	CY7C1383CV25-133BGC			
117	CY7C1383CV25-117BGC			
100	CY7C1383CV25-100BGC			
133	CY7C1381CV25-133BZC	BB165A	165 FBGA	
117	CY7C1381CV25-117BZC			
100	CY7C1381CV25-100BZC			
133	CY7C1383CV25-133BZC			
117	CY7C1383CV25-117BZC			
100	CY7C1383CV25-100BZC			
117	CY7C1381CV25-117AI	A101	100-Lead Thin Quad Flat Pack	Industrial
100	CY7C1381CV25-100AI			
117	CY7C1383CV25-117AI			
100	CY7C1383CV25-100AI			
117	CY7C1381CV25-117BGI	BG119	119 Ball BGA	
100	CY7C1381CV25-100BGI			
117	CY7C1383CV25-117BGI			
100	CY7C1383CV25-100BGI			
117	CY7C1381CV25-117BZI	BB165A	165 Ball FBGA	
100	CY7C1381CV25-100BZI			
117	CY7C1383CV25-117BZI			
100	CY7C1383CV25-100BZI			

Shaded areas contain advance information or parts may not be offered.

Package Diagrams

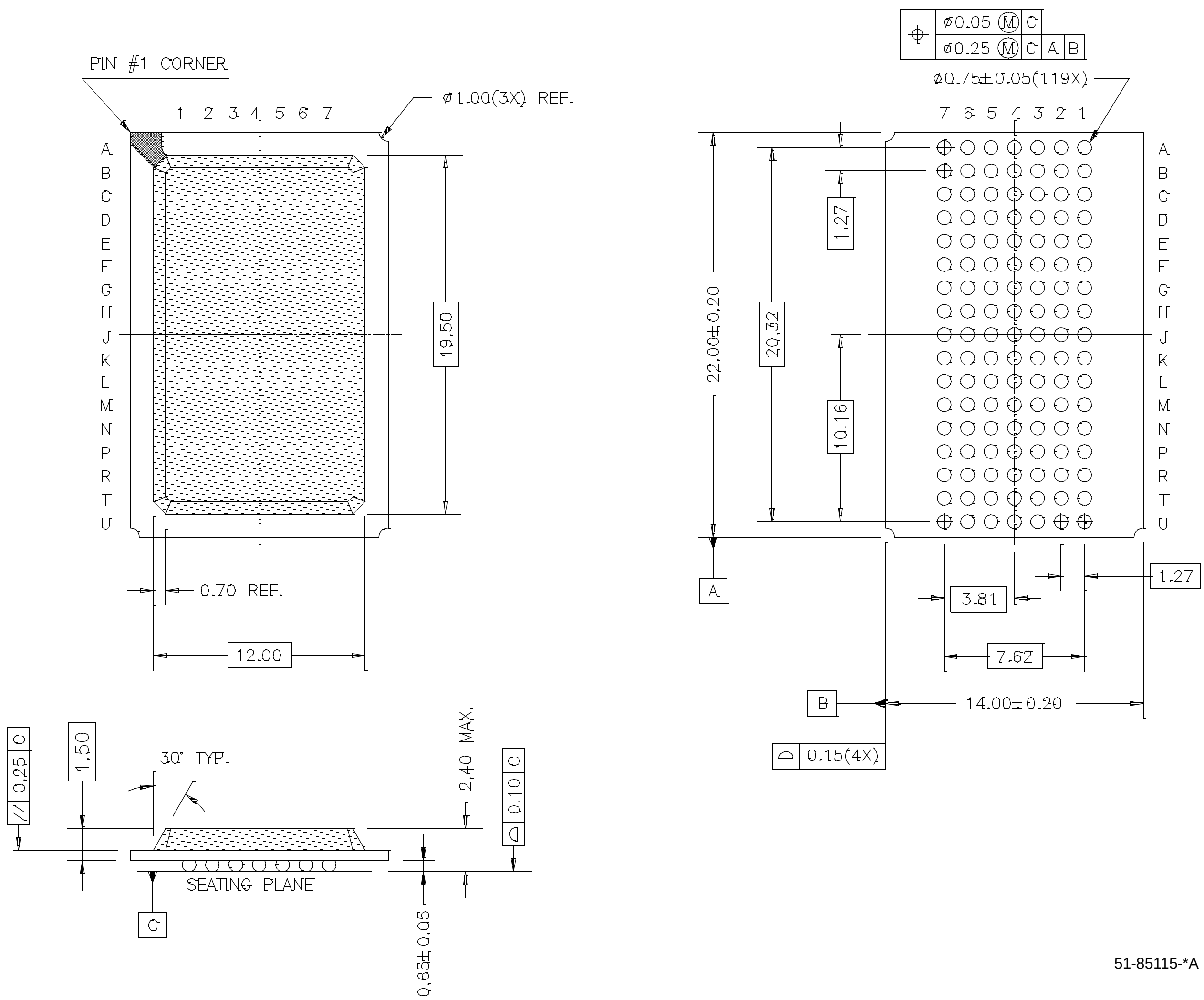
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



51-85050-A

Package Diagrams (continued)

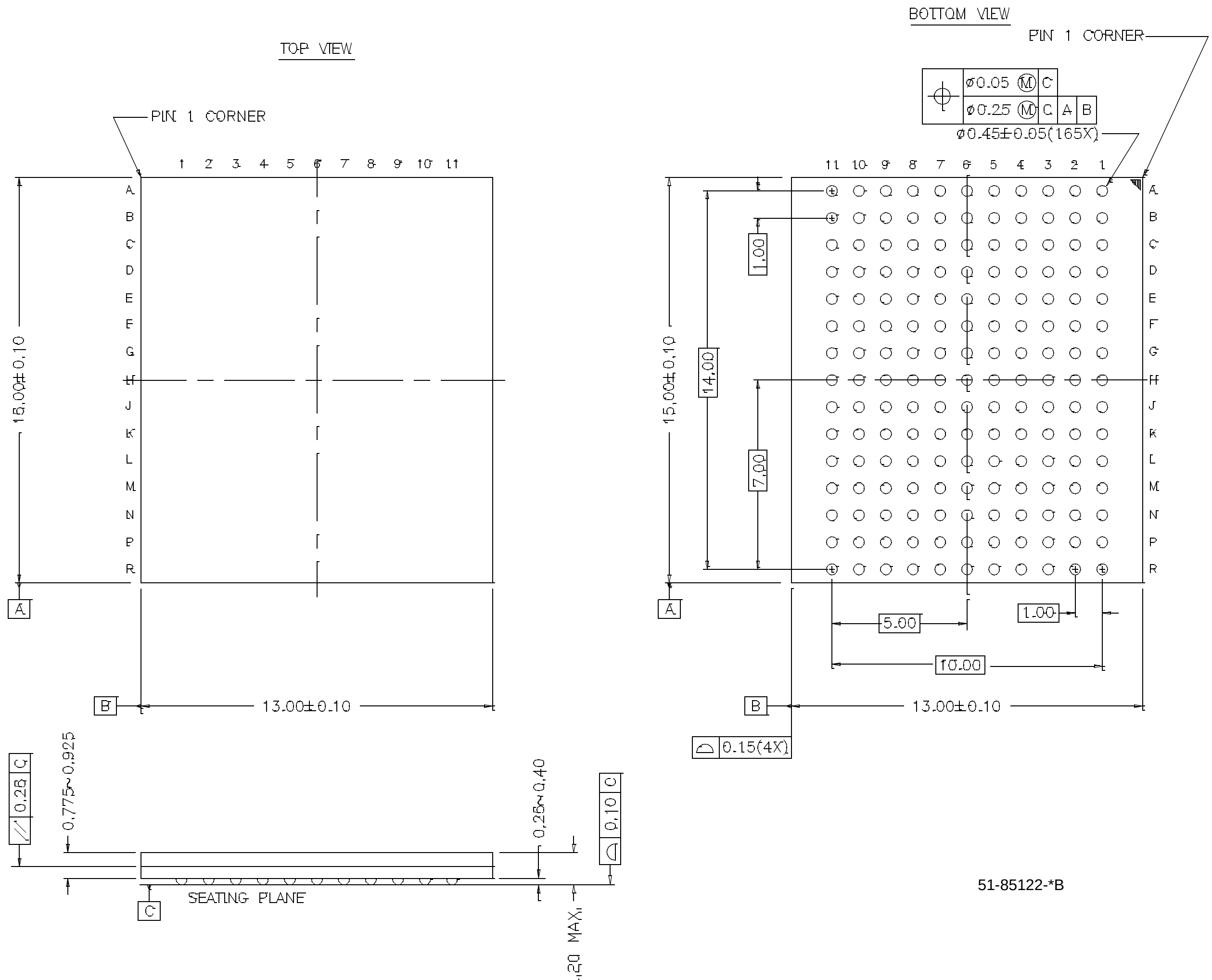
119-Lead BGA (14 x 22 x 2.4) BG119



51-85115-*A

Package Diagrams (continued)

165-Ball FBGA (13 x 15 x 1.2 mm) BB165A



51-85122-*B

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Document History Page

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REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	116281	8/28/2002	SKX	New Data Sheet