

CYPRESS
SEMICONDUCTOR

T-46-23-03

CY7C148

CY7C149

1024 x 4 Static RAM

Features

- Automatic power-down when deselected (7C148)
- CMOS for optimum speed/power
- 25-ns access time
- Low active power
 - 440 mW (commercial)
 - 605 mW (military)
- Low standby power (7C148)
 - 82.5 mW (25-ns version)
 - 55 mW (all others)
- 5-volt power supply $\pm 10\%$ tolerance, both commercial and military
- TTL-compatible inputs and outputs

Functional Description

The CY7C148 and CY7C149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the

memory locations specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

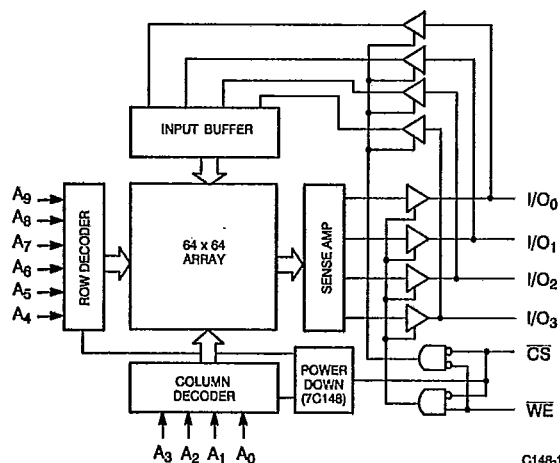
The I/O pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.



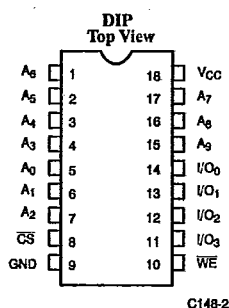
SRAMS

Logic Block Diagram

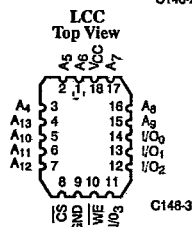
Pin Configurations



C148-1



C148-2



C148-3

Selection Guide

		7C148-25	7C148-35	7C148-45	7C149-25	7C149-35	7C149-45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	7C148/9-25		7C148/9-35,45		Units
			Min.	Max.	Min.	Max.	
I _{OH}	Output High Current	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
I _{OL}	Output Low Current	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input High Voltage		2.0	6.0	2.0	6.0	V
V _{IL}	Input Low Voltage		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	10	-10	10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-50	50	-50	50	μA
I _{CC}	V _{CC} Operating Supply Current	Max. V _{CC} , CS ≤ V _{IL} , Output Open	Com'l	90		80	mA
			Mil			110	
I _{SB}	Automatic CS Power-Down Current	Max. V _{CC} , CS ≥ V _{IH}	7C148 only	15		10	mA
			Mil			10	
I _{PO}	Peak Power-On Current ^[3]	Max. V _{CC} , CS ≥ V _{IH}	7C148 only	15		10	mA
			Mil			10	
I _{OS}	Output Short Circuit Current ^[4]	GND ≤ V _O ≤ V _{CC}	Com'l	±275		±275	mA
			Mil			±350	

Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	8	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
4. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

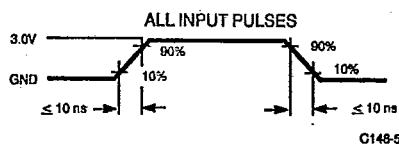
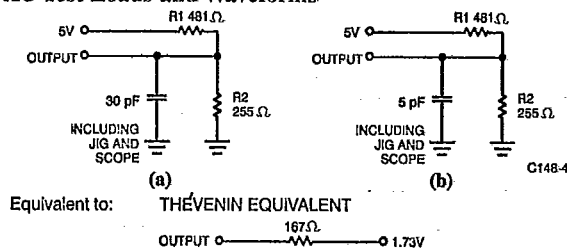


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AC Test Loads and Waveforms



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Switching Characteristics Over the Operating Range^[2]

Parameters	Description	7C148-25 7C149-25		7C148-35 7C149-35		7C148-45 7C149-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	25		35		45		ns
t _{AA}	Address Valid to Data Out Valid Delay (Address Access Time)		25		35		45	ns
t _{ACS1} t _{ACS2}	Chip Select LOW to Data Out Valid (7C148only)		25 ^[6]		35		45	ns
			30 ^[7]		35		45	ns
t _{ACS}	Chip Select LOW to Data Out Valid (7C149 only)		15		15		20	ns
t _{LZ} ^[8]	Chip Select LOW to Data Out On	7C148	8	10		10		ns
		7C149	5	5		5		
t _{HZ} ^[8]	Chip Select HIGH to Data Out Off	0	15	0	20	0	20	ns
t _{OH}	Address Unknown to Data Out Unknown Time	0		0		5		ns
t _{PD}	Chip Select HIGH to Power-Down Delay	7C148	20		30		30	ns
t _{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0	ns
WRITE CYCLE								
t _{WC}	Address Valid to Address Do Not Care (Write Cycle Time)	25		35		45		ns
t _{WP} ^[9]	Write Enable LOW to Write Enable HIGH	20		30		35		ns
t _{WR}	Address Hold from Write End	5		5		5		ns
t _{WZ} ^[8]	Write Enable to Output in High Z	0	8	0	8	0	8	ns
t _{DW}	Data in Valid to Write Enable HIGH	12		20		20		ns
t _{DH}	Data Hold Time	0		0		0		ns
t _{AS}	Address Valid to Write Enable LOW	0		0		0		ns
t _{CW} ^[9]	Chip Select LOW to Write Enable HIGH	20		30		40		ns
t _{OW} ^[8]	Write Enable HIGH to Output in Low Z	0		0		0		ns
t _{AW}	Address Valid to End of Write	20		30		35		

Notes:

- Chip deselected greater than 25 ns prior to selection.
- Chip deselected less than 25 ns prior to selection.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

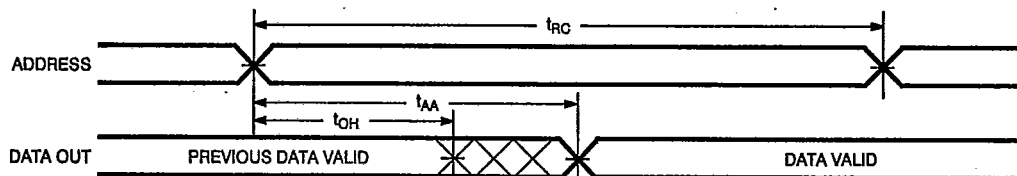


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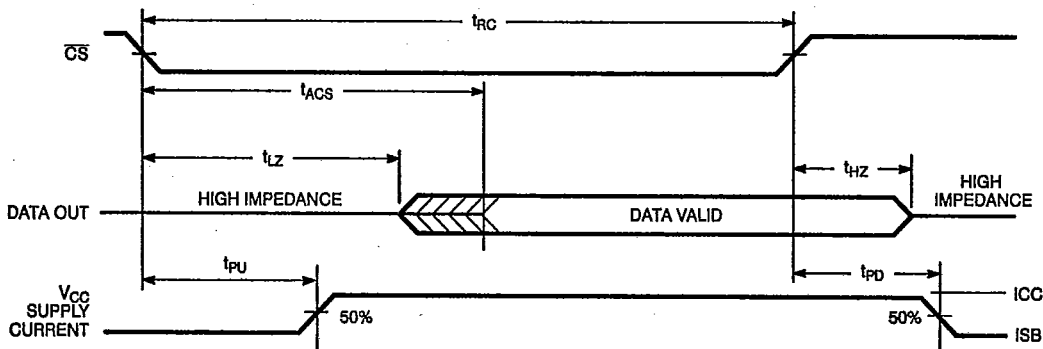
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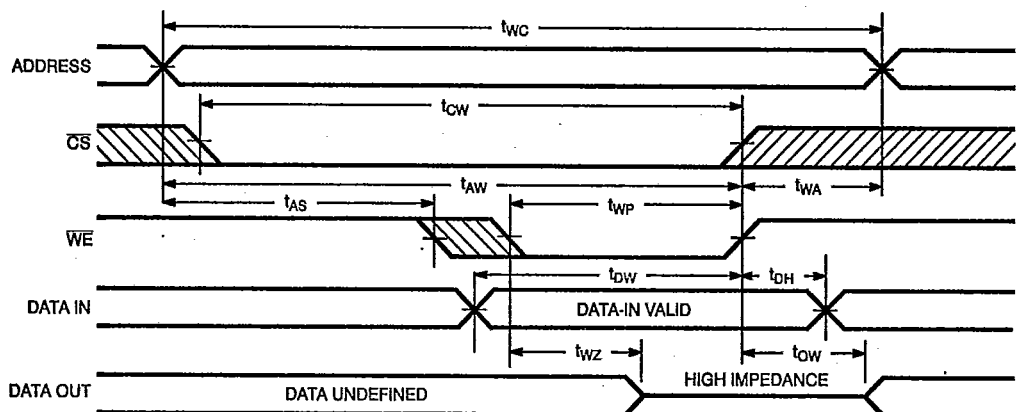
Switching Waveforms

Read Cycle No. 1^[10, 11]

G148-6

Read Cycle No. 2^[10, 12]

G148-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)

G148-8

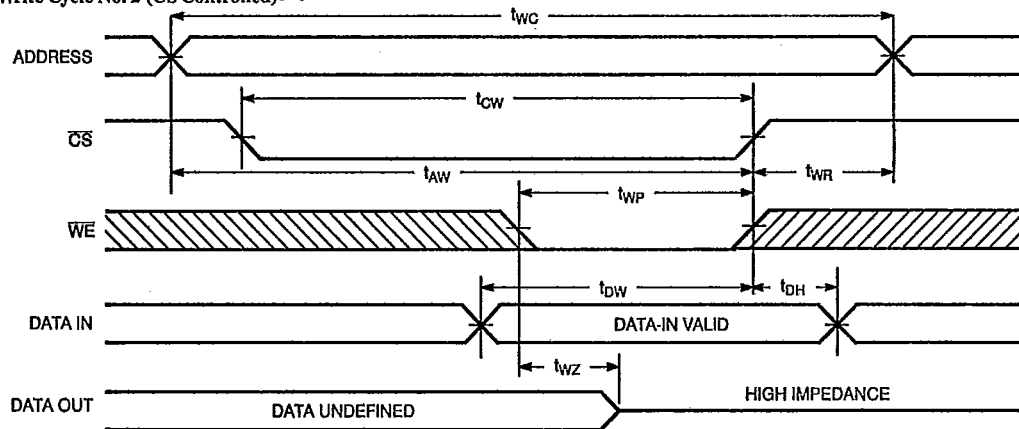
Notes:

10. $\overline{WE}$ is HIGH for read cycle.
 11. Device is continuously selected, $\overline{CS} = V_{IL}$.

12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.



Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)^[13]

C148-9

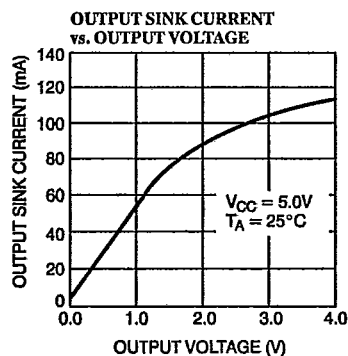
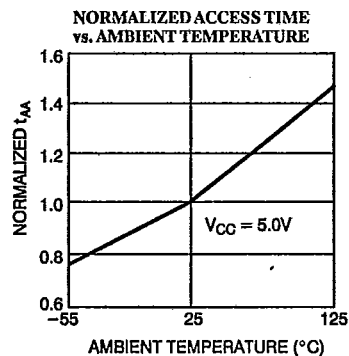
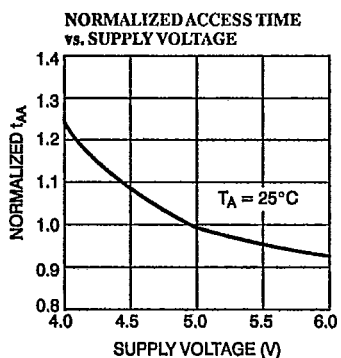
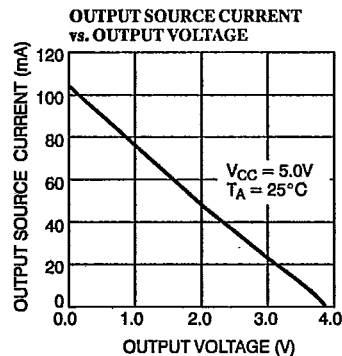
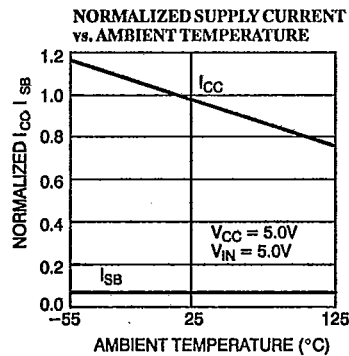
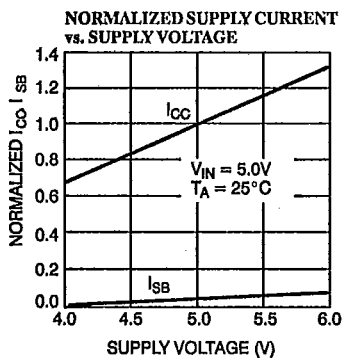


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Notes:

13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



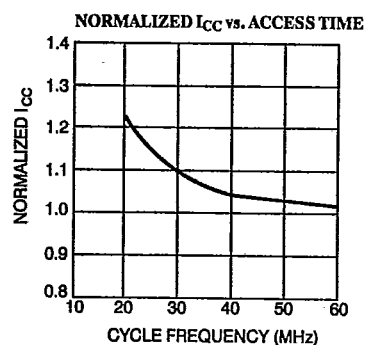
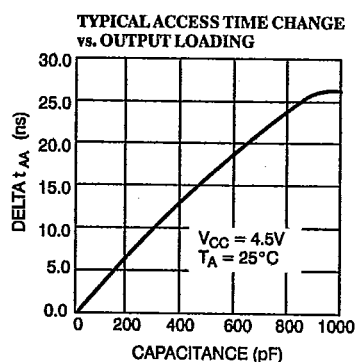
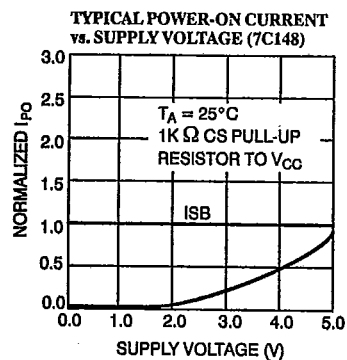


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Typical DC and AC Characteristics



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C148-25PC	P3	Commercial
	CY7C148-25DC	D4	
	CY7C148-25LC	L50	
35	CY7C148-35PC	P3	Commercial
	CY7C148-35DC	D4	
	CY7C148-35LC	L50	
	CY7C148-35DMB	D4	Military
	CY7C148-35KMB	K70	
	CY7C148-35LMB	L50	
45	CY7C148-45PC	P3	Commercial
	CY7C148-45DC	D4	
	CY7C148-45LC	L50	
	CY7C148-45DMB	D4	Military
	CY7C148-45KMB	K70	
	CY7C148-45LMB	L50	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C149-25PC	P3	Commercial
	CY7C149-25DC	D4	
	CY7C149-25LC	L50	
35	CY7C149-35PC	P3	Commercial
	CY7C149-35DC	D4	
	CY7C149-35LC	L50	
	CY7C149-35DMB	D4	Military
	CY7C149-35KMB	K70	
	CY7C149-35LMB	L50	
45	CY7C149-45PC	P3	Commercial
	CY7C149-45DC	D4	
	CY7C149-45LC	L50	
	CY7C149-45DMB	D4	Military
	CY7C149-45KMB	K70	
	CY7C149-45LMB	L50	



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MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
I _{OH}	1, 2, 3
I _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB} ^[14]	1, 2, 3

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Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{ACS1} ^[14]	7, 8, 9, 10, 11
t _{ACS2} ^[14]	7, 8, 9, 10, 11
t _{ACS} ^[15]	7, 8, 9, 10, 11
t _{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{WP}	7, 8, 9, 10, 11
t _{WR}	7, 8, 9, 10, 11
t _{DW}	7, 8, 9, 10, 11
t _{DH}	7, 8, 9, 10, 11
t _{AS}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11

Notes:

14. 7C148 only.

15. 7C149 only.



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