



CYPRESS
SEMICONDUCTOR

CY7C157A

16,384 x 16 Static R/W Cache Storage Unit

2

SRAMS

Features

- Optimized for use with RISC processors, including SPARC®
- Address and WE registers
- CMOS for optimum speed/power
- High speed
— 18 ns
- Data-in and Data-out latches
- Self-timed write
- Common I/O
- TTL-compatible inputs and outputs

Functional Description

The CY7C157A cache storage unit is a high-performance CMOS static RAM organized as 16,384 x 16 bits. It is optimized for use as a high-speed cache memory device with RISC processors such as the CY7C600 SPARC® family of devices. The CY7C157A employs common I/O architecture, a self-timed byte write mechanism, and on-chip address update latches.

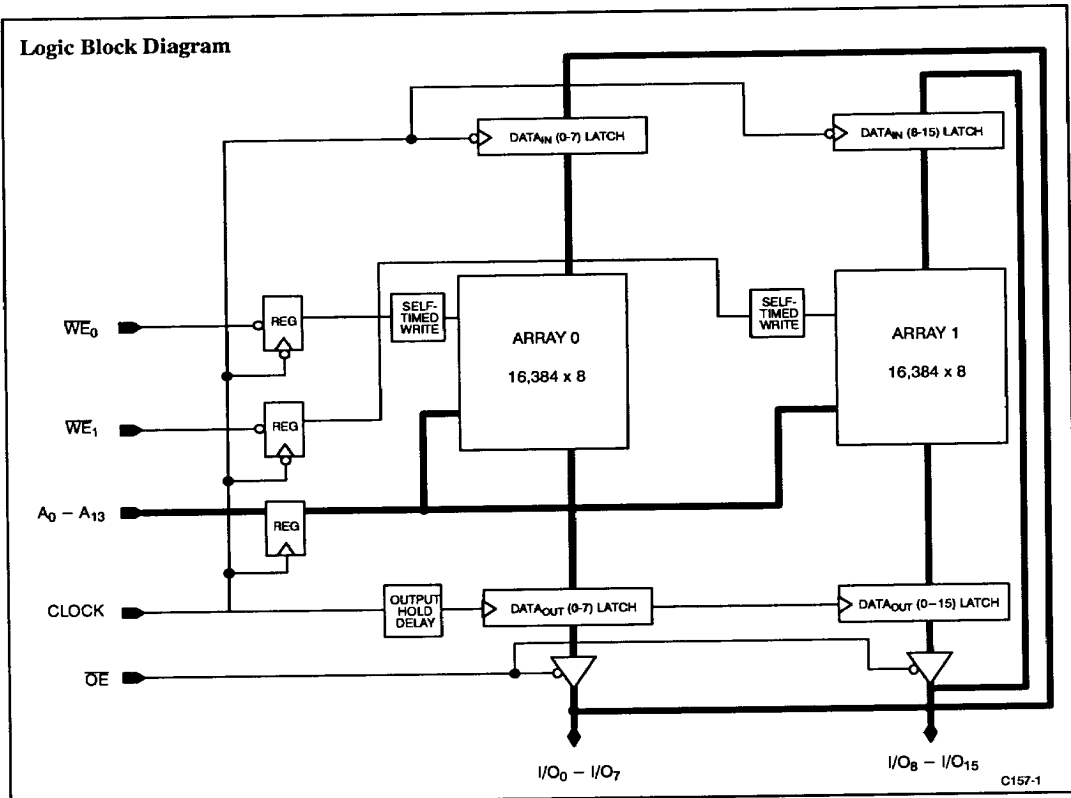
Reading the device is accomplished by taking WE HIGH and OE LOW. On the rising edge of CLOCK, addresses A₀ through A₁₃ are loaded into the input reg-

isters. A memory access occurs, and data is held after a read cycle beyond the next rising edge of CLOCK in order to meet the hold-time requirements of the microprocessor.

To write the device correctly, OE must be taken HIGH. If the falling edge of CLOCK samples either or both of WE₀ or WE₁ LOW, a self-timed byte write mechanism is triggered. Data is written from the data-in latch into the memory array at the corresponding address.

Note that the OE signal must be HIGH for a proper write because the WE₀ and WE₁ signals do not three-state the outputs.

Logic Block Diagram

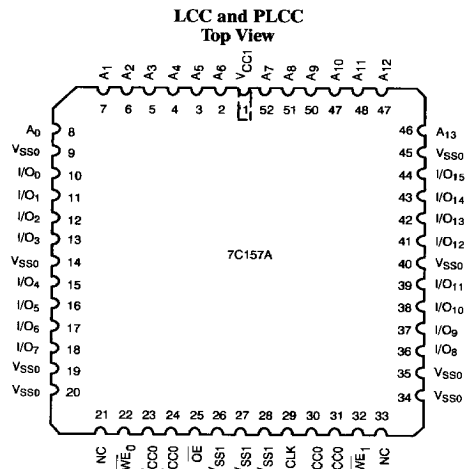


SPARC is a registered trademark of SPARC International, Inc.

Pin Timing Cross Reference

Pin Name	Timing Reference	Description
Clock	C	Clock Inputs
A ₀ – A ₁₃	A	Address Inputs
I/O ₀ – I/O ₁₅ (Input)	D	Data Inputs
I/O ₀ – I/O ₁₅ (Output)	Q	Data Outputs
WE ₀ , WE ₁ , WE _X	W	Write Enable
OE	G	Output Enable

Pin Diagram



C157-2

Selection Guide

		7C157A-18	7C157A-20	7C157A-24	7C157A-33
Maximum Clock to Output (ns)	Commercial	18	20	24	33
	Military			24	33
Maximum Output Enable to Output Time (ns)	Commercial	7	8	10	15
	Military			10	15
Maximum Current (mA)	Commercial	350	325	300	250
	Military			325	275

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage ^[1]	-0.5V to +7.0V
Output Current into Outputs (LOW)	50 mA

Notes:

1. V_{IL} (min.) = -3.0V for pulse durations of less than 20 ns.

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

2. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C157A-18		7C157A-20		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		- 0.3	0.8	- 0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+ 10	- 10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+ 10	- 10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	350		325	mA
			Mil				

Parameters	Description	Test Conditions	7C157A-24		7C157A-33		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[1]		- 0.3	0.8	- 0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+ 10	- 10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+ 10	- 10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	300		250	mA
			Mil	325		275	

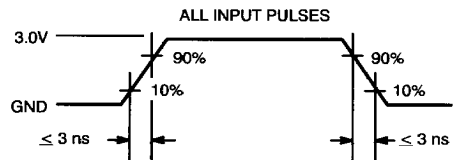
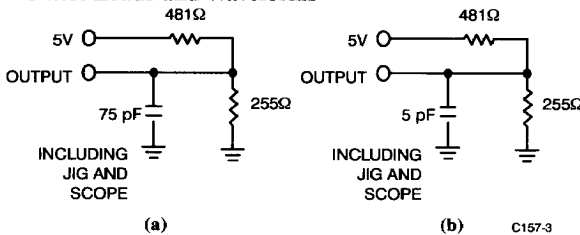
Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		8	pF

Notes:

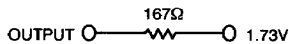
- See the last page of this specification for Group A subgroup testing information.
- Tested initially and after any design or process changes that may affect these parameters.
- Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.

AC Test Loads and Waveforms



C157-4

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[6]

Parameters	Description	7C157A-18		7C157A-20		7C157A-24		7C157A-33		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE ^[7,8]										
t _{CHCH}	Clock Cycle Time	22		25		30		40		ns
t _{CH}	Clock HIGH Time	10		11		13		18		ns
t _{CL}	Clock LOW Time	10		11		13		18		ns
t _{CHOV}	Clock HIGH to Output Valid		18		20		24		33	ns
t _{CHOX}	Output Data Hold	5		5		5		5		ns
t _{WHCH}	$\overline{WE}_x$ HIGH to Next Clock HIGH	2		2		2		3		ns
t _{GLQV}	$\overline{OE}$ LOW to Output Valid		7		8		10		15	ns
t _{GHQZ}	$\overline{OE}$ HIGH to Output Tristate ^[9]		7		8		10		15	ns
t _{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		7		ns
t _{AVCH}	Address Set-Up	2		2		2		3		ns
t _{CHAX}	Address Hold	5		6		6		6		ns
WRITE CYCLE ^[10]										
t _{CHCH}	Clock Cycle Time ^[11]	22		25		30		40		ns
t _{CH}	Clock HIGH Time	10		11		13		18		ns
t _{CL}	Clock LOW Time	10		11		13		18		ns
t _{GHQZ}	$\overline{OE}$ HIGH to Output Tristate ^[9]		7		8		10		15	ns
t _{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		7		ns
t _{DVCL}	Data in Set-Up to Clock	5		6		6		7		ns
t _{CLDX}	Data in Hold from Clock	2		2		2		2		ns
t _{WLCL}	$\overline{WE}_x$ LOW to Clock LOW ^[12,13]	2		2		2		3		ns
t _{CLWH}	Clock LOW to $\overline{WE}_x$ HIGH ^[12,13]	4		6		6		7		ns
t _{AVCH}	Address Set-Up	2		2		2		3		ns
t _{CHAX}	Address Hold	5		6		6		6		ns



Truth Table

OE	WE ₀	WE ₁	Operation	Inputs/Outputs
L	L	L	Invalid	Invalid
L	L	H	Invalid	Invalid
L	H	L	Invalid	Invalid
L	H	H	Read	Data Out (I/O ₀ – I/O ₁₅)
H	L	L	Write	Data In (I/O ₀ – I/O ₁₅)
H	L	H	Low Byte Write	Data In (I/O ₀ – I/O ₇)
H	H	L	High Byte Write	Data In (I/O ₈ – I/O ₁₅)
H	H	H	Disabled	High Z

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
18	CY7C157A-18LC	L69	Commercial
	CY7C157A-18JC	J69	
20	CY7C157A-20LC	L69	Commercial
	CY7C157A-20JC	J69	
24	CY7C157A-24LC	L69	Commercial
	CY7C157A-24JC	J69	
	CY7C157A-24LMB	L69	Military
	CY7C157A-24YMB	Y59	
33	CY7C157A-33LC	L69	Commercial
	CY7C157A-33JC	J69	
	CY7C157A-33LMB	L69	Military
	CY7C157A-33YMB	Y59	

MILITARY SPECIFICATIONS Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{CHCH}	7, 8, 9, 10, 11
t _{CHQV}	7, 8, 9, 10, 11
t _{GHQZ}	7, 8, 9, 10, 11
t _{CHOX}	7, 8, 9, 10, 11
t _{GHQV}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{CHCH}	7, 8, 9, 10, 11
t _{DPVCL}	7, 8, 9, 10, 11
t _{AVCH}	7, 8, 9, 10, 11
t _{CHAX}	7, 8, 9, 10, 11
t _{CLDX}	7, 8, 9, 10, 11
t _{DPWL}	7, 8, 9, 10, 11
t _{WLDX}	7, 8, 9, 10, 11

Document #: 38-R-10007-C