



CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM
Separate I/O

CY7C161
CY7C162

Features

- Automatic power-down when deselected
- Transparent write (7C161)
- CMOS for optimum speed/power
- High speed
 - 15 ns t_{AA}
- Low active power
 - 633 mW
- Low standby power
 - 220 mW
- TTL compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge.

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$) and write enable ($\overline{\text{WE}}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written

into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

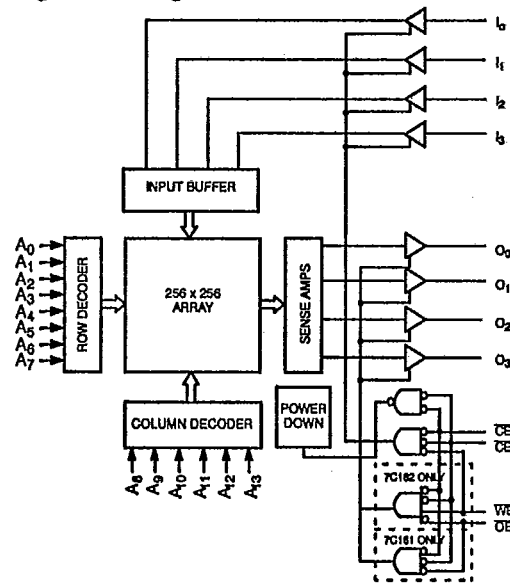
The output pins stay in high-impedance state when write enable (**WE**) is LOW (7C162 only), or one of the chip enables (**CE₁**, **CE₂**) are HIGH.

A die coat is used to insure alpha immunity.

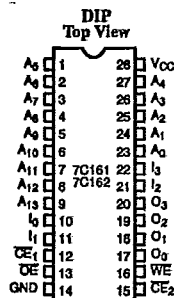


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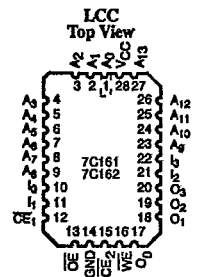
Logic Block Diagram



Pin Configurations



C162-2



6162-3

Selection Guide^[1]

	7C161--10 7C162--10	7C161--12 7C162--12	7C161--15 7C162--15	7C161--20 7C162--20	7C161--25 7C162--25	7C161--35 7C162--35	7C161--45 7C162--45
Maximum Access Time (ns)	10	12	15	20	25	35	45
Maximum Operating Current (mA)	160	160	115	80	70	70	50
Maximum Standby Current (mA)	40/20	40/20	40/20	40/20	20/20	20/20	20/20

Shaded areas indicate advanced information.

Note:

1. For military specifications, see the CY7C161A/CY7C162A datasheet.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with
Power Applied - 55°C to +125°CSupply Voltage to Ground Potential
(Pin 24 to Pin 12) - 0.5V to +7.0VDC Voltage Applied to Outputs
in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.0V to + 7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C161-10 7C162-10		7C161-12 7C162-12		7C161-15 7C162-15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		- 0.5	0.8	- 0.5	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		160		160		115	mA
I _{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		40	mA
I _{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

Shaded areas indicate advanced information.



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Electrical Characteristics Over the Operating Range(continued)

Parameters	Description	Test Conditions	7C161-20 7C162-20		7C161-25,35 7C162-25,35		7C161-45 7C162-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		80		70		50	mA
I _{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{IH} , Min. Duty Cycle = 100%		40		20		20	mA
I _{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA



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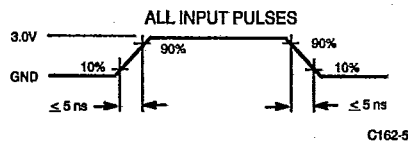
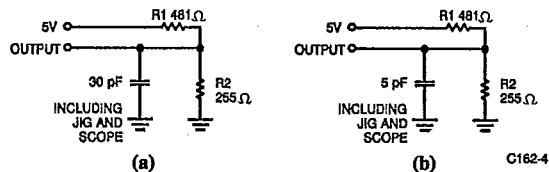
Capacitance^[4]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

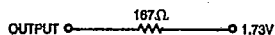
Notes:

- V_{IL} min. = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



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Switching Characteristics Over the Operating Range^[5, 6]

Parameters	Description	7C161-10 7C162-10		7C161-12 7C162-12		7C161-15 7C162-15		7C161-20 7C162-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	10		12		15		20		ns
t _{AA}	Address to Data Valid		10		12		15		20	ns
t _{OHA}	Output Hold from Address Change	3		3		3		5		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10		12		15		20	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		10		12		10		10	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0		0		3		3		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z		5		7		8		8	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[7]	2		3		3		5		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[7,8]		5		7		8		8	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE ^[9]										
t _{WC}	Write Cycle Time	10		12		15		20		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	8		8		12		15		ns
t _{AW}	Address Set-Up to Write End	8		8		12		15		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	8		8		12		15		ns
t _{SD}	Data Set-Up to Write End	5		6		10		10		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[7] (7C162)	2		3		5		5		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[7,8] (7C162)		6		6		7		7	ns
t _{AWE}	$\overline{\text{WE}}$ LOW to Data Valid (7C161)		10		12		15		20	ns
t _{ADV}	Data Valid to Output Valid (7C161)		10		12		15		20	ns
t _{DLE}	$\overline{\text{CE}}$ LOW to Data Valid		10		12		15		20	ns

Shaded areas indicate advanced information.



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Switching Characteristics Over the Operating Range^[5, 6]

Parameters	Description	7C161-25 7C162-25		7C161-35 7C162-35		7C161-45 7C162-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z		10		12		15	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7]	5		5		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[7,8]		10		15		15	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE ^[9]								
t _{WC}	Write Cycle Time	20		25		40		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	20		25		30		ns
t _{AW}	Address Set-Up to Write End	20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	15		20		20		ns
t _{SD}	Data Set-Up to Write End	10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[7] (7C162)	5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7,8] (7C162)		7		10		15	ns
t _{AWE}	$\overline{WE}$ LOW to Data Valid (7C161)		25		30		35	ns
t _{ADV}	Data Valid to Output Valid (7C161)		20		30		35	ns
t _{DLE}	$\overline{CE}$ LOW to Data Valid		25		30		35	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.

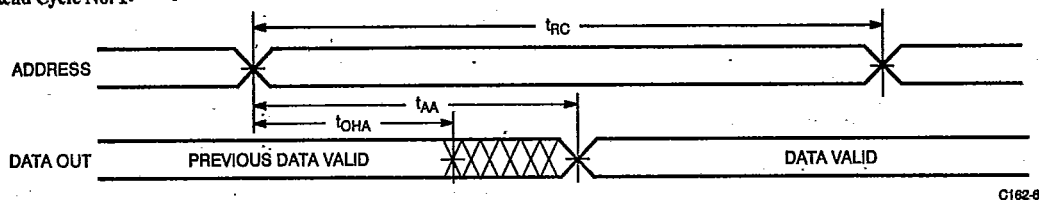
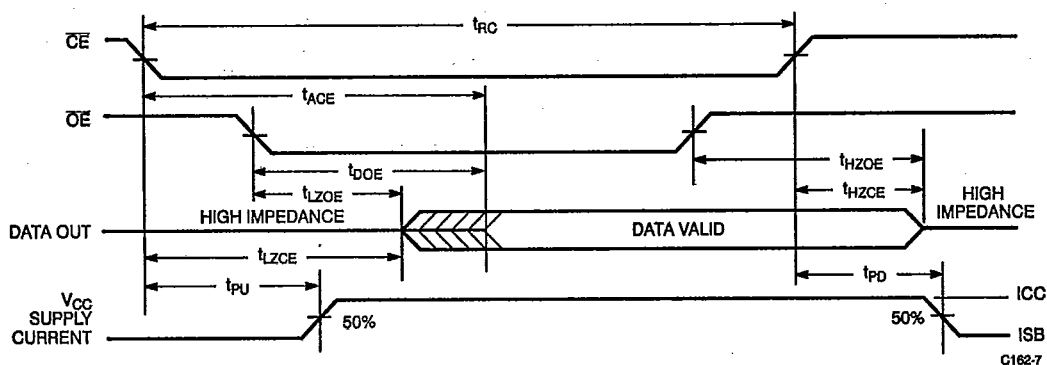
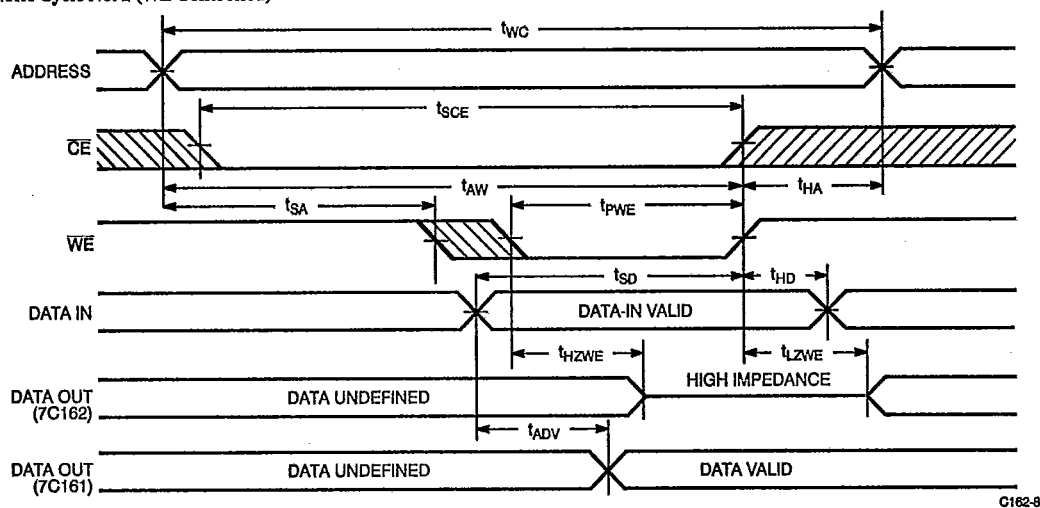
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



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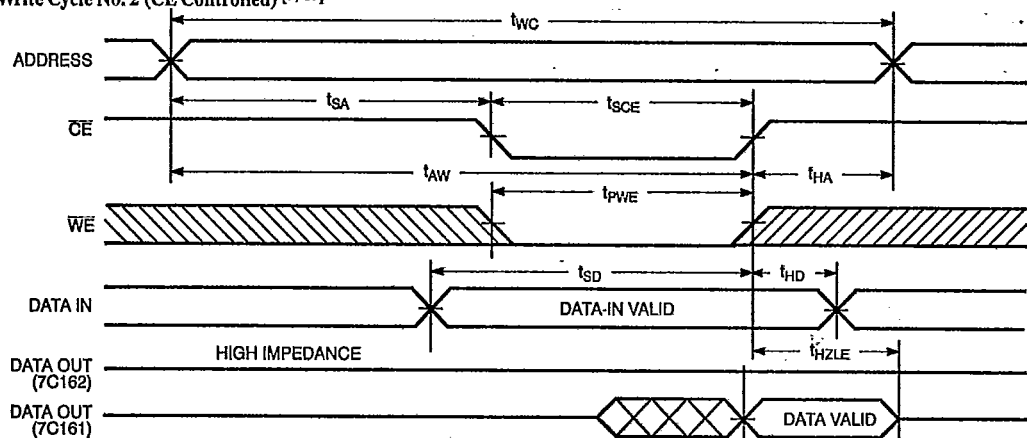
Switching Waveforms^[8]Read Cycle No. 1^[10, 11]Read Cycle No. 2^[10, 12]Write Cycle No. 1 ($\overline{WE}$ Controlled)^[9]

Notes:

10. $\overline{WE}$ is HIGH for read cycle.11. Device is continuously selected, $\overline{CE}_1, \overline{CE}_2 = V_{IL}$.12. Address valid prior to or coincident with $\overline{CE}_1, \overline{CE}_2$ transition LOW.

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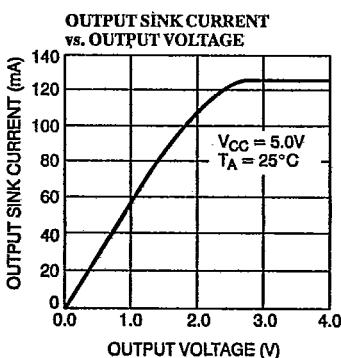
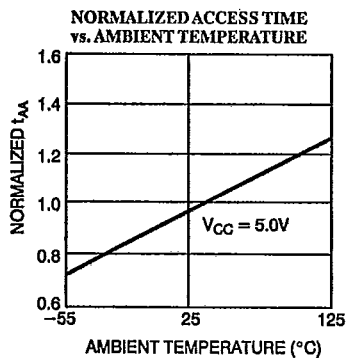
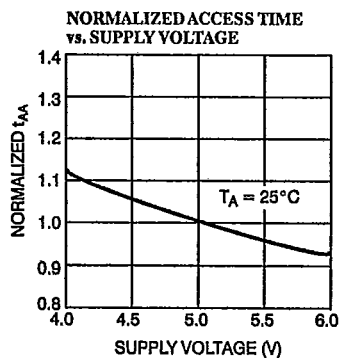
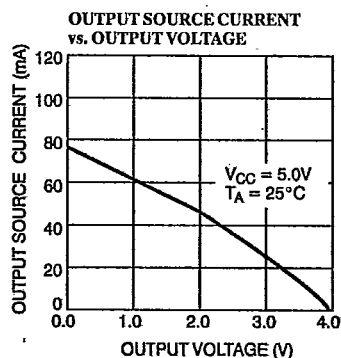
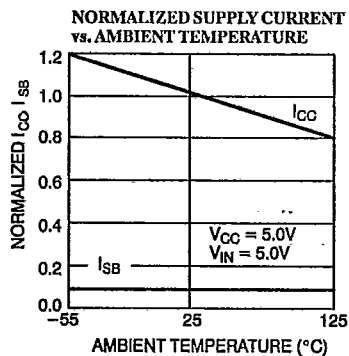
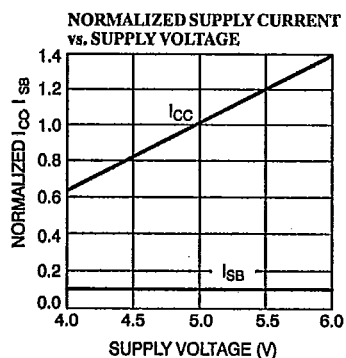
Switching Waveforms^[8] (continued)Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]

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Note:
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162 only).

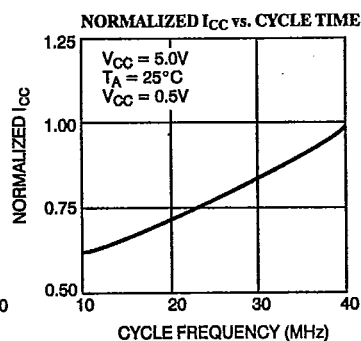
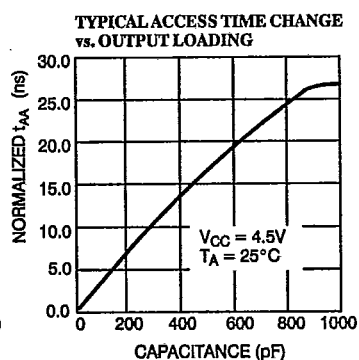
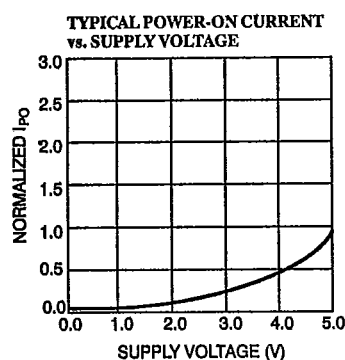
Typical DC and AC Characteristics





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Typical DC and AC Characteristics (continued)



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C161-10PC	P21	Commercial
	CY7C161-10VC	V21	
	CY7C161-10DC	D22	
	CY7C161-10LC	L54	
12	CY7C161-12PC	P21	Commercial
	CY7C161-12VC	V21	
	CY7C161-12DC	D22	
	CY7C161-12LC	L54	
15	CY7C161-15PC	P21	Commercial
	CY7C161-15VC	V21	
	CY7C161-15DC	D22	
	CY7C161-15LC	L54	
20	CY7C161-20PC	P21	Commercial
	CY7C161-20VC	V21	
	CY7C161-20DC	D22	
	CY7C161-20LC	L54	
25	CY7C161-25PC	P21	Commercial
	CY7C161-25VC	V21	
	CY7C161-25DC	D22	
	CY7C161-25LC	L54	
35	CY7C161-35PC	P21	Commercial
	CY7C161-35VC	V21	
	CY7C161-35DC	D22	
	CY7C161-35LC	L54	
45	CY7C161-45PC	P21	Commercial
	CY7C161-45VC	V21	
	CY7C161-45DC	D22	
	CY7C161-45LC	L54	

Shaded areas indicate advanced information.

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C162-10PC	P21	Commercial
	CY7C162-10VC	V21	
	CY7C162-10DC	D22	
	CY7C162-10LC	L54	
12	CY7C162-12PC	P21	Commercial
	CY7C162-12VC	V21	
	CY7C162-12DC	D22	
	CY7C162-12LC	L54	
15	CY7C162-15PC	P21	Commercial
	CY7C162-15VC	V21	
	CY7C162-15DC	D22	
	CY7C162-15LC	L54	
20	CY7C162-20PC	P21	Commercial
	CY7C162-20VC	V21	
	CY7C162-20DC	D22	
	CY7C162-20LC	L54	
25	CY7C162-25PC	P21	Commercial
	CY7C162-25VC	V21	
	CY7C162-25DC	D22	
	CY7C162-25LC	L54	
35	CY7C162-35PC	P21	Commercial
	CY7C162-35VC	V21	
	CY7C162-35DC	D22	
	CY7C162-35LC	L54	
45	CY7C162-45PC	P21	Commercial
	CY7C162-45VC	V21	
	CY7C162-45DC	D22	
	CY7C162-45LC	L54	

Shaded areas indicate advanced information.



SRAMs