



CYPRESS SEMICONDUCTOR

T-46-23-08

CY7C168A
CY7C169A

4096 x 4 R/W RAM

Features

- Automatic power—down when deselected (7C168A)
- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 15 \text{ ns}$
 - $t_{ACE} = 10 \text{ ns}$ (7C169A)
- Low active power
 - 385 mW
- Low standby power (7C168)
 - 83 mW
- TTL-compatible inputs and outputs
- V_{IH} of 2.2V

- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C168A and CY7C169A are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip select ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3)

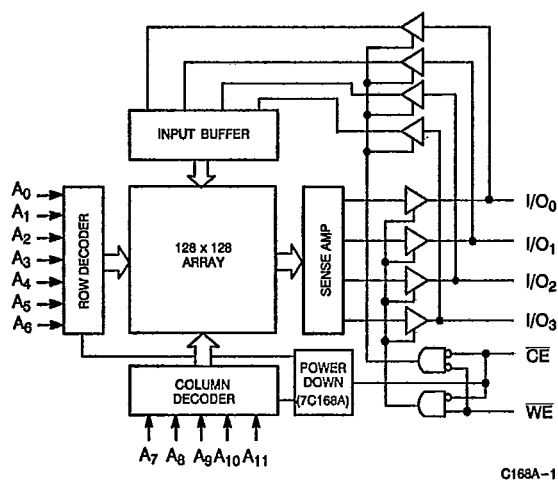
is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{\text{CE}}$) LOW, while ($\overline{\text{WE}}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable is HIGH or write enable ($\overline{WE}$) is LOW.

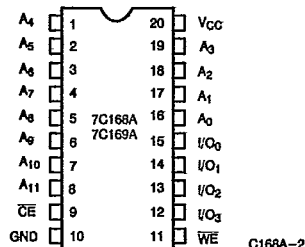
A die coat is used to insure alpha immunity.

Logic Block Diagram

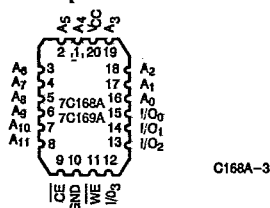


Pin Configurations

DIP/SOJ
Top View



LCC
Top View



Selection Guide

		7C168A-15 7C169A-15	7C168A-20 7C169A-20	7C168A-25 7C169A-25	7C168A-35 7C169A-35	7C169A-40	7C168A-45
Maximum Access Time (ns)		15	20	25	35	40	45
Maximum Operating Current (mA)	Commercial	115	90	70	70	50	50
	Military		90	80	70	70	70



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CY7C168A
CY7C169A**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V

Output Current into Outputs (Low)	20 mA
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	- 55°C to +125°C	5V ± 10%



SRAMS

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	7C168A-15 7C169A-15		7C168A-20 7C169A-20		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	115		90	mA
			Mil			90	
I _{SB1}	Automatic CS Power-Down Current	Max. V _{CC} , CE ≥ V _{IH}	Com'l	40		40	mA
			Mil			40	
I _{SB2}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{CC} - .0.3 V	Com'l	20		20	mA
			Mil			20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = -3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.



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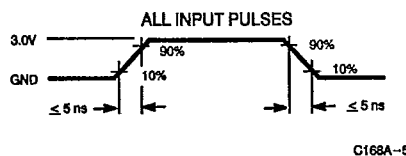
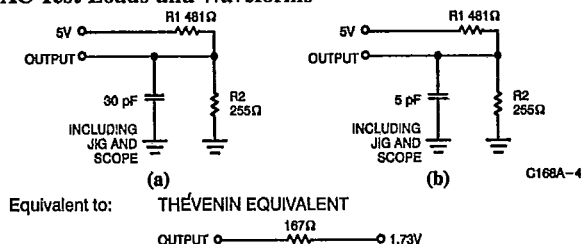
CY7C168A
CY7C169AElectrical Characteristics Over the Operating Range^[2] (continued)

Parameters	Description	Test Conditions	7C168A-25 7C169A-25		7C168A-35 7C169A-35		7C168A-45 7C169A-40		
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	10	-10	10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled	-10	+10	-50	50	-50	50	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	70		70		50	mA
			Mil	80		70		70	
I _{SB1}	Automatic $\overline{\text{CS}}$ Power-Down Current	Max. V _{CC} , CE ≥ V _{IH}	Com'l	20		20		20	mA
			Mil	20		20		20	
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-Down Current	Max. V _{CC} , CE ≥ V _{CC} - 0.3 V	Com'l	20		20		20	mA
			Mil	20		20		20	

Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.



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CY7C168A
CY7C169ASwitching Characteristics Over the Operating Range^[3, 6]

Parameters	Description		7C168A-15 7C169A-15		7C168A-20 7C169A-20		7C168A-25 7C169A-25		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t _{RC}	Read Cycle Time		15		20		25		ns
t _{AA}	Address to Data Valid			15		20		25	ns
t _{OHA}	Output Hold from Address Change		5		5		5		ns
t _{ACE}	Power Supply Current	7C168A		15		20		25	ns
		7C169A		10		12		15	ns
t _{LZCE}	CE LOW to Low Z ^[7, 8]		5		5		5		ns
t _{HZCE}	CE HIGH to High Z ^[7, 9]			8		8		10	ns
t _{PU}	CE LOW to Power Up (7C168)		0		0		0		ns
t _{PD}	CE HIGH to Power-Down (7C168)			15		20		20	ns
t _{RCS}	Read Command Set-Up		0		0		0		ns
t _{RCH}	Read Command Hold		0		0		0		ns
WRITE CYCLE ^[10]									
t _{WC}	Write Cycle Time		15		20		20		ns
t _{SCE}	CE LOW to Write End		12		15		20		ns
t _{AW}	Address Set-Up to Write End		12		15		20		ns
t _{HA}	Address Hold from Write End		0		0		0		ns
t _{SA}	Address Set-Up to Write Start		0		0		0		ns
t _{PWE}	WE Pulse Width		12		15		15		ns
t _{SD}	Data Set-Up to Write End		10		10		10		ns
t _{HD}	Data Hold from Write End		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[7]		7		7		7		ns
t _{HZWE}	WE LOW to High Z ^[7, 9]			5		5		5	ns



SRAMs

Notes:

- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ± 500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
- 3-ns minimum for the CY7C169A.
- t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{\text{WE}}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
- Address valid prior to or coincident with $\overline{\text{CE}}$ transition low.
- If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

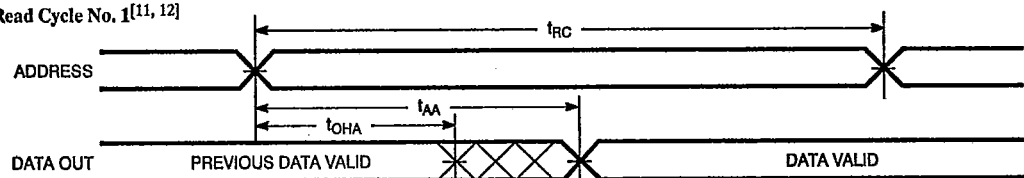
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CY7C168A
CY7C169ASwitching Characteristics Over the Operating Range^[3, 6] (continued)

Parameters	Description	7C168A-35 7C169A-35		7C169A-40		7C168A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		40		45		ns
t _{AA}	Address to Data Valid		35		40		45	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACE}	Power Supply Current	7C168A	35		40		45	ns
		7C169A	25		25			ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7, 8]	5		5		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[7, 9]		15		15		15	ns
t _{PU}	$\overline{CE}$ LOW to Power Up (7C168)	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)		20		20		25	ns
t _{RCS}	Read Command Set-Up	0		0		0		ns
t _{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE ^[10]								
t _{WC}	Write Cycle Time	25		35		40		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	25		30		30		ns
t _{AW}	Address Set-Up to Write End	25		30		30		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	20		20		20		ns
t _{SD}	Data Set-Up to Write End	15		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[7]	5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7, 9]		10		15		15	ns

Switching Waveforms

Read Cycle No. 1^[11, 12]

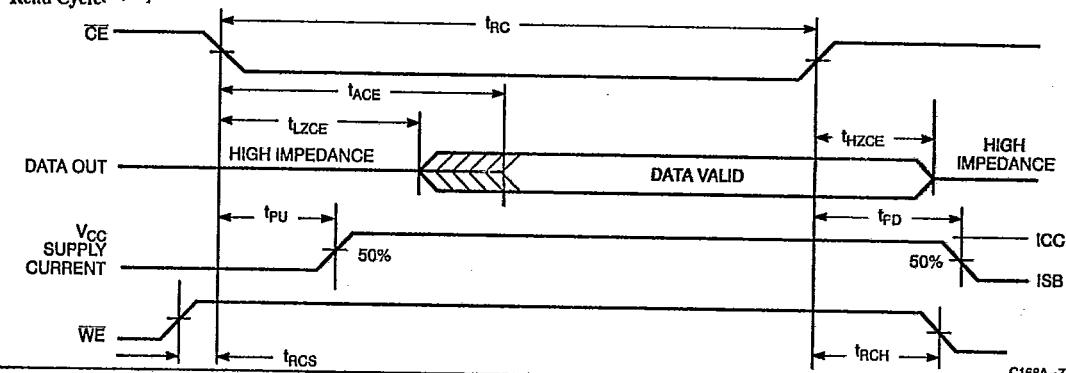
C168A-6



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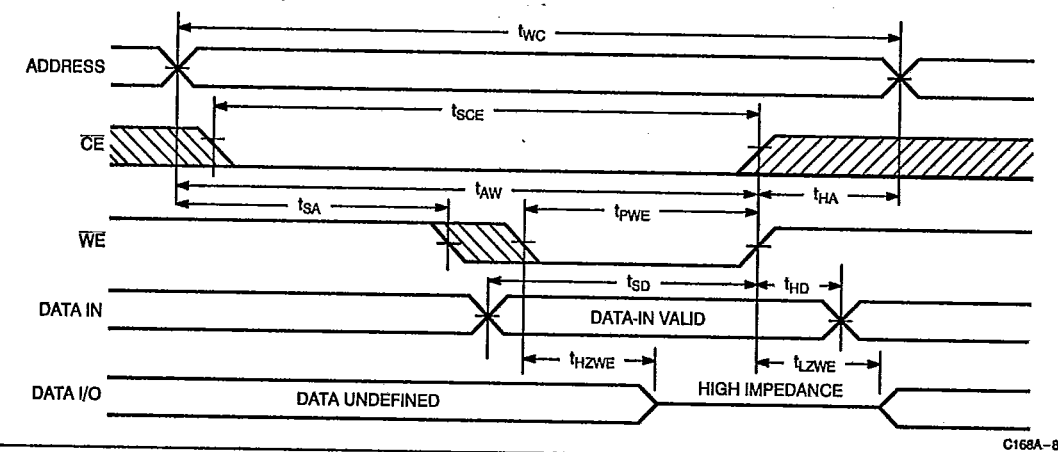
CY7C168A
CY7C169A

Switching Waveforms (continued)

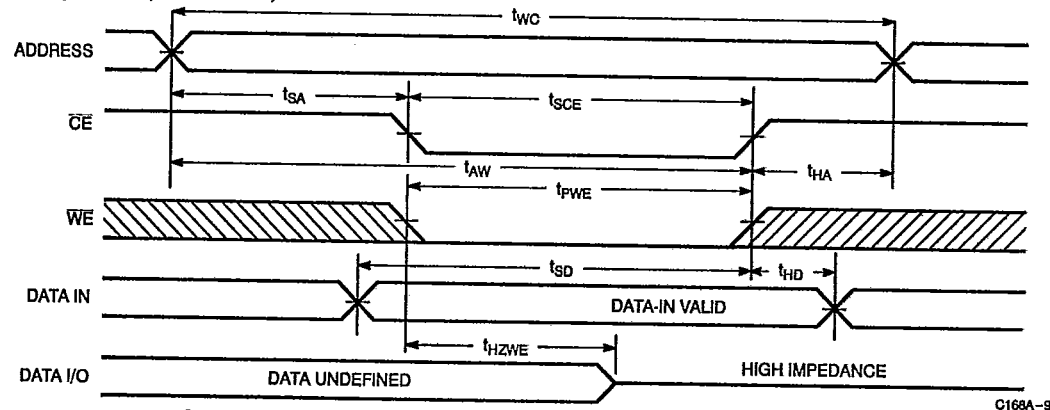
Read Cycle^[11, 13]

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C168A-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[10]

C168A-8

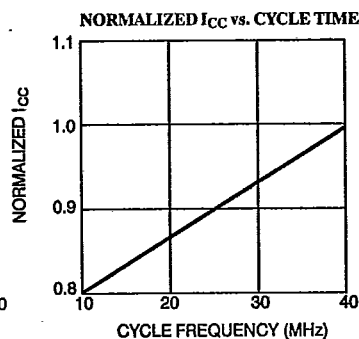
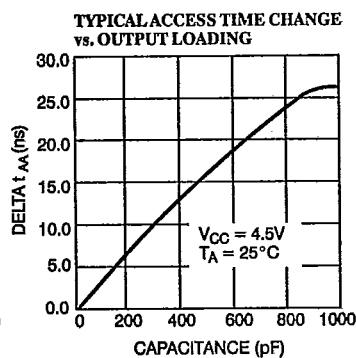
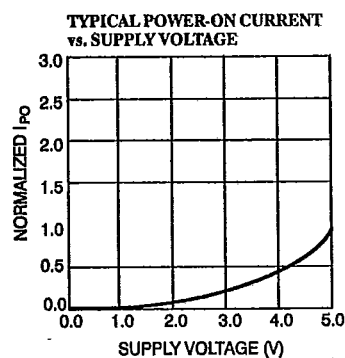
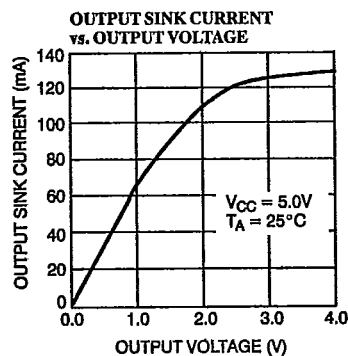
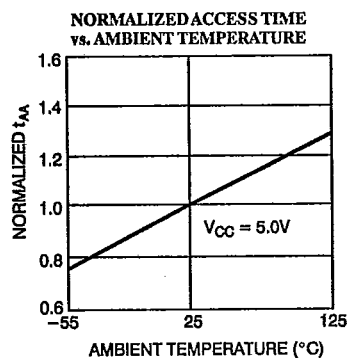
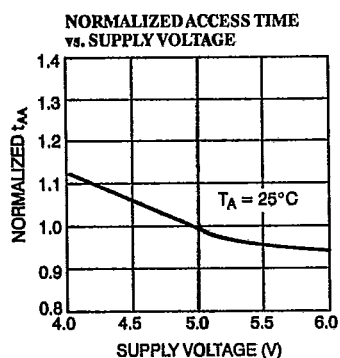
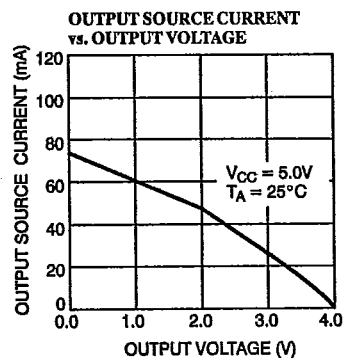
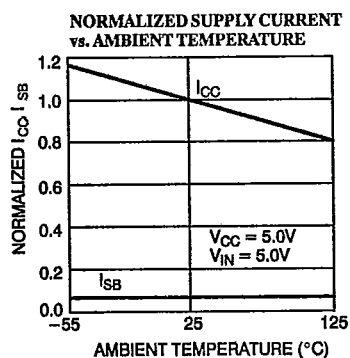
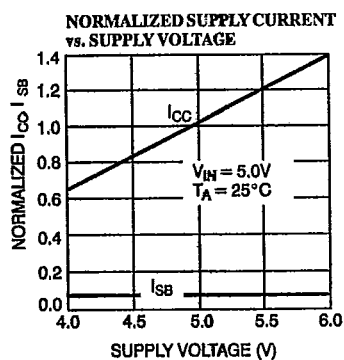
Write Cycle No. 2 ($\overline{CS}$ Controlled)^[10, 14]

C168A-9

CY7C168A
CY7C169A

Typical DC and AC Characteristics

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CY7C168A

CY7C169A

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Ordering Information

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Type	Operating Range
15	115	CY7C168A-15PC	P5	Commercial
		CY7C168A-15DC	D6	
		CY7C168A-15VC	V5	
20	90	CY7C168A-20PC	P5	Commercial
		CY7C168A-20DC	D6	
		CY7C168A-20VC	V5	
		CY7C168A-20DMB	D6	Military
		CY7C168A-20LMB	L51	
		CY7C168A-20FMB	F71	
		CY7C168A-20KMB	K71	
25	70	CY7C168A-25PC	P5	Commercial
		CY7C168A-25DC	D6	
		CY7C168A-25LC	L51	
		CY7C168A-25VC	V5	
	80	CY7C168A-25DMB	D6	Military
		CY7C168A-25LMB	L51	
		CY7C168A-25FMB	F71	
		CY7C168A-25KMB	K71	
	70	CY7C168A-35PC	P5	Commercial
		CY7C168A-35DC	D6	
		CY7C168A-35LC	L51	
		CY7C168A-35VC	V5	Military
		CY7C168A-35DMB	D6	
		CY7C168A-35LMB	L51	
45	50	CY7C168A-45PC	P5	Commercial
		CY7C168A-45DC	D6	
		CY7C168A-45LC	L51	
		CY7C168A-45VC	V5	
	70	CY7C168A-45DMB	D6	Military
		CY7C168A-45LMB	L51	
		CY7C168A-45FMB	F71	
		CY7C168A-45KMB	K71	

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Type	Operating Range
15	115	CY7C169A-15PC	P5	Commercial
		CY7C169A-15DC	D6	
		CY7C169A-15VC	V5	
20	90	CY7C169A-20PC	P5	Commercial
		CY7C169A-20DC	D6	
		CY7C169A-20VC	V5	
		CY7C169A-20DMB	D6	Military
		CY7C169A-20LMB	L51	
		CY7C169A-20FMB	F71	
		CY7C169A-20KMB	K71	
		CY7C169A-20KMB	K71	
25	70	CY7C169A-25PC	P5	Commercial
		CY7C169A-25DC	D6	
		CY7C169A-25LC	L51	
		CY7C169A-25VC	V5	
	80	CY7C169A-25DMB	D6	Military
		CY7C169A-25LMB	L51	
		CY7C169A-25FMB	F71	
		CY7C169A-25KMB	K71	
	70	CY7C169A-35PC	P5	Commercial
		CY7C169A-35DC	D6	
		CY7C169A-35LC	L51	
		CY7C169A-35VC	V5	Military
		CY7C169A-35DMB	D6	
		CY7C169A-35LMB	L51	
45	50	CY7C169A-45PC	P5	Commercial
		CY7C169A-45DC	D6	
		CY7C169A-45LC	L51	
		CY7C169A-45VC	V5	
	70	CY7C169A-45DMB	D6	Military
		CY7C169A-45LMB	L51	
		CY7C169A-45FMB	F71	
		CY7C169A-45KMB	K71	



SRAMs



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MILITARY SPECIFICATIONS
Group A-Subgroup Testing

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DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1} ^[15]	1, 2, 3
I _{SB2} ^[15]	1, 2, 3

Note:

15. 7C168 only.

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{RCS}	7, 8, 9, 10, 11
t _{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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