

CYPRESS
SEMICONDUCTOR

T-4623-08

CY7C170

4096 x 4 Static R/W RAM

Features

- CMOS for optimum speed/power
- High speed
 - $t_{AA} = 25$ ns
 - $t_{ACS} = 15$ ns
- Low active power
 - 495 mW (commercial)
 - 660 mW (military)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable

Functional Description

The CY7C170 is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$), and three-state drivers.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four I/O pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

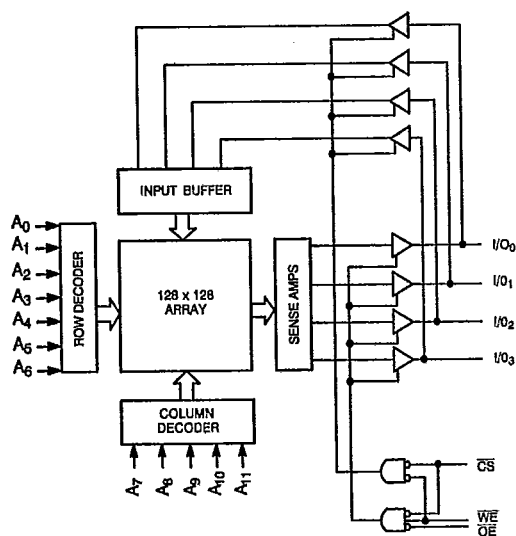
Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

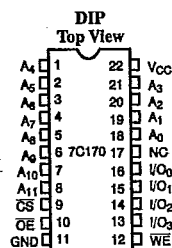
A die coat is used to insure alpha immunity.



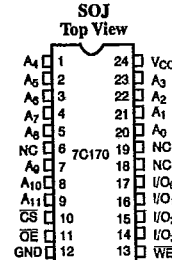
SRAMS

Logic Block Diagram

C170-1

Pin Configurations

C170-2



C170-3

Selection Guide

		7C170-25	7C170-35	7C170-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120



T-46-23-08

CY7C170

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ⁽¹⁾	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range⁽²⁾

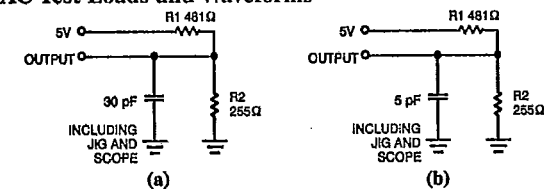
Parameters	Description	Test Conditions	7C170		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-50	+50	μA
I _{OS}	Output Short Circuit Current ⁽³⁾	V _{CC} = Max., V _{OUT} = GND		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA	Com'l	90	mA
			Mil	120	mA

Capacitance⁽⁴⁾

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

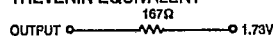
Notes

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

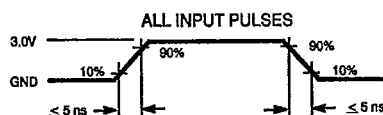
AC Test Loads and Waveforms

Equivalent to:

THEVENIN EQUIVALENT



C170-4



C170-5



T-46-23-08

CY7C170

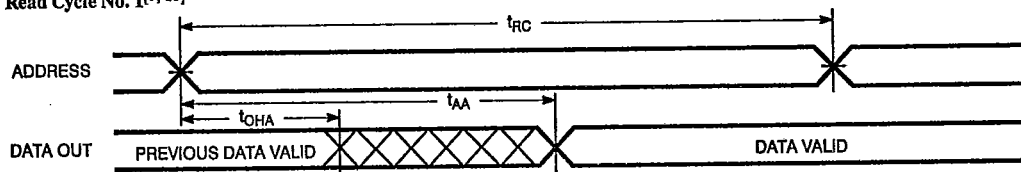
Switching Characteristics Over the Operating Range^[2, 5]

Parameters	Description	7C170-25		7C170-35		7C170-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Output Hold from AddressChange	3		3		3		ns
t _{ACS}	$\overline{CS}$ LOW to Data Valid		15		25		30	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		15		15		20	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6]		15		15		15	ns
t _{LZCS}	$\overline{CS}$ LOW to Low Z ^[7]	3		5		5		ns
t _{HZCS}	$\overline{CE}$ HIGH to High Z ^[6, 7]		15		20		25	ns
WRITE CYCLE ^[8]								
t _{WC}	Write Cycle Time	25		35		40		ns
t _{SCS}	$\overline{CS}$ LOW to Write End	25		35		35		ns
t _{AW}	Address Set-Up to Write End	20		30		35		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	20		30		35		ns
t _{SD}	Data Set-Up to Write End	10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		3		ns
t _{HZWE}	$\overline{WE}$ HIGH to High Z		10		15		20	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	6		6		6		ns

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} , and 30-pF load capacitance.
- t_{HZOE} , t_{HZCS} , and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
- Address valid prior to or coincident with $\overline{CE}$ transition LOW.
- Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
- If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1^[9, 10]

C170-8

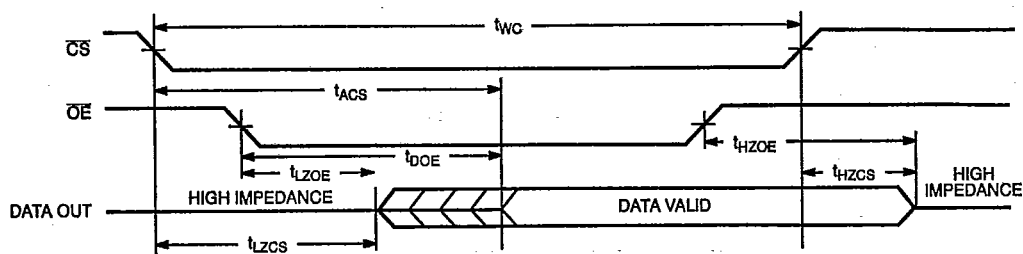


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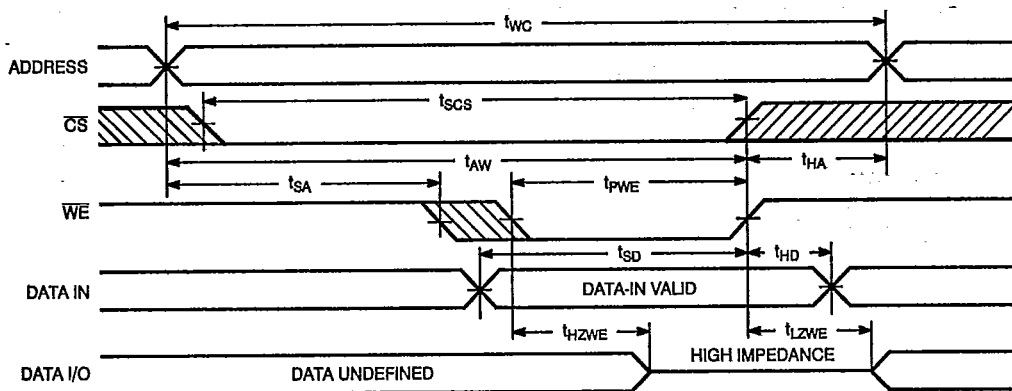
CY7C170

Switching Waveforms (continued)

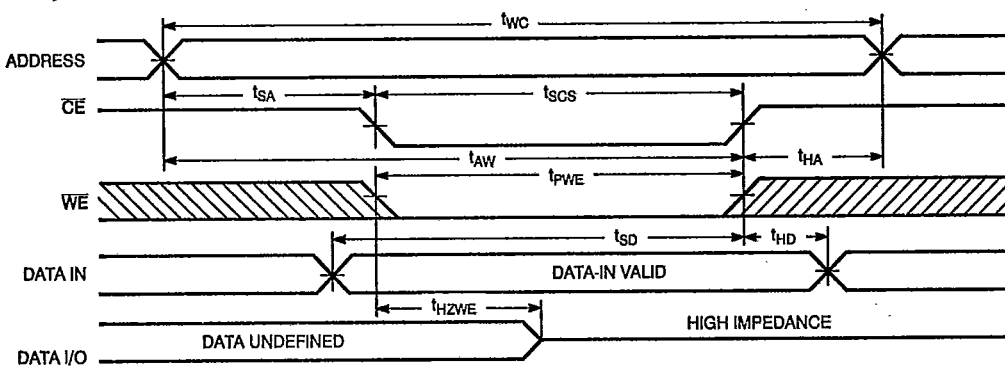
T-46-23-08

Read Cycle No. 2^[9, 11]

C170-7

Write Cycle No. 1 (WE Controlled)^[8, 12]

C170-8

Write Cycle No. 2 (CS Controlled)^[8, 12, 13]

C170-9



T-46-23-08

CY7C170

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C170-25PC	P9	Commercial
	CY7C170-25DC	D10	
	CY7C170-25VC	V13	
35	CY7C170-35PC	P9	Commercial
	CY7C170-35DC	D10	
	CY7C170-35VC	V13	
	CY7C170-35DMB	D10	Military
45	CY7C170-45PC	P9	Commercial
	CY7C170-45DC	D10	
	CY7C170-45VC	V13	
	CY7C170-45DMB	D10	Military



SRAMs

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACS}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCS}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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