

CYPRESS
SEMICONDUCTOR

T-46-23-05 CY7C187

65,536 x 1 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
 - 15 ns
- Low active power
 - 495 mW
- Low standby power
 - 220 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A₀ through A₁₅).

Reading the device is accomplished by taking the chip enable (CE) LOW, while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable (CE) is HIGH or write enable (WE) is LOW.

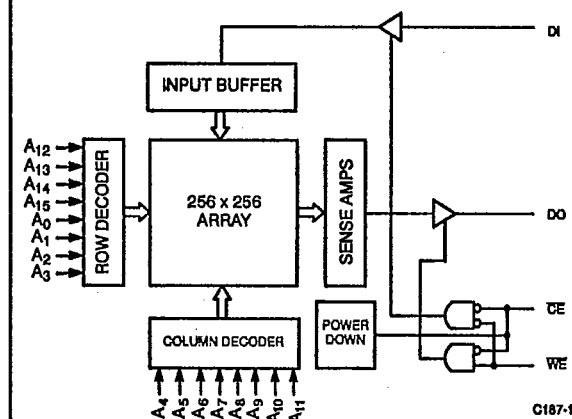
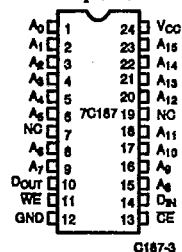
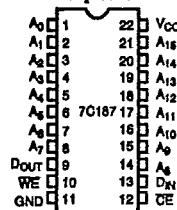
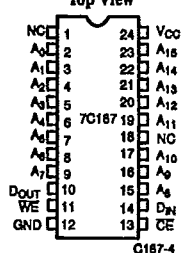
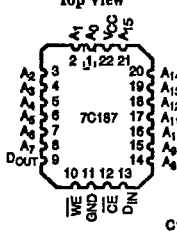
The 7C187 utilizes a die coat to insure alpha immunity.



SRAMS

Logic Block Diagram

Pin Configurations

SOJ
Top ViewDIP
Top ViewCerpack
Top ViewLCC
Top ViewSelection Guide^[1]

	7C187-10	7C187-12	7C187-15	7C187-20	7C187-25	7C187-35	7C187-45
Maximum Access Time (ns)	10	12	15	20	25	35	45
Maximum Operating Current (mA)	160	160	90	80	70	70	50
Maximum Standby Current (mA)	40/40	40/40	40/20	40/20	20/20	20/20	20/20

Shaded area indicates advanced information.

Note:

1. For military specifications, see the CY7C187A datasheet.



T-46-23-05

CY7C187

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C

Ambient Temperature with

Power Applied - 55°C to +125°C

Supply Voltage to Ground Potential

(Pin 22 to Pin 11) - 0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State - 0.5V to +7.0V

DC Input Voltage - 3.0V to +7.0V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C187-10		7C187-12		7C187-15		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		- 3.0	0.8	- 3.0	0.8	- 3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 10	+10	- 10	+10	- 10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+10	- 10	+10	- 10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		- 350		- 350		- 350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		160		160		90	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$		40		40		40	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

Shaded area indicates advanced information.



Electrical Characteristics Over the Operating Range(continued)

Parameters	Description	Test Conditions	7C187-20		7C187-25, 35		7C187-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 12.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[2]		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		80		70		50	mA
I _{SB1}	Automatic CE Power-Down Current ^[4]	Max. V _{CC} , CE ≥ V _{IH}		40		20		20	mA
I _{SB2}	Automatic CE Power-Down Current	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

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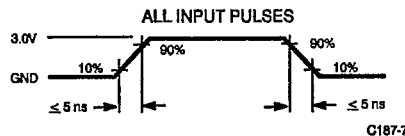
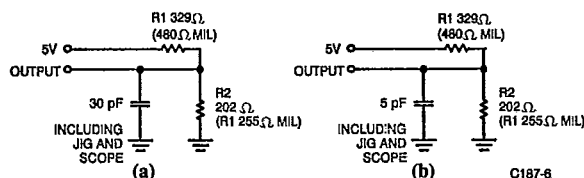
Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

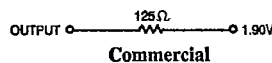
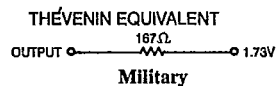
Notes:

- V_{IL} min. = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to:



CYPRESS
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T-46-23-05

CY7C187

Switching Characteristics Over the Operating Range^[6]

Parameters	Description	7C187-10		7C187-12		7C187-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Output Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7]	2		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[8, 9]		5		7		8	ns
t _{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power Down		10		12		15	ns
WRITE CYCLE ^[9]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	8		8		12		ns
t _{AW}	Address Set-up to Write End	8		9		12		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	8		8		12		ns
t _{SD}	Data Set-up to Write End	5		6		10		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[9]	2		3		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[9, 10]		6		6		7	ns

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T-46-23-05

CY7C187

Switching Characteristics Over the Operating Range^[6] (continued)

Parameters	Description	7C187-20		7C187-25		7C187-35		7C187-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	20		25		35		45		ns
t _{AA}	Address to Data Valid		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	5		5		5		5		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		20		25		35		45	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[7]	5		5		5		5		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[8, 9]		8		10		15		15	ns
t _{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power Down		20		20		20		25	ns
WRITE CYCLE ^[9]										
t _{WC}	Write Cycle Time	20		20		25		40		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low ^[9]	5		5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[9, 10]		7		7		10		15	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$ is HIGH for read cycle.

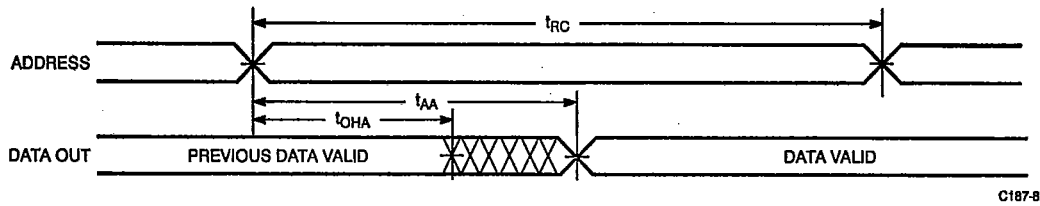
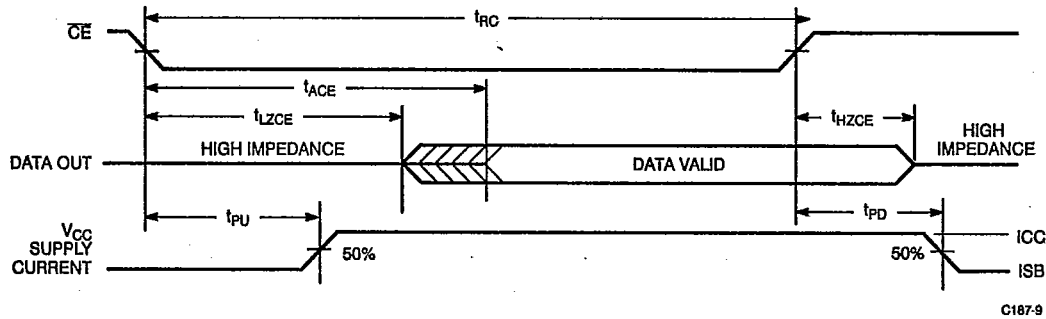
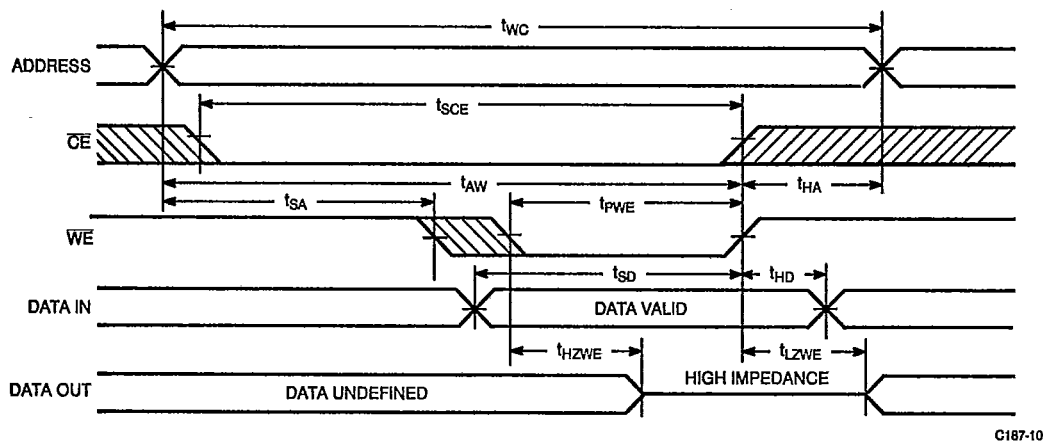
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T-46-23-05

CY7C187

Switching Waveforms

Read Cycle No. 1^[10, 11]Read Cycle No. 2^[10, 12]Write Cycle No. 1 ($\overline{WE}$ Controlled)^[11]

Notes:

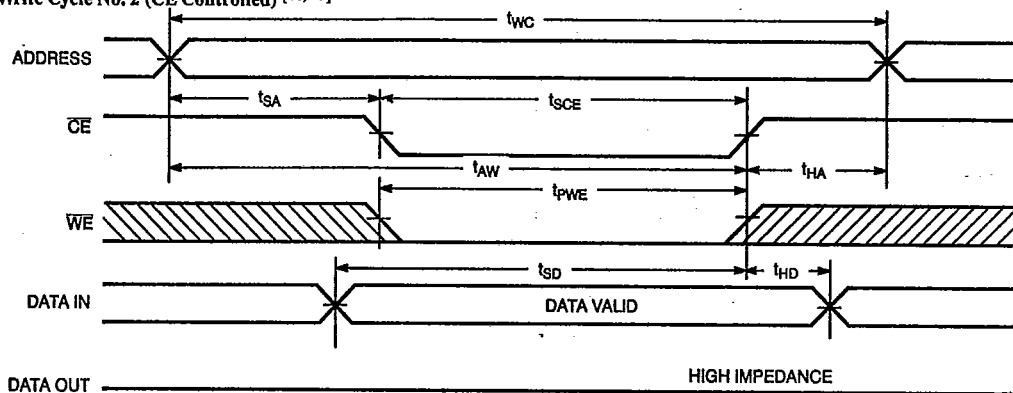
11. Device is continuously selected, $\overline{CE} = V_{IL}$.12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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T-46-23-05

CY7C187

Switching Waveforms (continued)

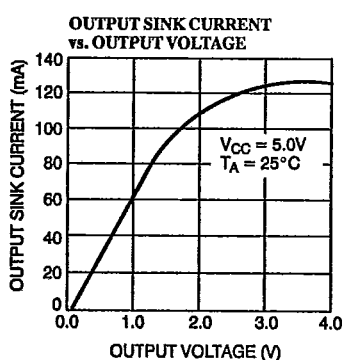
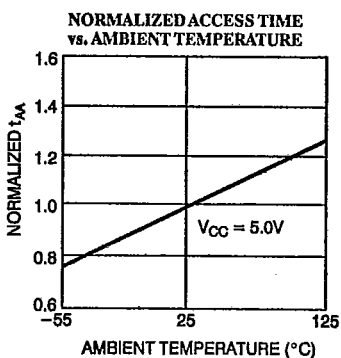
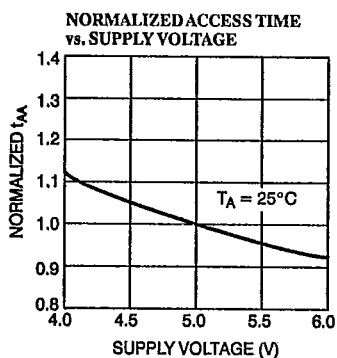
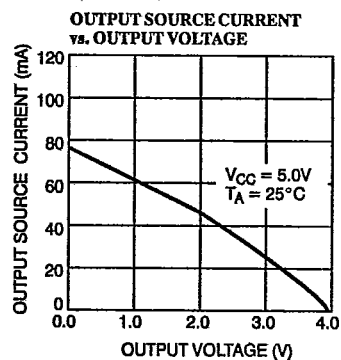
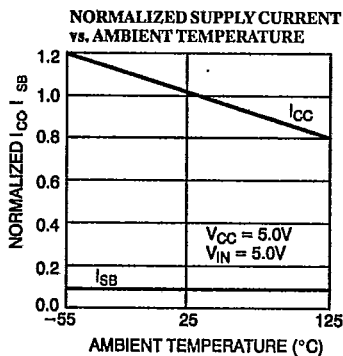
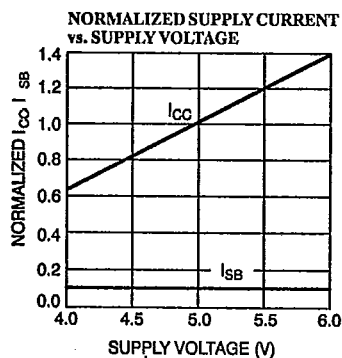
Write Cycle No. 2 ($\overline{CE}$ Controlled) [11, 13]

C187-11

Notes:

13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

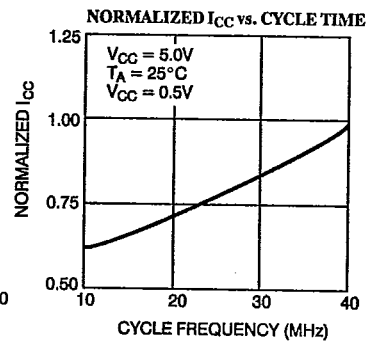
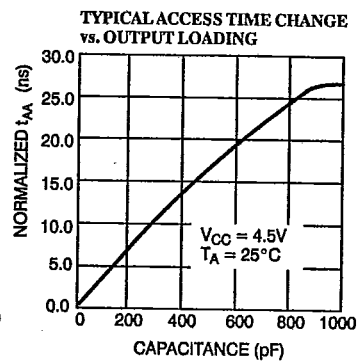
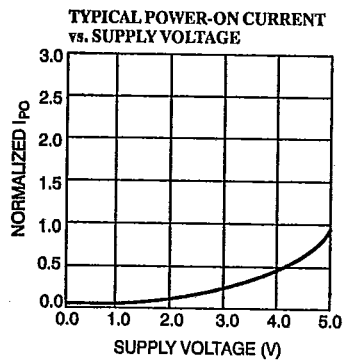


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T-46-23-05

CY7C187

Typical DC and AC Characteristics (continued)



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

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T-46-23-05

CY7C187

Ordering Information^[14]

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C187-10DC	D10	Commercial
	CY7C187-10LC	L52	
	CY7C187-10PC	P9	
	CY7C187-10VC	V13	
12	CY7C187-12DC	D10	Commercial
	CY7C187-12LC	L52	
	CY7C187-12PC	P9	
	CY7C187-12VC	V13	
15	CY7C187-15DC	D10	Commercial
	CY7C187-15LC	L52	
	CY7C187-15PC	P9	
	CY7C187-15VC	V13	
20	CY7C187-20DC	D10	Commercial
	CY7C187-20LC	L52	
	CY7C187-20PC	P9	
	CY7C187-20VC	V13	
25	CY7C187-25DC	D10	Commercial
	CY7C187-25LC	L52	
	CY7C187-25PC	P9	
	CY7C187-25VC	V13	
35	CY7C187-35DC	D10	Commercial
	CY7C187-35LC	L52	
	CY7C187-35PC	P9	
	CY7C187-35VC	V13	
45	CY7C187-45DC	D10	Commercial
	CY7C187-45LC	L52	
	CY7C187-45PC	P9	
	CY7C187-45VC	V13	

Shaded area indicates advanced information.

Notes:

14. For military variations, see the CY7C187A datasheet.

Document #: 38-00038-H



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