CYPRESS SEMICONDUCTOR

CY7C225

512 x 8 Registered PROM

Features

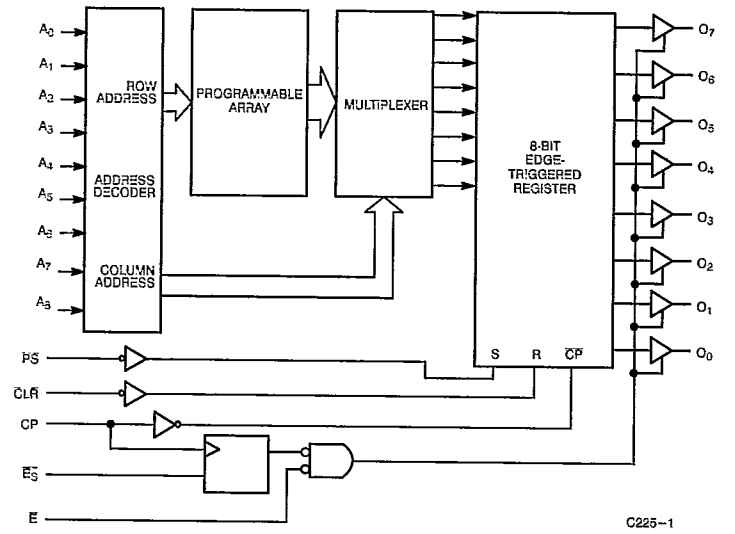
- CMOS for optimum speed/power
- High speed
  - —25 ns max set-up
  - —12 ns clock to output
- Low power
  - —495 mW (commercial)
  - —660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- EPROM technology, 100% programmable
- Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC
- 5V ±10% V_{CC}, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 1500V static discharge

Functional Description

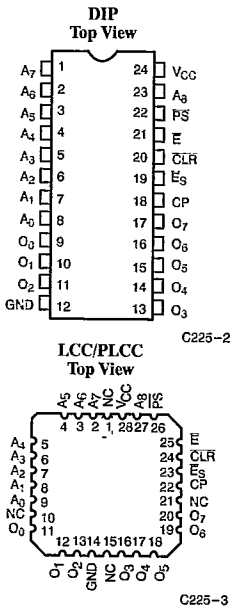
The CY7C225 is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C225-25	7C225-30	7C225-35	7C225-40
Maximum Set-Up Time (ns)		25	30	35	40
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90		90
	Military		120	120	120

CYPRESS SEMICONDUCTOR

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	− 40°C to +85°C	5V ± 10%
Military[2]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA, V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		− 10	+10	µA
V_{CD}	Input Clamp Diode Voltage	Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled[5]		− 40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		− 20	− 90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA, V_{CC} = Max.[7]	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			13	14	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

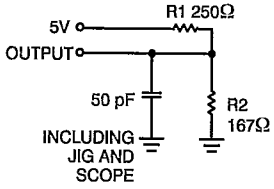
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

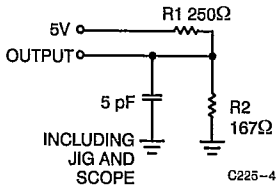
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Due to the design of the differential cell in this device, I_{CC} can only be accurately measured on a programmed array.

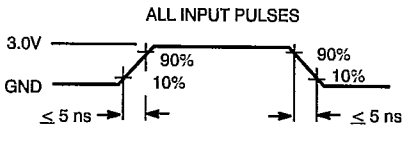
AC Test Loads and Waveforms[4]



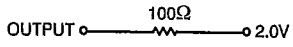
(a) Normal Load



(b) High Z Load



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

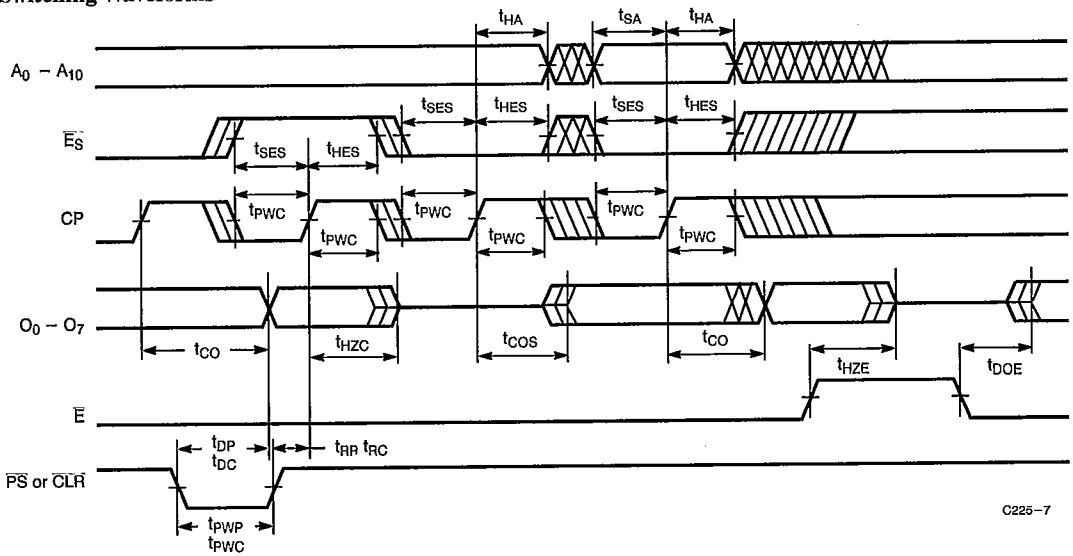
The CY7C225 has buffered asynchronous $\overline{CLEAR}$ and $\overline{PRESET}$ inputs. Applying a LOW to the $\overline{PRESET}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{CLEAR}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C225–25		7C225–30		7C225–35		7C225–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		20		ns
t_{SES}	$\overline{E_S}$ Setup to Clock HIGH	10		10		10		10		ns
t_{HES}	$\overline{E_S}$ Hold from Clock HIGH	0		5		5		5		ns
t_{DP} t_{DC}	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ to Valid Output		20		20		20		20	ns
t_{RR} t_{RC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWP} t_{PWC}	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width	15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[8]		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[8]		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		20		20		25		30	ns

Switching Waveforms[4]



Note:
8. Applies only when the synchronous ($\overline{E_S}$) function is used.

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[9]						
	Read or Output Disable	$A_8 - A_0$	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	$O_7 - O_0$
	Other	$A_8 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	$D_7 - D_0$
Read		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_8 - A_0$	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_8 - A_0$	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
Clear		$A_8 - A_0$	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
Preset		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Program Verify		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_8 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Blank Check Ones		$A_8 - A_0$	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	Ones
Blank Check Zeros		$A_8 - A_0$	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	Zeros

Note:
9. X = "don't care" but not to exceed V_{CC} ±5%.

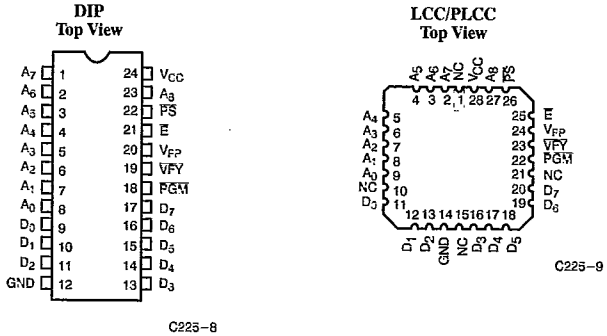
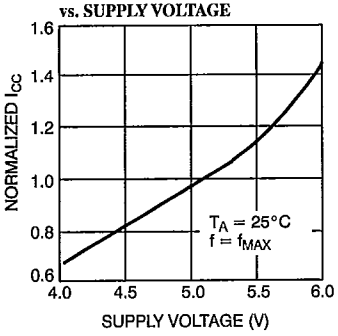


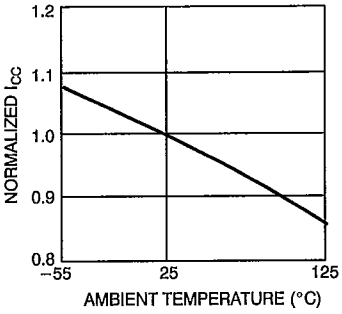
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

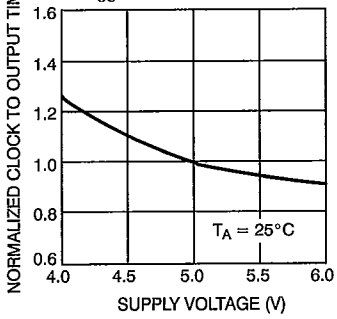
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



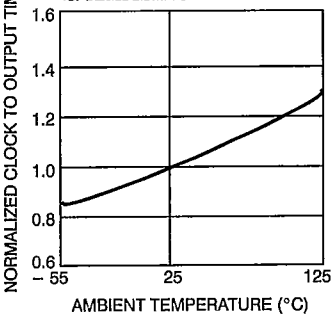
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



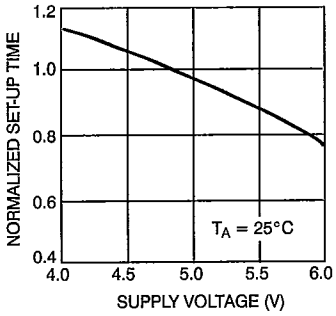
CLOCK TO OUTPUT TIME vs. V_{CC}



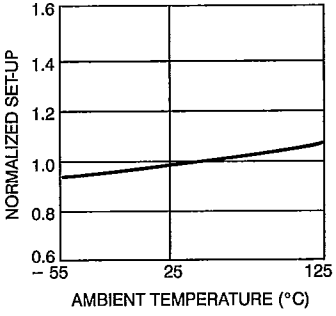
CLOCK TO OUTPUT TIME vs. TEMPERATURE



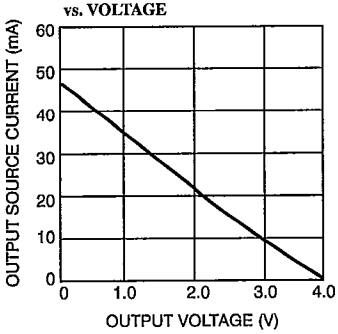
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



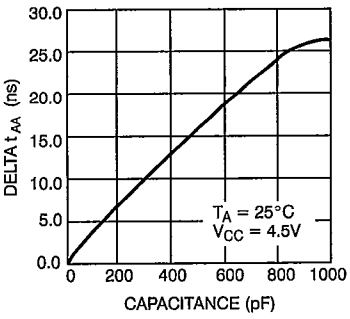
NORMALIZED SET-UP TIME vs. TEMPERATURE



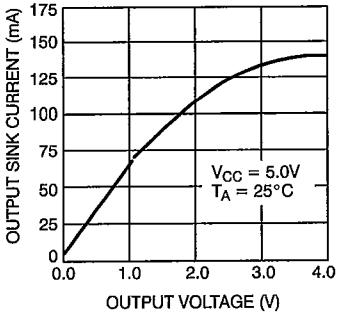
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



C225–10

Ordering Information[10]

Speed (ns)		Ordering Code	Package Name	Package Type	Operating Range
t_{SA}	t_{CO}				
25	12	CY7C225–25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–25PC	P13	24-Lead (300-Mil) Molded DIP	
30	15	CY7C225–30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225–35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225–40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225–40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225–40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225–40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225–40LMB	L64	28-Square Leadless Chip Carrier	

Note:

10. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DP}	7, 8, 9, 10, 11
t_{RP}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962–88518	01LX	CY7C225–30DMB
5962–88518	013X	CY7C225–30LMB
5962–88518	02LX	CY7C225–35DMB
5962–88518	023X	CY7C225–35LMB
5962–88518	03LX	CY7C225–40DMB
5962–88518	033X	CY7C225–40LMB

Document #: 38–00002–E

CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

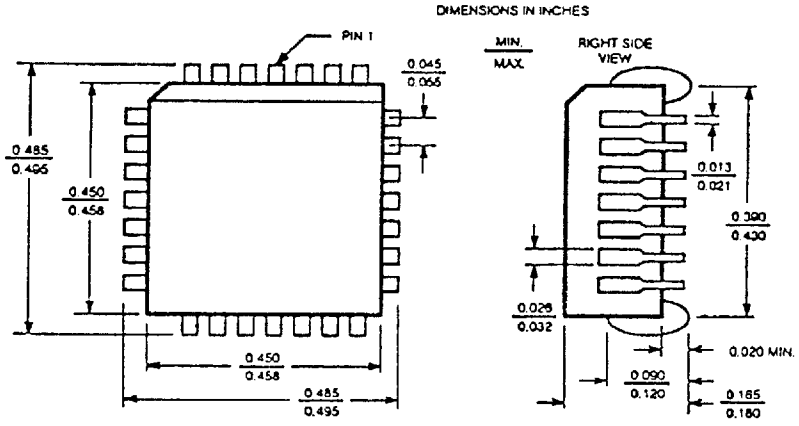
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

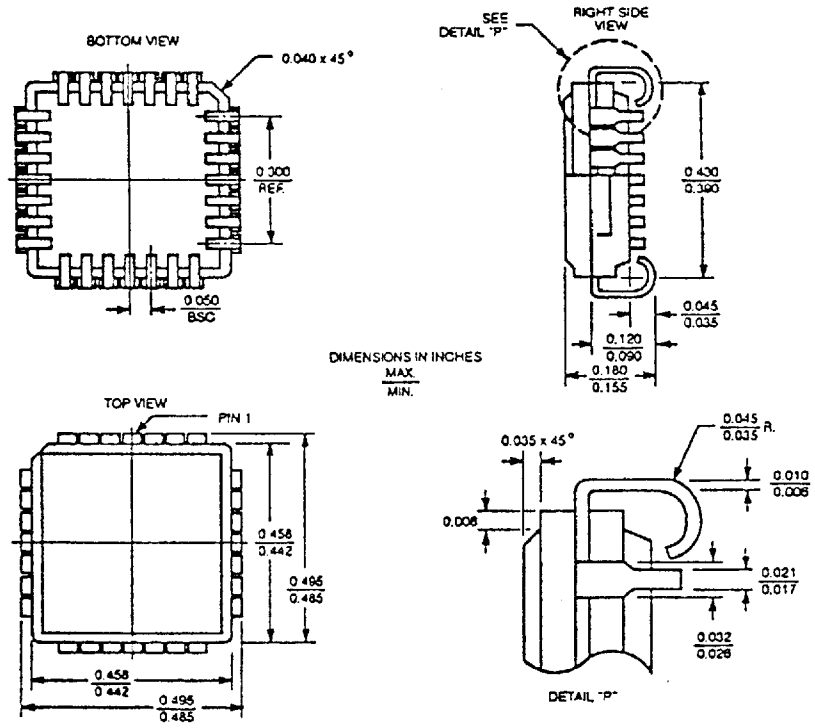


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

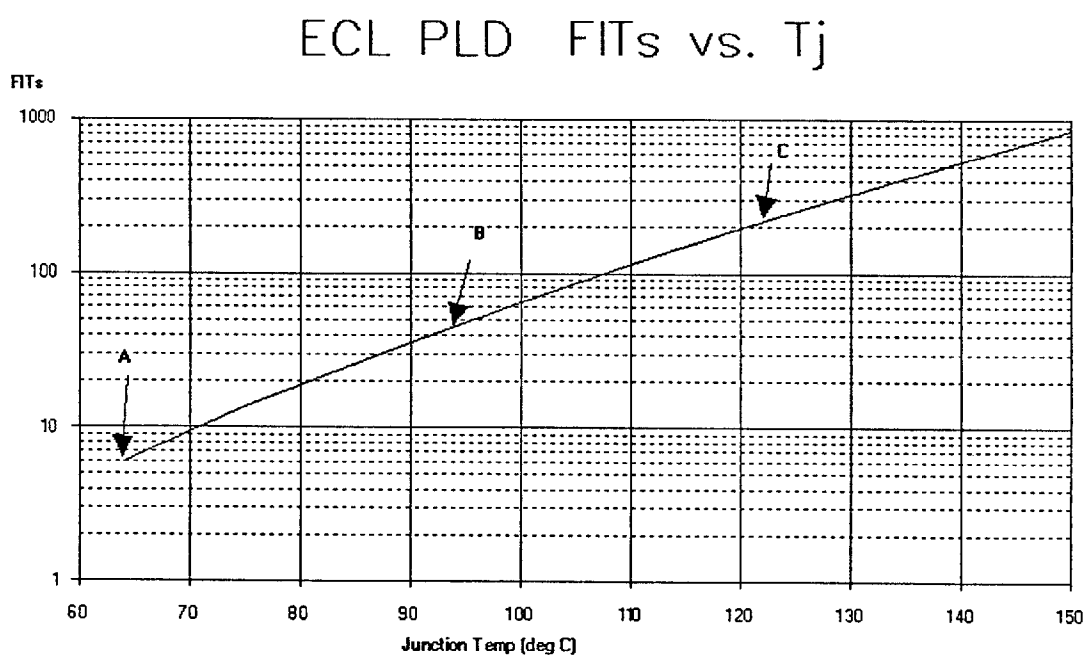


Figure 2. Failures in Time vs Junction Temperature

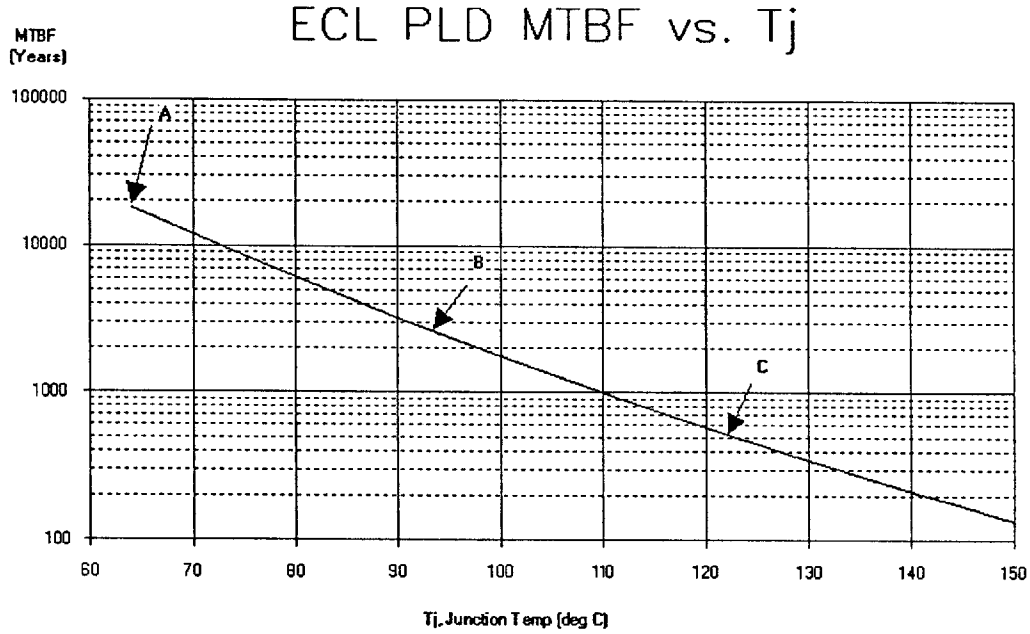


Figure 3. Mean Time Between Failures vs Junction Temp.

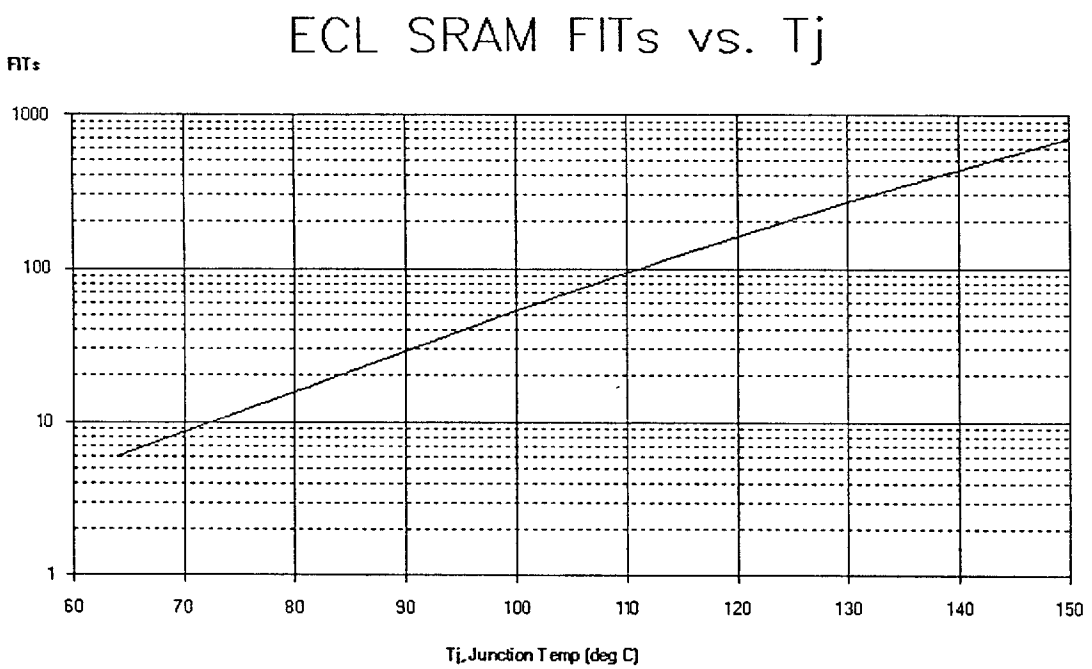


Figure 4. Failures in Time vs Junction Temperature

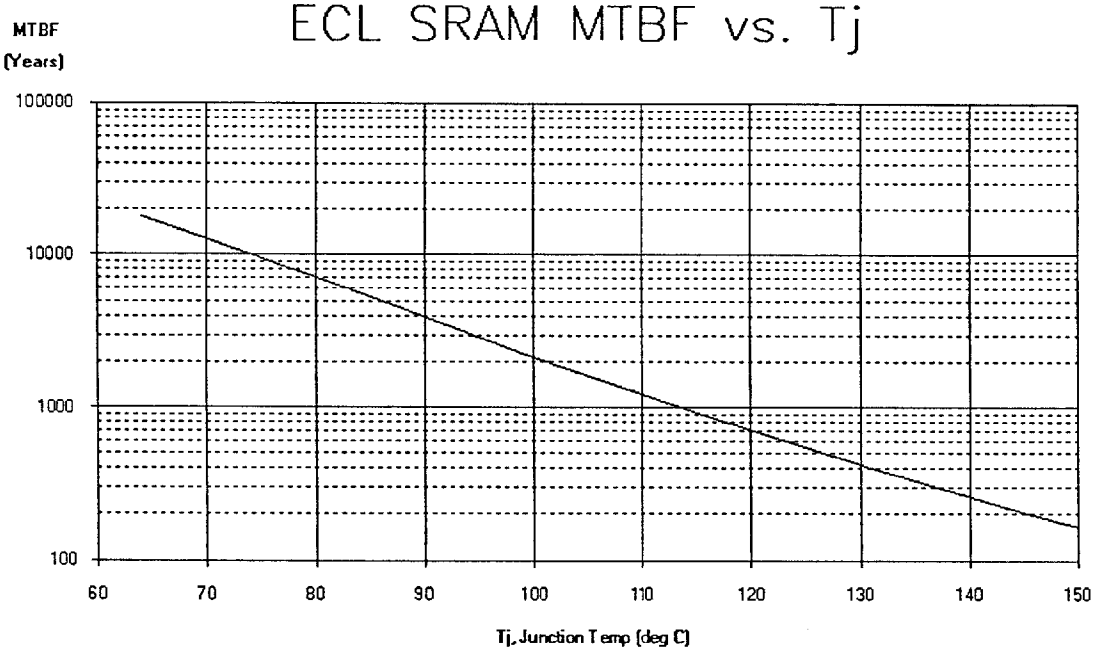


Figure 5. Mean Time Between Failure vs Junction Temp.