CY7C225A

512 x 8 Registered PROM

Features

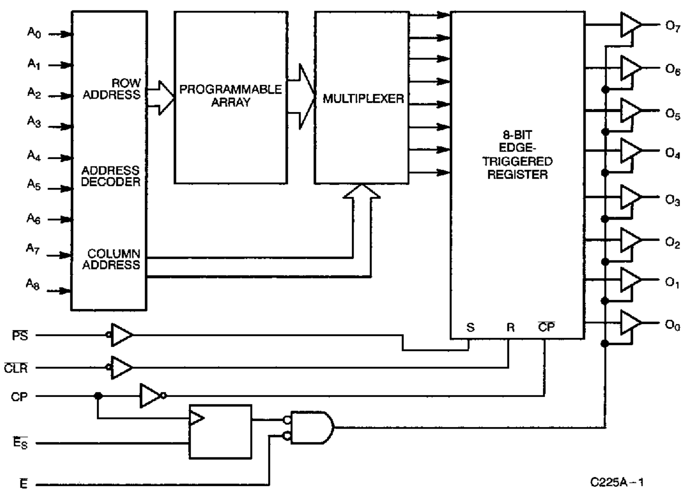
- **CMOS for optimum speed/power**
- **High speed**
  - **— 18 ns address set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs**
- **EPROM technology, 100% programmable**
- **Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C225A is a high-performance 512 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225A replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

Logic Block Diagram



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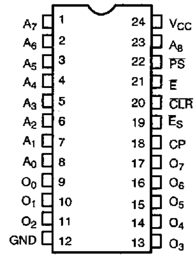
Pin Configurations

DIP
Top View



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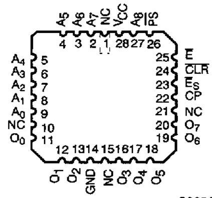
LCC/PLCC
Top View



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Selection Guide

		7C225A–18	7C225A–25	7C225A–30	7C225A–35	7C225A–40
Minimum Address Set-Up Time (ns)		18	25	30	35	40
Maximum Clock to Output (ns)		12	12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90	90		90
	Military		120	120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3, 4]

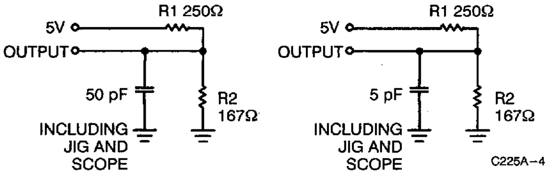
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 4				
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled[5]		−10	+10	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[6]		−20	−90	mA
I_{CC}	Power Supply Current	I_{OUT} = 0 mA V_{CC} = Max.	Commercial		90	mA
			Military		120	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

Capacitance[4]

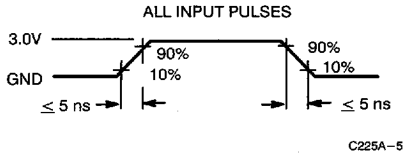
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

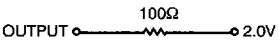
AC Test Loads and Waveforms[4]



(a) Normal Load **(b) High Z Load**



Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C225A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E_S}$) and asynchronous ($\overline{E}$) output enables and $\overline{CLEAR}$ and $\overline{PRESET}$ inputs.

Upon power-up, the synchronous enable ($\overline{E_S}$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs ($A_0 - A_8$) and a logic LOW to the enable ($\overline{E_S}$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\overline{E_S}$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225A has buffered asynchronous $\overline{CLEAR}$ and $\overline{PRESET}$ inputs. Applying a LOW to the $\overline{PRESET}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{CLEAR}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

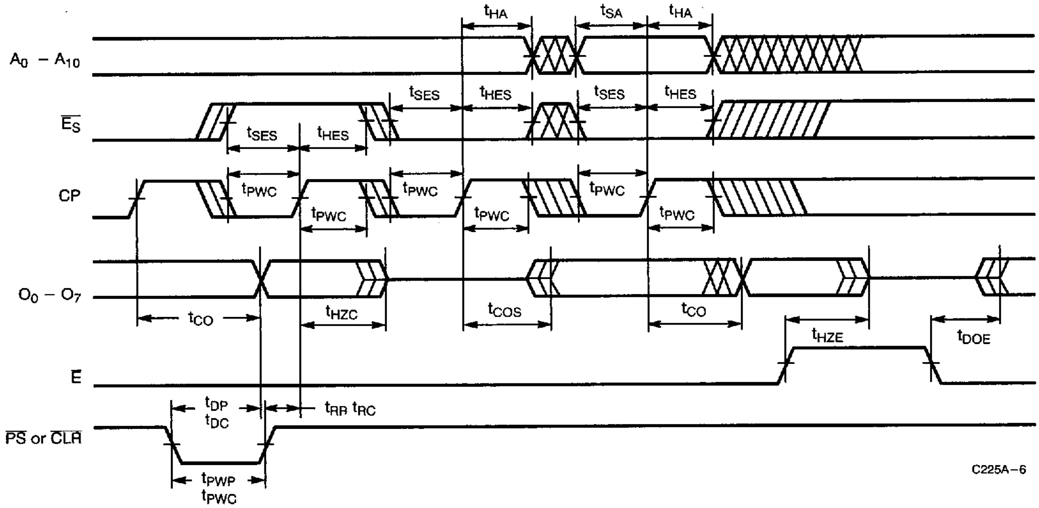
When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\overline{E_S}$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C225A–18		7C225A–25		7C225A–30		7C225A–35		7C225A–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	18		25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		10		10		10		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	0		0		5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ to Valid Output		20		20		20		20		20	ns
t_{RP}, t_{RC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Recovery to Clock HIGH	15		15		20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Pulse Width	15		15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[7]		15		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		15		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		15		20		20		25		30	ns

Note:
7. Applies only when the synchronous ($\overline{E}_S$) function is used.

Switching Waveforms[4]



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Programming Information

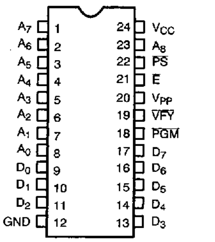
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode		Pin Function[8]						
	Read or Output Disable	$A_8 - A_0$	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	$O_7 - O_0$
	Other	$A_8 - A_0$	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	$D_7 - D_0$
Read		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	$O_7 - O_0$
Output Disable		$A_8 - A_0$	X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		$A_8 - A_0$	X	X	V_{IH}	V_{IH}	V_{IH}	High Z
Clear		$A_8 - A_0$	X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
Preset		$A_8 - A_0$	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Program Verify		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	$O_7 - O_0$
Program Inhibit		$A_8 - A_0$	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program		$A_8 - A_0$	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	$D_7 - D_0$
Blank Check		$A_8 - A_0$	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	Zeros

Note:
8. X = "don't care" but not to exceed V_{CC} ±5%.

DIP
Top View



C225A–7

LCC/PLCC
Top View

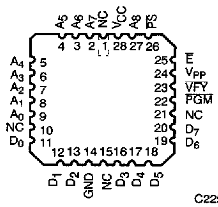


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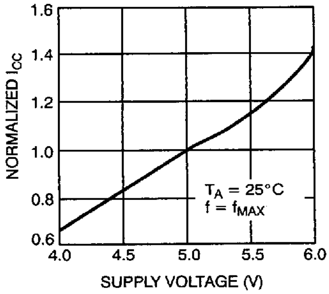
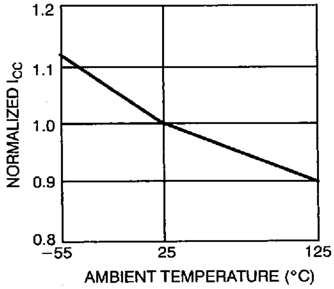
Figure 1. Programming Pinouts

Typical DC and AC Characteristics

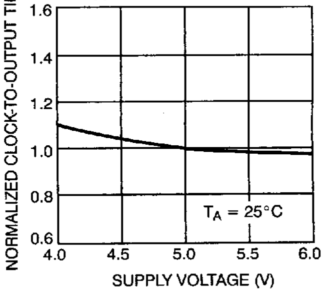
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



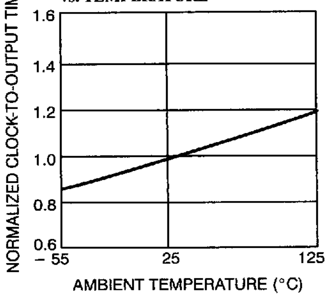
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



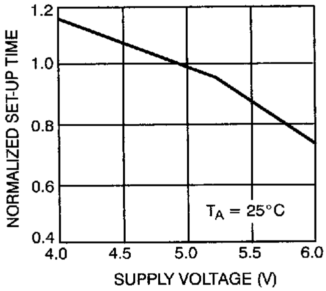
CLOCK TO OUTPUT TIME vs. V_{CC}



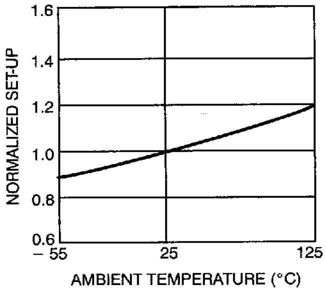
CLOCK TO OUTPUT TIME vs. TEMPERATURE



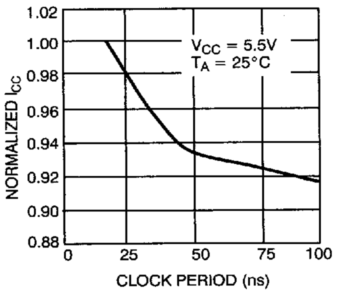
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



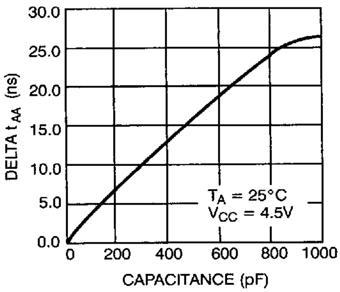
NORMALIZED SET-UP TIME vs. TEMPERATURE



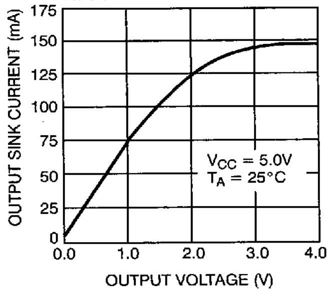
NORMALIZED SUPPLY CURRENT vs. CLOCK PERIOD



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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Ordering Information[9]

Speed (ns) t_{SA}	Speed (ns) t_{CO}	Ordering Code	Package Type	Package Type	Operating Range
18	12	CY7C225A−18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A−18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A−18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C225A−25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A−25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A−25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A−25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A−25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C225A−30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A−30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A−30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A−30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A−30LMB	L64	28-Square Leadless Chip Carrier	
35	20	CY7C225A−35DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A−35LMB	L64	28-Square Leadless Chip Carrier	
40	25	CY7C225A−40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C225A−40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C225A−40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C225A−40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C225A−40LMB	L64	28-Square Leadless Chip Carrier	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DP}	7, 8, 9, 10, 11
t_{RP}	7, 8, 9, 10, 11

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