



CYPRESS SEMICONDUCTOR

CY7C235

1K x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
 - 25 ns max set-up
 - 12 ns clock to output
- **Low power**
 - 495 mW (commercial)
 - 660 mW (military)
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous registers (INIT)**
- **EPROM technology, 100% programmable**

- Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC
- $5V \pm 10\% V_{CC}$, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 1500V static discharge

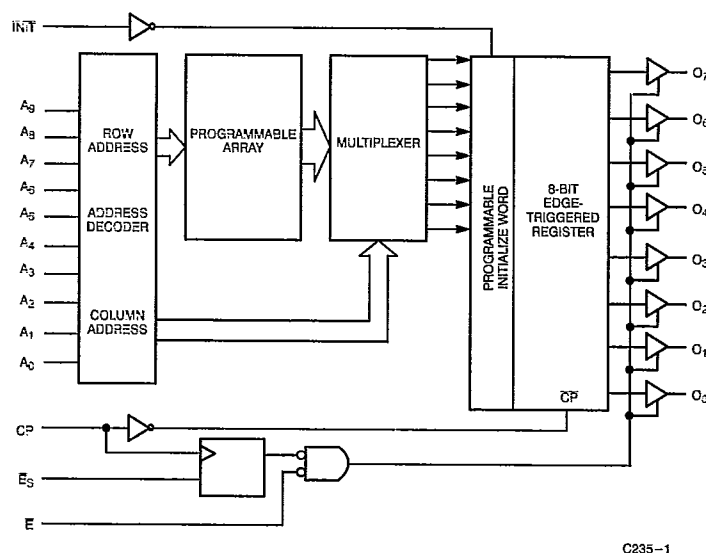
Functional Description

The CY7C235 is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells uti-

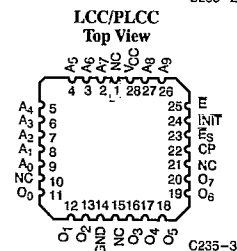
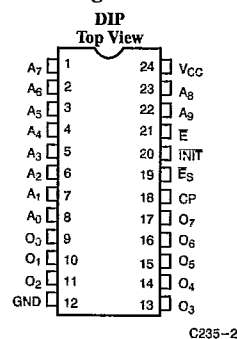
lize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 13.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C235 – 25	7C235 – 30	7C235 – 40
Maximum Set-Up Time (ns)		25	30	40
Maximum Clock to Output (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP)	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V
DC Program Voltage (Pins 7, 18, 20 for DIP)	14.0V

Static Discharge Voltage >1500V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	- 40°C to +85°C	5V ±10%
Military ^[2]	- 55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range^[3]

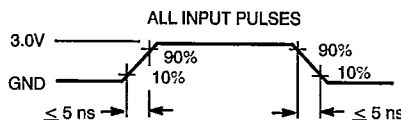
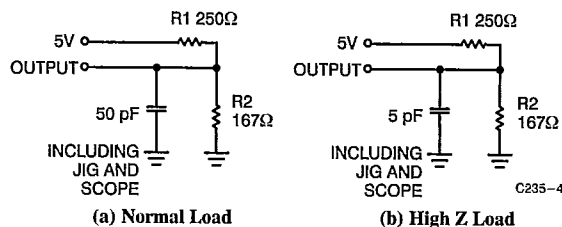
Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OIH}	Output HIGH Voltage	V _{CC} = Min., I _{OIH} = - 4.0 mA V _{IN} = V _{IH} or V _{IL}	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs ^[4]	2.0		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs ^[4]		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	- 10	+10	μA
V _{CD}	Input Clamp Diode Voltage	Note 5			
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} Output Disabled ^[5]	- 40	+40	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	- 20	- 90	mA
I _{CC}	Power Supply Current ^[7]	V _{CC} = Max., I _{OUT} = 0 mA	Commercial	90	mA
			Military	120	
V _{PP}	Programming Supply Voltage		13	14	V
I _{PP}	Programming Supply Current			50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4	V

Capacitance^[5]

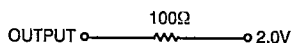
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
7. Due to the design of the differential cell in this device, I_{CC} can only be accurately measured on a programmed array.

AC Test Loads and Waveforms^[5]

Equivalent to: THÉVENIN EQUIVALENT



Operating Modes

The CY7C235 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\bar{E}_S$) and asynchronous ($\bar{E}$) output enables and asynchronous initialization ($\bar{INIT}$).

Upon power-up, the synchronous enable ($\bar{E}_S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable ($\bar{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable ($\bar{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\bar{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of $\bar{E}$, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable ($\bar{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\bar{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system

clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235 has an asynchronous initialize input ($\bar{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating $\bar{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\bar{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\bar{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\bar{E}$) LOW.

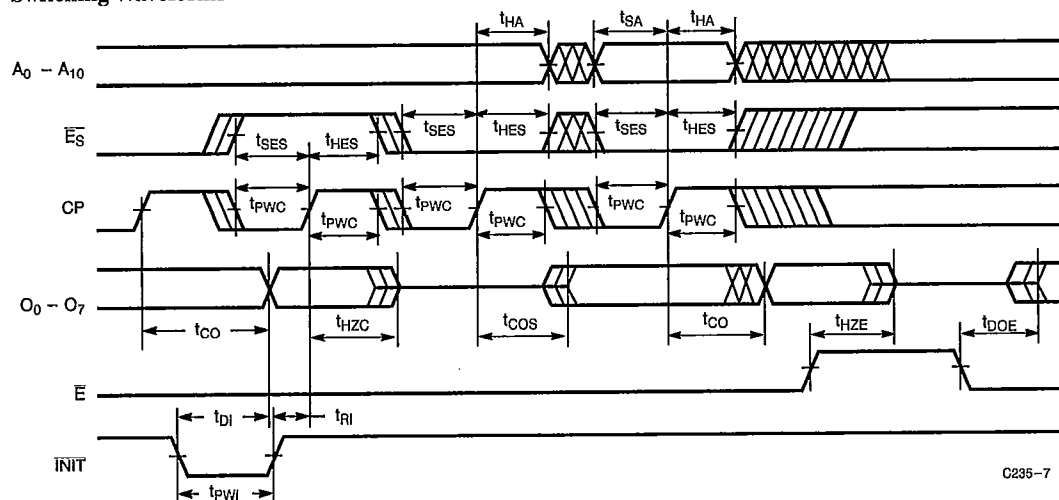
When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the $\bar{E}_S$ input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The $\bar{E}$ input may then be used to enable the outputs.

When the asynchronous initialize input, $\bar{INIT}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Characteristics Over Operating Range^[3, 5]

Parameter	Description	7C235-25		7C235-30		7C235-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	10		10		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{INIT}$ to Valid Output		25		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock HIGH	20		20		20		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH ^[8]		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH ^[8]		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH		20		20		25	ns

Note:

8. Applies only when the synchronous ($\overline{E}_S$) function is used.Switching Waveforms^[5]

C235-7



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please

see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

Mode	Pin Function ^[9]								
	Read or Output Disable	A ₀ , A ₃ - A ₉	A ₁	A ₂	CP	$\bar{E}_S$	$\bar{E}$	INIT	O ₇ - O ₀
	Other	A ₀ , A ₃ - A ₉	A ₁	A ₂	PGM	V _{FF}	E	V _{PP}	D ₇ - D ₀
Read		A ₀ , A ₃ - A ₉	A ₁	A ₂	X	V _{IL}	V _{IL}	V _{IH}	O ₇ - O ₀
Output Disable		A ₀ , A ₃ - A ₉	A ₁	A ₂	X	V _{IH}	X	V _{IH}	High Z
Output Disable		A ₀ , A ₃ - A ₉	A ₁	A ₂	X	X	V _{IH}	V _{IH}	High Z
Initialize		A ₀ , A ₃ - A ₉	A ₁	A ₂	X	X	V _{IL}	V _{IL}	Init Byte
Program		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Verify		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{IHP}	V _{ILP}	V _{IHP}	V _{PP}	O ₇ - O ₀
Program Inhibit		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{IHP}	V _{IHP}	V _{IHP}	V _{PP}	High Z
Intelligent Program		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Program Initialize Byte		A ₀ , A ₃ - A ₉	V _{PP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	D ₇ - D ₀
Blank Check Ones		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{PP}	V _{ILP}	V _{ILP}	V _{ILP}	Ones
Blank Check Zeros		A ₀ , A ₃ - A ₉	A ₁	A ₂	V _{PP}	V _{IHP}	V _{ILP}	V _{ILP}	Zeros

Note:

9. X = "don't care" but not to exceed V_{CC} ±5%.

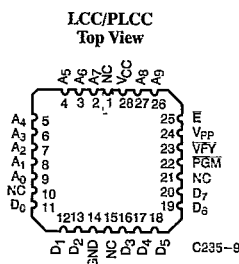
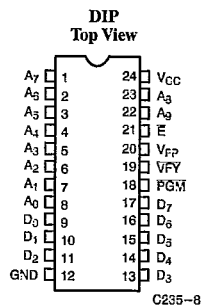
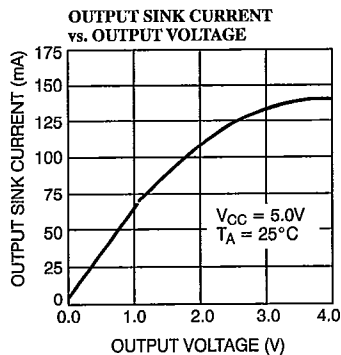
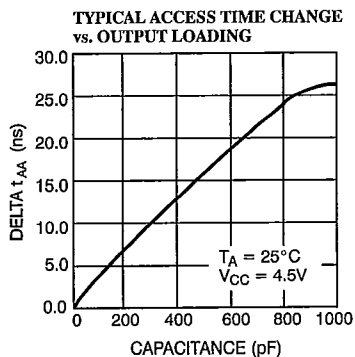
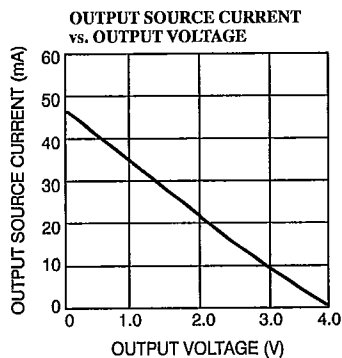
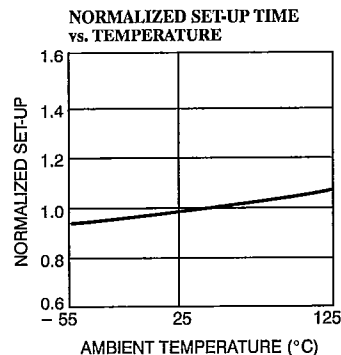
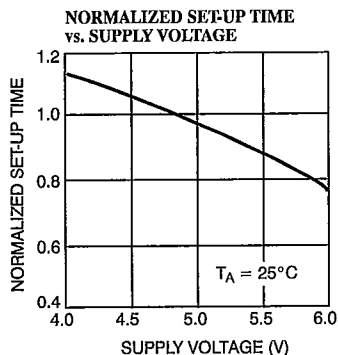
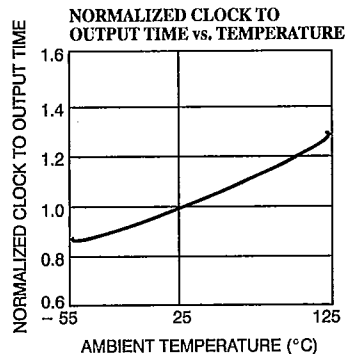
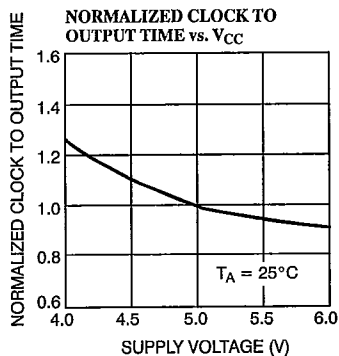
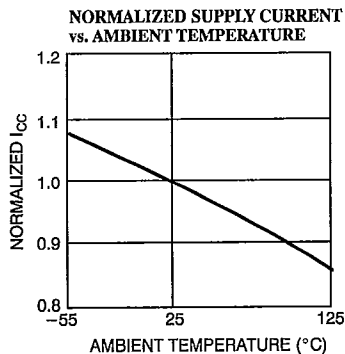
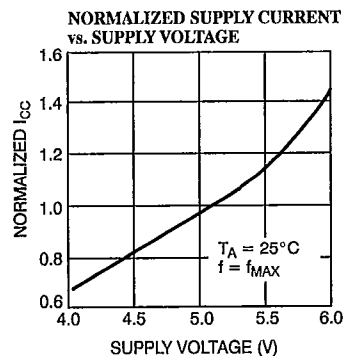


Figure 1. Programming Pinouts



Typical DC and AC Characteristics



Ordering Information^[10]

Speed (ns)		Ordering Code	Package Name	Package Type	Operating Range
t _{SA}	t _{CO}				
25	12	CY7C235-25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235-25PC	P13	24-Lead (300-Mil) Molded DIP	
30	15	CY7C235-30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235-30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235-30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235-30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235-30KMB	K73	24-Lead Rectangular Cerpack	
		CY7C235-30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235-40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235-40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235-40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235-40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235-40KMB	K73	24-Lead Rectangular Cerpack	
		CY7C235-40LMB	L64	28-Square Leadless Chip Carrier	

Note:

10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-88636	01KX	CY7C235-40KMB
5962-88636	01LX	CY7C235-40DMB
5962-88636	013X	CY7C235-40LMB
5962-88636	02KX	CY7C235-30KMB
5962-88636	02LX	CY7C235-30DMB
5962-88636	023X	CY7C235-30LMB

Document #: 38-00003-E

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T-90-20

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to Cerdip, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to

fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and Cerdips, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and Cerdip. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

Reliability

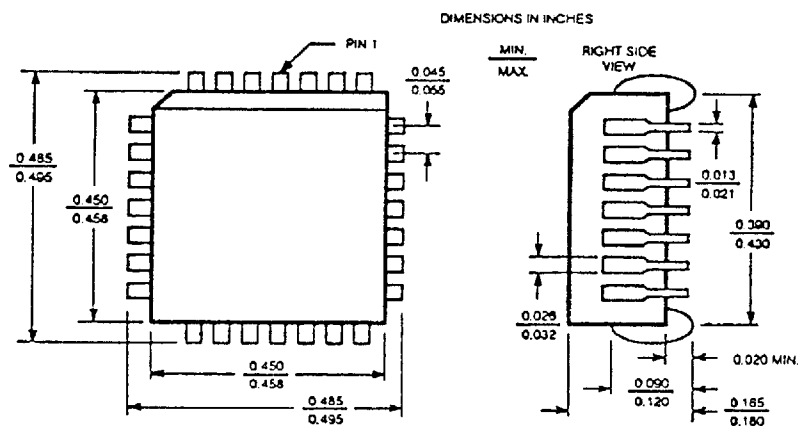
Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the



28-Lead Plastic Leaded Chip Carrier J64

T-90-20



28-Pin Ceramic Leaded Chip Carrier Y64

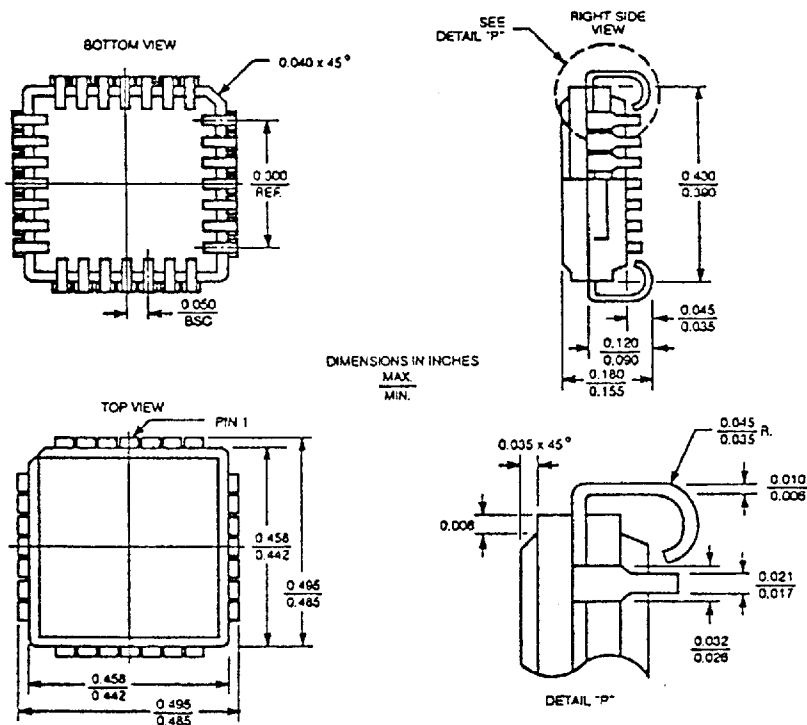


Figure 1. Diagrams of 28-Lead Chip Carriers



16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$$T_J = \Delta T + T_A$$

where

$$\Delta T = P_D \times \Theta_{JA}$$

and

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device $I_{EE} = 170$ mA max and $V_{EE} = 5.46$ V max for $P_D = 928$ mW. Add 15 mW per output for a total output $P_D = 120$ mW. Therefore, the total $P_D = 1048$ mW.

For a PLCC, $\Theta_{JA} = 45^\circ\text{C/W}$ at 500 LFPM, and $\Theta_{JA} = 64^\circ\text{C/W}$ for still air.

For a CLCC, $\Theta_{JA} = 35^\circ\text{C/W}$ at 500 LFPM, and $\Theta_{JA} = 54^\circ\text{C/W}$ for still air.

Because

$$T_J = \text{total } P_D \times \Theta_{JA} + T_A$$

and

$T_A = 75^\circ\text{C}$ worst-case commercial temperature range, for the PLCC:

$$T_J = (1.048 \text{ W})(45^\circ\text{C/W}) + 75^\circ\text{C} = 122^\circ\text{C at 500 LFPM}$$

$$T_J = (1.048 \text{ W})(64^\circ\text{C/W}) + 75^\circ\text{C} = 142^\circ\text{C in still air}$$

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use $V_{EENOM} = 5.2$ V or 4.5 V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, Figures 2 through 5 show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT .

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, Figures 2 and 3 note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE} , 50Ω loads, 500 LFPM air flow, $T_J = 64^\circ\text{C}$, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE} , 50Ω loads, 500 LFPM air flow, $T_J = 94^\circ\text{C}$, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, $T_J = 122^\circ\text{C}$, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL_{INPS} ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL_{INPS} family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

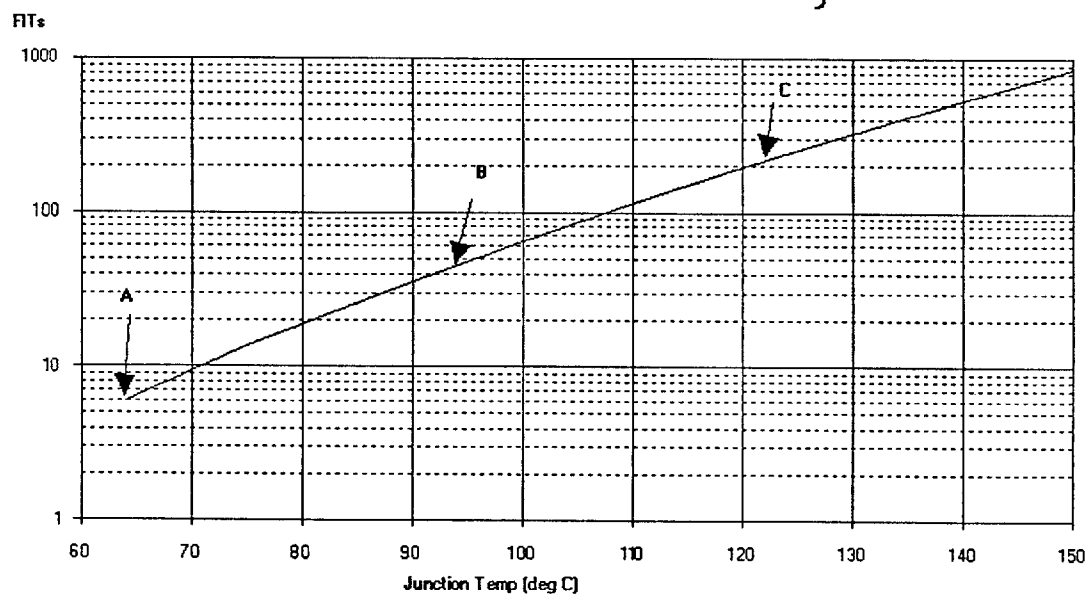
ECL PLD FITs vs. T_j 

Figure 2. Failures in Time vs Junction Temperature

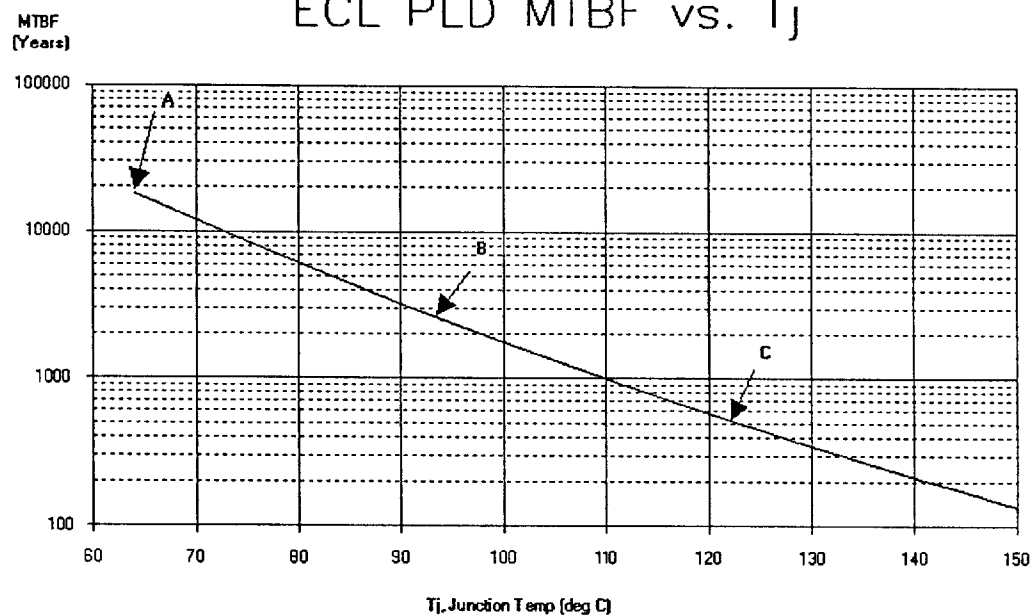
ECL PLD MTBF vs. T_j 

Figure 3. Mean Time Between Failures vs Junction Temp.

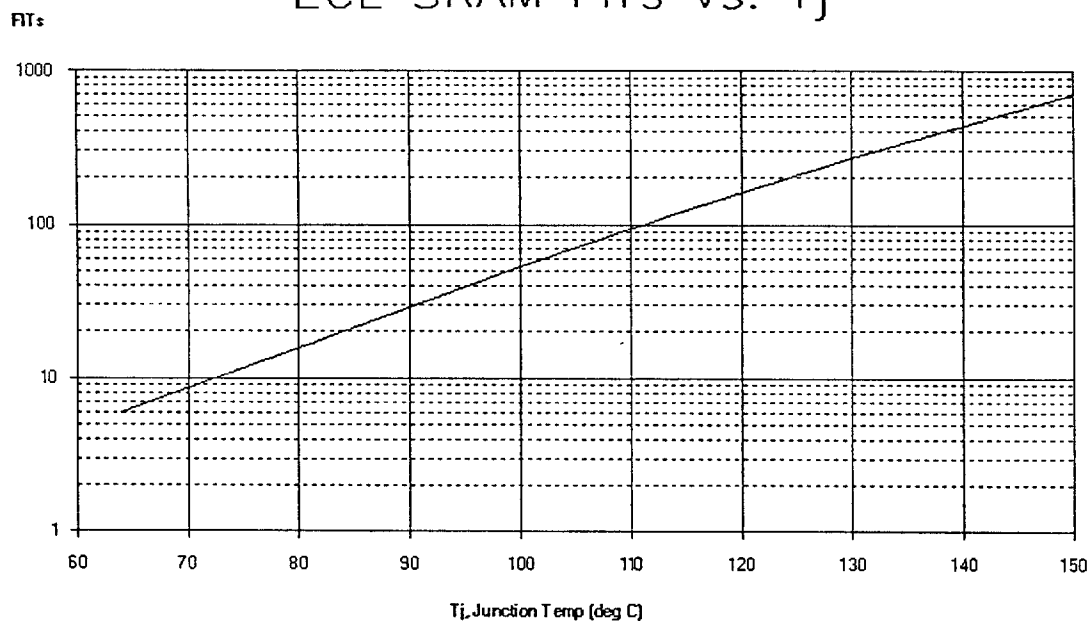
ECL SRAM FITs vs. T_j 

Figure 4. Failures in Time vs Junction Temperature

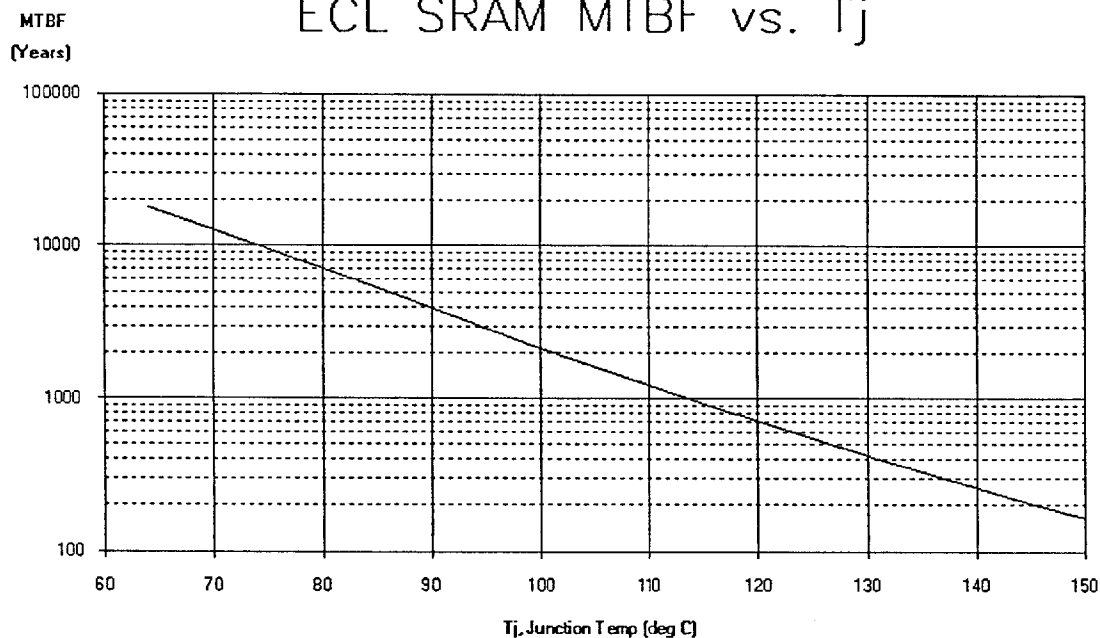
ECL SRAM MTBF vs. T_j 

Figure 5. Mean Time Between Failure vs Junction Temp.