



CYPRESS

CY7C341B

## 192-Macrocell MAX® EPLD

## Features

- 192 macrocells in 12 LABs
- 8 dedicated inputs, 64 bidirectional I/O pin
- Advanced 0.65-micron CMOS technology to increase performance
- Programmable interconnect array
- 384 expander product terms
- Available in 84-pin HLCC, PLCC, and PGA packages

## Functional Description

The CY7C341B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341B is divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341B allows them to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multifunction chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341B allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341B reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G, and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J, and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term

logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

## Logic Array Blocks

There are 12 logic array blocks in the CY7C341B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341B provide 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins that may be individually configured for input, output, or bidirectional data flow.

## Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skew among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skew or races are avoided. The result is ease of design imple-

mentation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

## Timing Delays

Timing delays within the CY7C341B may be easily determined using *Warp2™*, *Warp2+™*, or *Warp3™* software or by the model shown in Figure 1. The CY7C341B has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information, the *Warp3* software provides a timing simulator.

## Design Recommendations

For proper operation, input and output pins must be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic level (either  $V_{CC}$  or  $GND$ ). Each set of  $V_{CC}$  and  $GND$  pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2  $\mu F$  must be connected between  $V_{CC}$  and  $GND$ . For the most effective decoupling, each  $V_{CC}$  pin should be separately decoupled to  $GND$ , directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

## Design Security

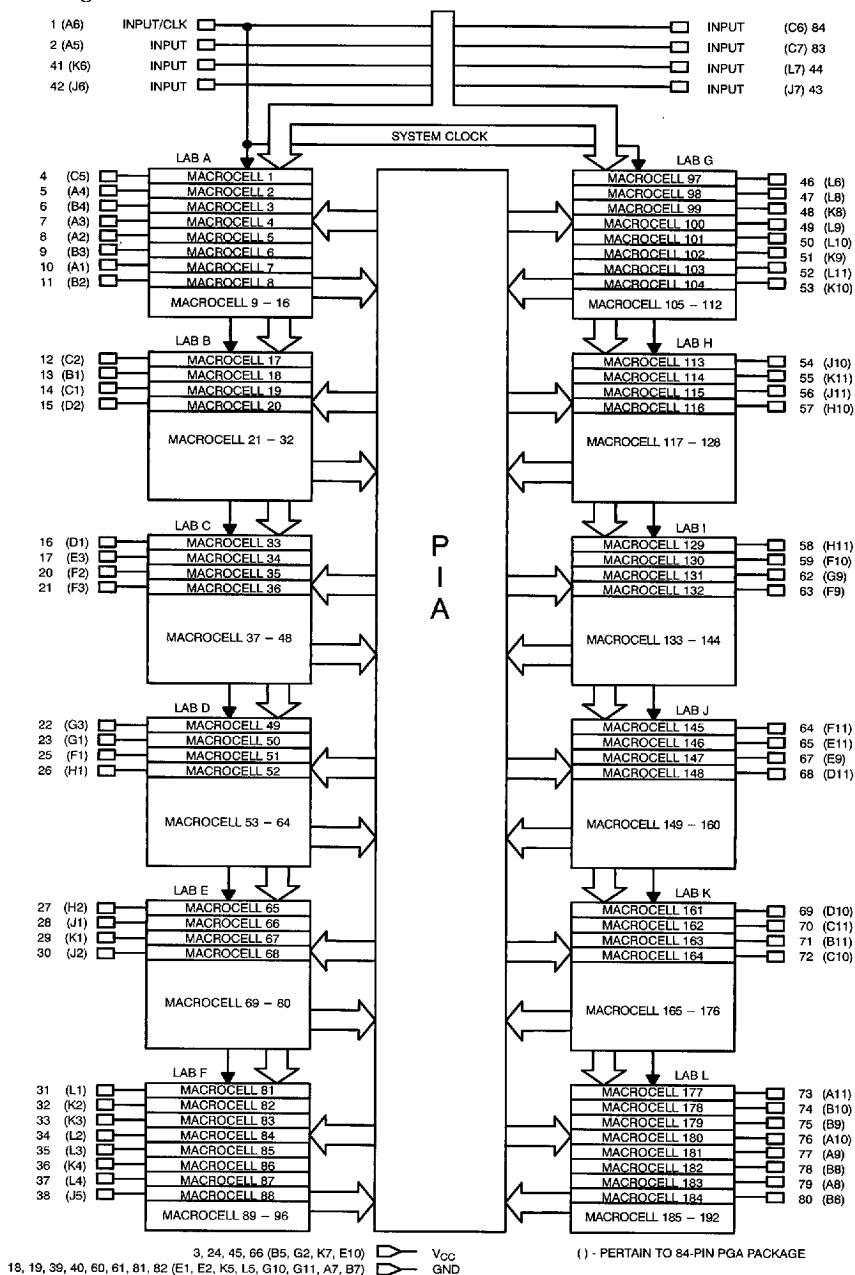
The CY7C341B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

## Selection Guide

|                                |            | 7C341B-15 | 7C341B-20 | 7C341B-25 | 7C341B-30 | 7C341B-35 |
|--------------------------------|------------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)       |            | 15        | 20        | 25        | 30        | 35        |
| Maximum Operating Current (mA) | Commercial | 380       | 380       | 380       | 380       | 380       |
|                                | Industrial | 480       | 480       | 480       | 480       | 480       |
|                                | Military   |           | 480       | 480       | 480       | 480       |
| Maximum Standby Current (mA)   | Commercial | 360       | 360       | 360       | 360       | 360       |
|                                | Industrial | 435       | 435       | 435       | 435       | 435       |
|                                | Military   |           | 435       | 435       | 435       | 435       |

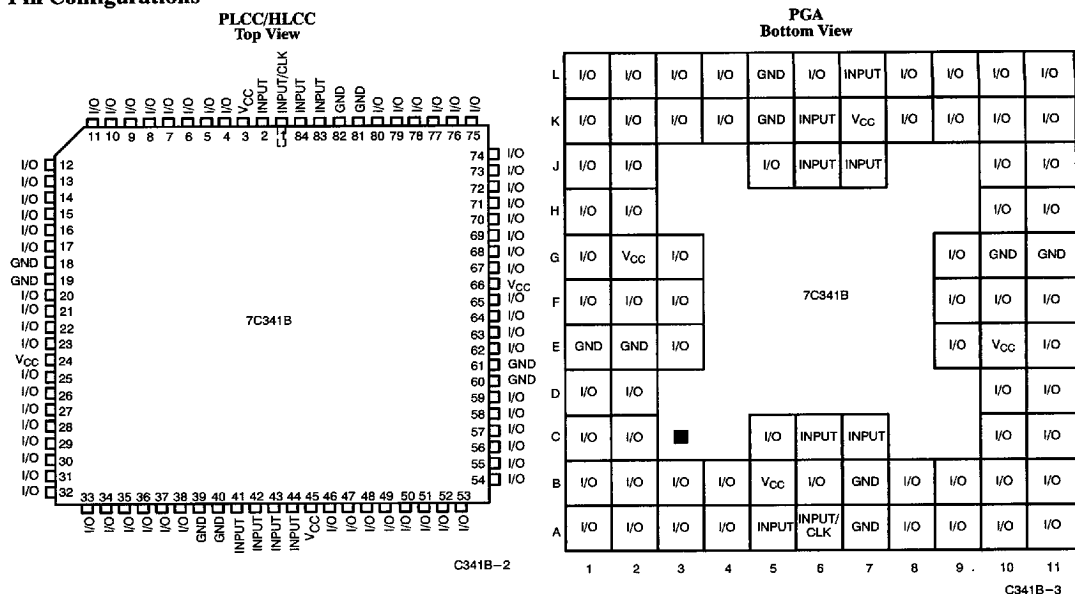
Shaded areas contain preliminary information.

MAX is a registered trademark of Altera Corporation. *Warp*, *Warp2+*, and *Warp3* are trademarks of Cypress Semiconductor Corporation.

**Logic Block Diagram**


C341B-1

## Pin Configurations



## Design Security (continued)

The CY7C341B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

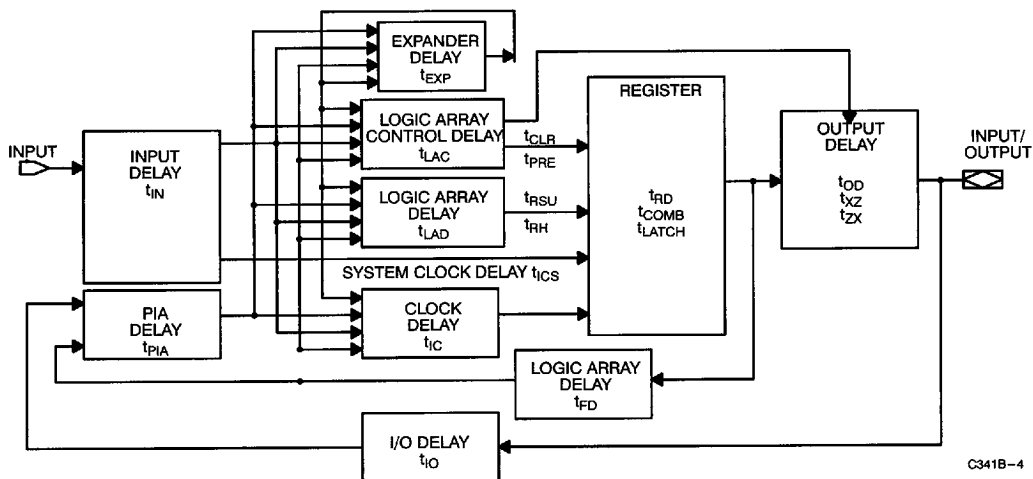


Figure 1. CY7C341B Internal Timing Model

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|                                           |                  |
|-------------------------------------------|------------------|
| Storage Temperature                       | -65°C to +150°C  |
| Ambient Temperature with Power Applied    | 0°C to +70°C     |
| Maximum Junction Temperature (Under Bias) | 150°C            |
| Supply Voltage to Ground Potential        | -2.0V to +7.0V   |
| Maximum Power Dissipation                 | 2500 mW          |
| DC $V_{CC}$ or GND Current                | 500 mA           |
| DC Output Current, per Pin                | -25 mA to +25 mA |

|                                                         |                |
|---------------------------------------------------------|----------------|
| DC Input Voltage <sup>[1]</sup>                         | -3.0V to +7.0V |
| DC Program Voltage                                      | 13.0V          |
| Static Discharge Voltage (per MIL-STD-883, method 3015) | > 1100V        |

### Operating Range

| Range      | Ambient Temperature    | $V_{CC}$     |
|------------|------------------------|--------------|
| Commercial | 0°C to +70°C           | 5V $\pm$ 5%  |
| Industrial | -40°C to +85°C         | 5V $\pm$ 10% |
| Military   | -55°C to +125°C (Case) | 5V $\pm$ 10% |

### Electrical Characteristics Over the Operating Range<sup>[2]</sup>

| Parameter           | Description                         | Test Conditions                                                  | Min.    | Max.           | Unit          |
|---------------------|-------------------------------------|------------------------------------------------------------------|---------|----------------|---------------|
| $V_{OH}$            | Output HIGH Voltage                 | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                 | 2.4     |                | V             |
| $V_{OL}$            | Output LOW Voltage                  | $V_{CC} = \text{Min.}, I_{OL} = 8 \text{ mA}$                    |         | 0.45           | V             |
| $V_{IH}$            | Input HIGH Level                    |                                                                  | 2.2     | $V_{CC} + 0.3$ | V             |
| $V_{IL}$            | Input LOW Level                     |                                                                  | -0.3    | 0.8            | V             |
| $I_{IX}$            | Input Current                       | $GND \leq V_{IN} \leq V_{CC}$                                    | -10     | +10            | $\mu\text{A}$ |
| $I_{OZ}$            | Output Leakage Current              | $V_O = V_{CC}$ or GND                                            | -40     | +40            | $\mu\text{A}$ |
| $I_{OS}$            | Output Short Circuit Current        | $V_{CC} = \text{Max.}, V_{OUT} = GND^{[3,4]}$                    | -30     | -90            | mA            |
| $I_{CC1}$           | Power Supply Current (Standby)      | $V_I = V_{CC}$ or GND (No Load)                                  | Com'l   | 360            | mA            |
|                     |                                     |                                                                  | Mil/Ind | 435            | mA            |
| $I_{CC2}$           | Power Supply Current <sup>[5]</sup> | $V_I = V_{CC}$ or GND (No Load)<br>$f = 1.0 \text{ MHz}^{[3,5]}$ | Com'l   | 380            | mA            |
|                     |                                     |                                                                  | Mil/Ind | 480            | mA            |
| $t_R$ (Recommended) | Input Rise Time                     |                                                                  |         | 100            | ns            |
| $t_F$ (Recommended) | Input Fall Time                     |                                                                  |         | 100            | ns            |

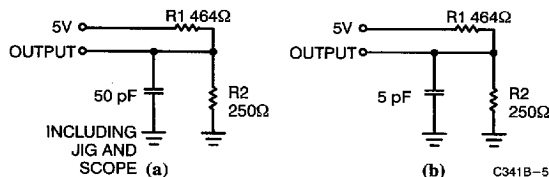
### Capacitance<sup>[6]</sup>

| Parameter | Description        | Test Conditions                                                   | Max. | Unit |
|-----------|--------------------|-------------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance  | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0\text{V}$ | 10   | pF   |
| $C_{OUT}$ | Output Capacitance |                                                                   | 20   | pF   |

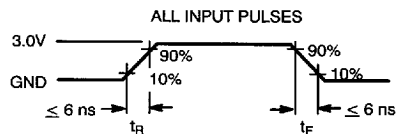
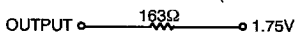
#### Notes:

1. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns.
2. Typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .
3. Guaranteed but not 100% tested.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.  $V_{OUT} = 0.5\text{V}$  has been chosen to avoid test problems caused by tester ground degradation.
5. This parameter is measured with device programmed as a 16-bit counter in each LAB and is tested periodically by sampling production material.
6. Part (a) in AC Test Load and Waveforms is used for all parameters except  $t_{ER}$  and  $t_{XZ}$ , which is used for part (b) in AC Test Load and Waveforms. All external timing parameters are measured referenced to external pins of the device.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



C341B-6

**External Synchronous Switching Characteristics Over the Operating Range<sup>[6]</sup>**

| Parameter        | Description                                                                            |       | 7C341B-15 |     | 7C341B-20 |     | 7C341B-25 |     | 7C341B-30 |     | 7C341B-35 |     | Unit |
|------------------|----------------------------------------------------------------------------------------|-------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|
|                  |                                                                                        |       | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max |      |
| t <sub>PD1</sub> | Dedicated Input to Combinatorial Output Delay <sup>[7]</sup>                           | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| t <sub>PD2</sub> | I/O Input to Combinatorial Output Delay <sup>[8]</sup>                                 | Com'l |           | 25  |           | 33  |           | 40  |           | 45  |           | 55  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 33  |           | 40  |           | 45  |           | 55  |      |
| t <sub>PD3</sub> | Dedicated Input to Combinatorial Output Delay with Expander Delay <sup>[9]</sup>       | Com'l |           | 23  |           | 30  |           | 37  |           | 44  |           | 55  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 30  |           | 37  |           | 44  |           | 55  |      |
| t <sub>PD4</sub> | I/O Input to Combinatorial Output Delay with Expander Delay <sup>[3, 10]</sup>         | Com'l |           | 33  |           | 43  |           | 52  |           | 59  |           | 75  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 43  |           | 52  |           | 59  |           | 75  |      |
| t <sub>EA</sub>  | Input to Output Enable Delay <sup>[3, 7]</sup>                                         | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| t <sub>ER</sub>  | Input to Output Disable Delay <sup>[6]</sup>                                           | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| t <sub>CO1</sub> | Synchronous Clock Input to Output Delay                                                | Com'l |           | 7   |           | 8   |           | 14  |           | 16  |           | 20  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 8   |           | 14  |           | 16  |           | 20  |      |
| t <sub>CO2</sub> | Synchronous Clock to Local Feedback to Combinatorial Output <sup>[3, 11]</sup>         | Com'l |           | 17  |           | 20  |           | 30  |           | 35  |           | 42  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 20  |           | 30  |           | 35  |           | 42  |      |
| t <sub>S1</sub>  | Dedicated Input or Feedback Set-up Time to Synchronous Clock Output <sup>[6, 12]</sup> | Com'l | 10        |     | 13        |     | 15        |     | 20        |     | 25        |     | ns   |
|                  |                                                                                        | Mil   |           |     | 13        |     | 15        |     | 20        |     | 25        |     |      |
| t <sub>S2</sub>  | I/O Input Set-up Time to Synchronous Clock Input <sup>[8]</sup>                        | Com'l | 20        |     | 24        |     | 30        |     | 39        |     | 45        |     | ns   |
|                  |                                                                                        | Mil   |           |     | 24        |     | 30        |     | 39        |     | 45        |     |      |
| t <sub>H</sub>   | Input Hold Time from Synchronous Clock Input <sup>[6]</sup>                            | Com'l | 0         |     | 0         |     | 0         |     | 0         |     | 0         |     | ns   |
|                  |                                                                                        | Mil   |           |     | 0         |     | 0         |     | 0         |     | 0         |     |      |
| t <sub>WH</sub>  | Synchronous Clock Input High Time                                                      | Com'l | 5         |     | 7         |     | 8         |     | 10        |     | 12.5      |     | ns   |
|                  |                                                                                        | Mil   |           |     | 7         |     | 8         |     | 10        |     | 12.5      |     |      |
| t <sub>WL</sub>  | Synchronous Clock Input Low Time                                                       | Com'l | 5         |     | 7         |     | 8         |     | 10        |     | 12.5      |     | ns   |
|                  |                                                                                        | Mil   |           |     | 7         |     | 8         |     | 10        |     | 12.5      |     |      |
| t <sub>RW</sub>  | Asynchronous Clear Width <sup>[3, 6]</sup>                                             | Com'l | 16        |     | 22        |     | 25        |     | 30        |     | 35        |     | ns   |
|                  |                                                                                        | Mil   |           |     | 22        |     | 25        |     | 30        |     | 35        |     |      |
| t <sub>RR</sub>  | Asynchronous Clear Recovery <sup>[3, 7]</sup>                                          | Com'l | 16        |     | 22        |     | 25        |     | 30        |     | 35        |     | ns   |
|                  |                                                                                        | Mil   |           |     | 22        |     | 25        |     | 30        |     | 35        |     |      |
| t <sub>RO</sub>  | Asynchronous Clear to Registered Output Delay <sup>[5]</sup>                           | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|                  |                                                                                        | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| t <sub>PW</sub>  | Asynchronous Preset Width <sup>[3, 6]</sup>                                            | Com'l | 15        |     | 20        |     | 25        |     | 30        |     | 35        |     | ns   |
|                  |                                                                                        | Mil   |           |     | 20        |     | 25        |     | 30        |     | 35        |     |      |

Shaded areas contain preliminary information.

**External Synchronous Switching Characteristics Over the Operating Range<sup>[6]</sup>(continued)**

| Parameter         | Description                                                                                                                                                       |       | 7C341B-15 |     | 7C341B-20 |     | 7C341B-25 |     | 7C341B-30 |     | 7C341B325 |     | Unit |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|
|                   |                                                                                                                                                                   |       | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max |      |
| t <sub>PR</sub>   | Asynchronous Preset Recovery Time <sup>[5, 6]</sup>                                                                                                               | Com'l | 15        |     | 20        |     | 25        |     | 30        |     | 35        |     | ns   |
|                   |                                                                                                                                                                   | Mil   |           |     |           |     | 25        |     | 30        |     | 35        |     |      |
| t <sub>PO</sub>   | Asynchronous Preset to Registered Output Delay <sup>[6]</sup>                                                                                                     | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|                   |                                                                                                                                                                   | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| t <sub>CF</sub>   | Synchronous Clock to Local Feedback Input <sup>[3, 13]</sup>                                                                                                      | Com'l |           | 3   |           | 3   |           | 3   |           | 3   |           | 5   | ns   |
|                   |                                                                                                                                                                   | Mil   |           |     |           | 3   |           | 3   |           | 3   |           | 5   |      |
| t <sub>P</sub>    | External Synchronous Clock Period (1/f <sub>MAX3</sub> ) <sup>[3]</sup>                                                                                           | Com'l | 12        |     | 14        |     | 16        |     | 20        |     | 25        |     | ns   |
|                   |                                                                                                                                                                   | Mil   |           |     | 14        |     | 16        |     | 20        |     | 25        |     |      |
| f <sub>MAX1</sub> | External Feedback Maximum Frequency (1/(t <sub>CO1</sub> + t <sub>S1</sub> )) <sup>[3, 14]</sup>                                                                  | Com'l | 58.8      |     | 50        |     | 34.5      |     | 27.7      |     | 22.2      |     | MHz  |
|                   |                                                                                                                                                                   | Mil   |           |     | 50        |     | 34.5      |     | 27.7      |     | 22.2      |     |      |
| f <sub>MAX2</sub> | Internal Local Feedback Maximum Frequency, lesser of (1/(t <sub>S1</sub> + t <sub>CF</sub> )) or (1/t <sub>CO1</sub> ) <sup>[3, 15]</sup>                         | Com'l | 76.9      |     | 62.5      |     | 55.5      |     | 43        |     | 33        |     | MHz  |
|                   |                                                                                                                                                                   | Mil   |           |     | 62.5      |     | 55.5      |     | 43        |     | 33        |     |      |
| f <sub>MAX3</sub> | Data Path Maximum Frequency, least of 1/(t <sub>WL</sub> + t <sub>WP1</sub> ), 1/(t <sub>S1</sub> + t <sub>H</sub> ), or (1/t <sub>CO1</sub> ) <sup>[3, 16]</sup> | Com'l | 100       |     | 71.4      |     | 62.5      |     | 50        |     | 40.0      |     | MHz  |
|                   |                                                                                                                                                                   | Mil   |           |     | 71.4      |     | 62.5      |     | 50        |     | 40.0      |     |      |
| f <sub>MAX4</sub> | Maximum Register Toggle Frequency (1/(t <sub>WL</sub> + t <sub>WH</sub> )) <sup>[3, 17]</sup>                                                                     | Com'l | 100       |     | 71.4      |     | 62.5      |     | 50        |     | 40.0      |     | MHz  |
|                   |                                                                                                                                                                   | Mil   |           |     | 71.4      |     | 62.5      |     | 50        |     | 40.0      |     |      |
| t <sub>OH</sub>   | Output Data Stable Time from Synchronous Clock Input <sup>[3, 18]</sup>                                                                                           | Com'l | 3         |     | 3         |     | 3         |     | 3         |     | 3         |     | ns   |
|                   |                                                                                                                                                                   | Mil   |           |     | 3         |     | 3         |     | 3         |     | 3         |     |      |

Shaded areas contain preliminary information.

**Notes:**

- This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function. When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic. If an input signal is applied to an I/O pin an additional delay equal to t<sub>PIA</sub> should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t<sub>EXP</sub> to the overall delay for the comparable delay without expanders.
- This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
- This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic functions and includes the worst-case expander logic delay for one pass through the expander logic.
- This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
- This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all

feedback is within the same LAB. This parameter is tested periodically by sampling production material.

- If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t<sub>S2</sub> for synchronous operation and t<sub>AS2</sub> for asynchronous operation.
- This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t<sub>S1</sub>, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
- This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
- This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than 1/t<sub>CO1</sub>.

**External Asynchronous Switching Characteristics Over the Operating Range<sup>[6]</sup> (continued)**

| Parameter   | Description                                                                                       |       | 7C341B-15 |     | 7C341B-20 |     | 7C341B-25 |     | 7C341B-30 |     | 7C341B-35 |     | Unit |
|-------------|---------------------------------------------------------------------------------------------------|-------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|
|             |                                                                                                   |       | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max |      |
| $t_{ACO1}$  | Dedicated Asynchronous Clock Input to Output Delay <sup>[6]</sup>                                 | Com'l |           | 15  |           | 20  |           | 25  |           | 30  |           | 35  | ns   |
|             |                                                                                                   | Mil   |           |     |           | 20  |           | 25  |           | 30  |           | 35  |      |
| $t_{ACO2}$  | Asynchronous Clock Input to Local Feedback to Combinatorial Output <sup>[19]</sup>                | Com'l |           | 25  |           | 32  |           | 40  |           | 46  |           | 55  | ns   |
|             |                                                                                                   | Mil   |           |     |           | 32  |           | 40  |           | 46  |           | 55  |      |
| $t_{AS1}$   | Dedicated Input or Feedback Set-up Time to Asynchronous Clock Input <sup>[6]</sup>                | Com'l | 5         |     | 5         |     | 5         |     | 6         |     | 8         |     | ns   |
|             |                                                                                                   | Mil   |           |     | 5         |     | 5         |     | 6         |     | 8         |     |      |
| $t_{AS2}$   | I/O Input Set-Up Time to Asynchronous Clock Input <sup>[6]</sup>                                  | Com'l | 14        |     | 18        |     | 20        |     | 27        |     | 30        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 18        |     | 20        |     | 27        |     | 30        |     |      |
| $t_{AH}$    | Input Hold Time from Asynchronous Clock Input <sup>[6]</sup>                                      | Com'l | 5         |     | 6         |     | 6         |     | 8         |     | 10        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 6         |     | 6         |     | 8         |     | 10        |     |      |
| $t_{AWH}$   | Asynchronous Clock Input HIGH Time <sup>[6]</sup>                                                 | Com'l | 9         |     | 10        |     | 11        |     | 14        |     | 16        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 10        |     | 11        |     | 14        |     | 16        |     |      |
| $t_{AWL}$   | Asynchronous Clock Input LOW Time <sup>[6, 20]</sup>                                              | Com'l | 7         |     | 8         |     | 9         |     | 11        |     | 14        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 8         |     | 9         |     | 11        |     | 14        |     |      |
| $t_{ACF}$   | Asynchronous Clock to Local Feedback Input <sup>[21]</sup>                                        | Com'l |           | 11  |           | 13  |           | 15  |           | 18  |           | 22  | ns   |
|             |                                                                                                   | Mil   |           |     |           | 13  |           | 15  |           | 18  |           | 22  |      |
| $t_{AP}$    | External Asynchronous Clock Period ( $1/f_{MAX4}$ )                                               | Com'l | 16        |     | 18        |     | 20        |     | 25        |     | 30        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 18        |     | 20        |     | 25        |     | 30        |     |      |
| $f_{MAXA1}$ | External Feedback Maximum Frequency in Asynchronous Mode $1/(t_{ACO1} + t_{AS1})$ <sup>[22]</sup> | Com'l | 50        |     | 40        |     | 33.3      |     | 27        |     | 23        |     | MHz  |
|             |                                                                                                   | Mil   |           |     | 40        |     | 33.3      |     | 27        |     | 23        |     |      |
| $f_{MAXA2}$ | Maximum Internal Asynchronous Frequency <sup>[23]</sup>                                           | Com'l | 62.5      |     | 55.5      |     | 50        |     | 40        |     | 33.3      |     | MHz  |
|             |                                                                                                   | Mil   |           |     | 55.5      |     | 50        |     | 40        |     | 33.3      |     |      |
| $f_{MAXA3}$ | Data Path Maximum Frequency in Asynchronous Mode <sup>[24]</sup>                                  | Com'l | 62.5      |     | 50        |     | 40        |     | 33.3      |     | 28.5      |     | MHz  |
|             |                                                                                                   | Mil   |           |     | 50        |     | 40        |     | 33.3      |     | 28.5      |     |      |
| $f_{MAXA4}$ | Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$ <sup>[25]</sup>            | Com'l | 62.5      |     | 55.5      |     | 50        |     | 40        |     | 33.3      |     | MHz  |
|             |                                                                                                   | Mil   |           |     | 55.5      |     | 50        |     | 40        |     | 33.3      |     |      |
| $t_{AOH}$   | Output Data Stable Time from Asynchronous Clock Input <sup>[26]</sup>                             | Com'l | 15        |     | 15        |     | 15        |     | 15        |     | 15        |     | ns   |
|             |                                                                                                   | Mil   |           |     | 15        |     | 15        |     | 15        |     | 15        |     |      |

Shaded areas contain preliminary information.

**Notes:**

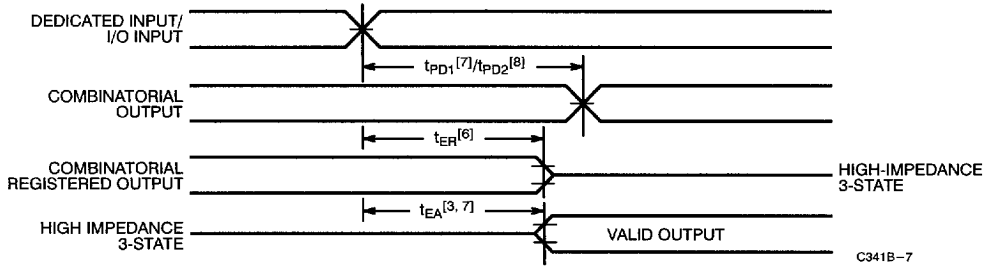
16. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins,  $t_{S2}$  is the appropriate  $t_S$  for calculation.
17. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycle by a clock signal applied to the dedicated clock input pin.
18. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.
19. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the

dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.

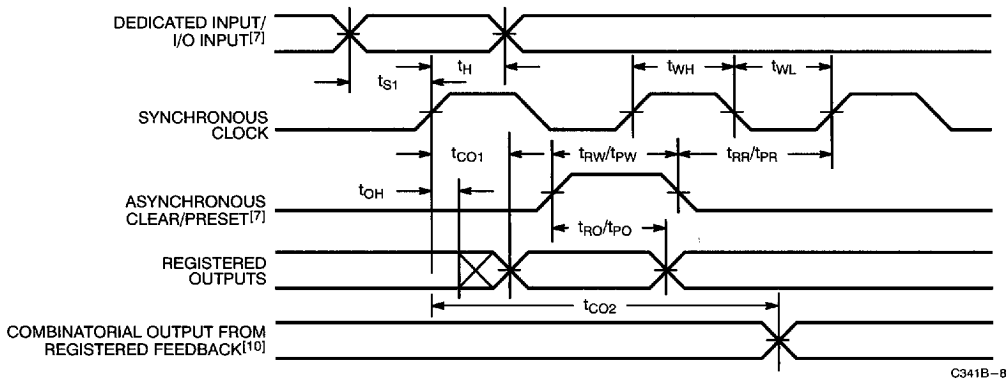
20. This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge triggering, the  $t_{AWH}$  and  $t_{AWL}$  parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity,  $t_{AWH}$  should be used for both  $t_{AWH}$  and  $t_{AWL}$ .
21. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register set-up time,  $t_{AS1}$ , is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, and assumes there is no expander logic in the clock path and the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.

## Switching Waveforms

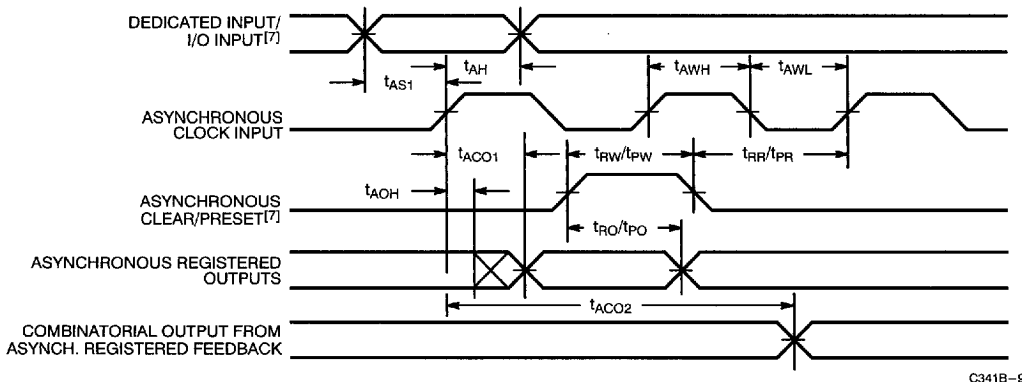
### External Combinatorial



### External Synchronous



### External Asynchronous



**Internal Switching Characteristics Over the Operating Range<sup>[2]</sup>**

| Parameter   | Description                                               |       | 7C341B-15 |     | 7C341B-20 |     | 7C341B-25 |     | 7C341B-30 |     | 7C341B-35 |     | Unit |
|-------------|-----------------------------------------------------------|-------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|
|             |                                                           |       | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max |      |
| $t_{IN}$    | Dedicated Input Pad and Buffer Delay                      | Com'l |           | 3   |           | 4   |           | 5   |           | 7   |           | 9   | ns   |
|             |                                                           | Mil   |           |     |           | 4   |           | 5   |           | 7   |           | 9   |      |
| $t_{IO}$    | I/O Input Pad and Buffer Delay                            | Com'l |           | 3   |           | 4   |           | 6   |           | 6   |           | 9   | ns   |
|             |                                                           | Mil   |           |     |           | 4   |           | 6   |           | 6   |           | 9   |      |
| $t_{EXP}$   | Expander Array Delay                                      | Com'l |           | 8   |           | 10  |           | 12  |           | 14  |           | 20  | ns   |
|             |                                                           | Mil   |           |     |           | 10  |           | 12  |           | 14  |           | 20  |      |
| $t_{LAD}$   | Logic Array Data Delay                                    | Com'l |           | 8   |           | 10  |           | 12  |           | 14  |           | 16  | ns   |
|             |                                                           | Mil   |           |     |           | 10  |           | 12  |           | 14  |           | 16  |      |
| $t_{LAC}$   | Logic Array Control Delay                                 | Com'l |           | 5   |           | 7   |           | 10  |           | 12  |           | 13  | ns   |
|             |                                                           | Mil   |           |     |           | 7   |           | 10  |           | 12  |           | 13  |      |
| $t_{OD}$    | Output Buffer and Pad Delay                               | Com'l |           | 3   |           | 3   |           | 5   |           | 5   |           | 6   | ns   |
|             |                                                           | Mil   |           |     |           | 3   |           | 5   |           | 5   |           | 6   |      |
| $t_{ZX}$    | Output Buffer Enable Delay <sup>[27]</sup>                | Com'l |           | 5   |           | 5   |           | 10  |           | 11  |           | 13  | ns   |
|             |                                                           | Mil   |           |     |           | 5   |           | 10  |           | 11  |           | 13  |      |
| $t_{XZ}$    | Output Buffer Disable Delay                               | Com'l |           | 5   |           | 5   |           | 10  |           | 11  |           | 13  | ns   |
|             |                                                           | Mil   |           |     |           | 5   |           | 10  |           | 11  |           | 13  |      |
| $t_{RSU}$   | Register Set-Up Time Relative to Clock Signal at Register | Com'l | 4         |     | 5         |     | 6         |     | 8         |     | 10        |     | ns   |
|             |                                                           | Mil   |           |     | 5         |     | 6         |     | 8         |     | 10        |     |      |
| $t_{RH}$    | Register Hold Time Relative to Clock Signal at Register   | Com'l | 4         |     | 5         |     | 6         |     | 8         |     | 10        |     | ns   |
|             |                                                           | Mil   |           |     | 5         |     | 6         |     | 8         |     | 10        |     |      |
| $t_{LATCH}$ | Flow-Through Latch Delay                                  | Com'l |           | 1   |           | 2   |           | 3   |           | 4   |           | 4   | ns   |
|             |                                                           | Mil   |           |     |           | 2   |           | 3   |           | 4   |           | 4   |      |
| $t_{RD}$    | Register Delay                                            | Com'l |           | 1   |           | 1   |           | 1   |           | 2   |           | 2   | ns   |
|             |                                                           | Mil   |           |     |           | 1   |           | 1   |           | 2   |           | 2   |      |
| $t_{COMB}$  | Transparent Mode Delay <sup>[28]</sup>                    | Com'l |           | 1   |           | 2   |           | 3   |           | 4   |           | 4   | ns   |
|             |                                                           | Mil   |           |     |           | 2   |           | 3   |           | 4   |           | 4   |      |
| $t_{CH}$    | Clock High Time                                           | Com'l | 4         |     | 6         |     | 8         |     | 10        |     | 12.5      |     | ns   |
|             |                                                           | Mil   |           |     | 6         |     | 8         |     | 10        |     | 12.5      |     |      |
| $t_{CL}$    | Clock Low Time                                            | Com'l | 4         |     | 6         |     | 8         |     | 10        |     | 12.5      |     | ns   |
|             |                                                           | Mil   |           |     | 6         |     | 8         |     | 10        |     | 12.5      |     |      |

Shaded areas contain preliminary information.

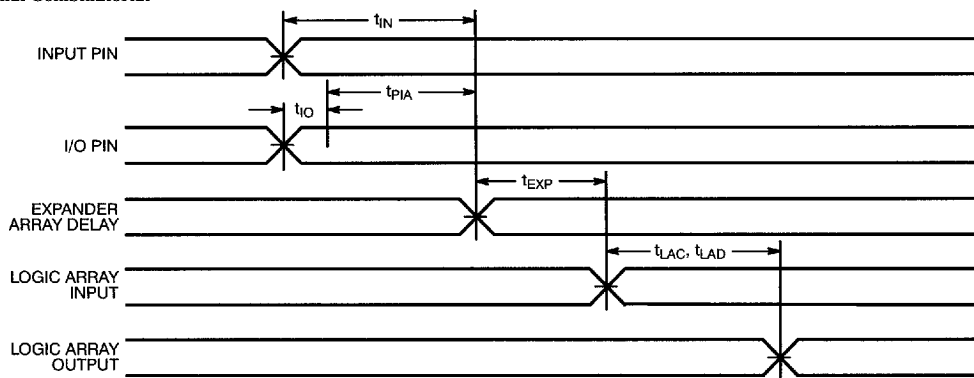
**Notes:**

22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of  $(1/t_{ACF} + t_{AS1})$  or  $(1/(t_{AWH} + t_{AWL}))$ . If register output states must also control external points, this frequency can still be observed as long as this frequency is less than  $1/t_{ACQ1}$ .
24. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of  $1/(t_{AWH} + t_{AWL})$ ,  $1/(t_{AS1} + t_{AH})$  or  $1/t_{ACQ1}$ . It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.
27. Sample tested only for an output change of 500 mV.
28. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

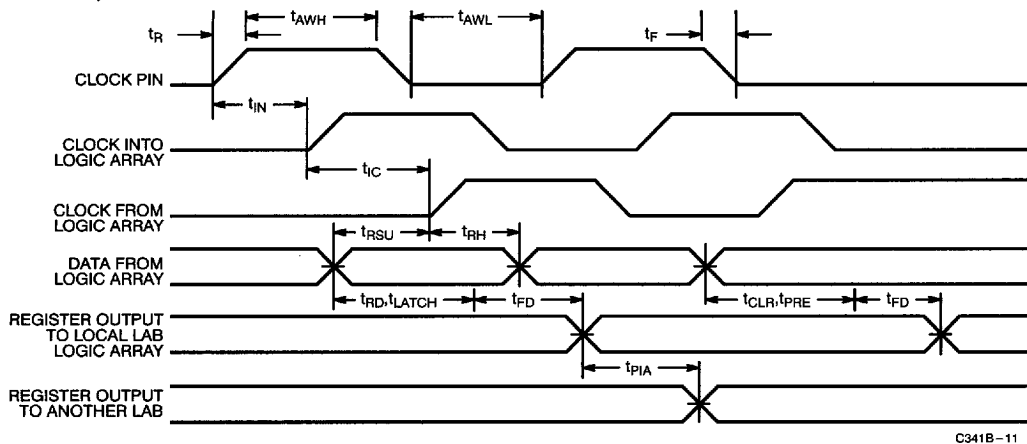
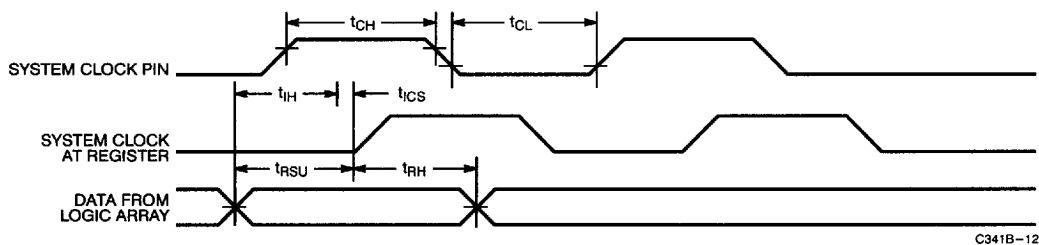
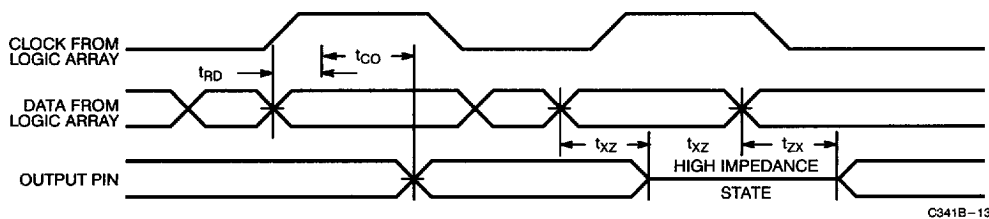
**Internal Switching Characteristics Over the Operating Range<sup>[2]</sup>**

| Parameter | Description                                 |       | 7C341B-15 |     | 7C341B-20 |     | 7C341B-25 |     | 7C341B-30 |     | 7C341B-35 |     | Unit |
|-----------|---------------------------------------------|-------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|
|           |                                             |       | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max | Min.      | Max |      |
| $t_{IC}$  | Asynchronous Clock Logic Delay              | Com'l |           | 6   |           | 8   |           | 14  |           | 16  |           | 18  | ns   |
|           |                                             | Mil   |           |     |           | 8   |           | 14  |           | 16  |           | 18  |      |
| $t_{ICS}$ | Synchronous Clock Delay                     | Com'l |           | 0.5 |           | 0.5 |           | 2   |           | 2   |           | 3   | ns   |
|           |                                             | Mil   |           |     |           | 0.5 |           | 2   |           | 2   |           | 3   |      |
| $t_{FD}$  | Feedback Delay                              | Com'l |           | 1   |           | 1   |           | 1   |           | 1   |           | 2   | ns   |
|           |                                             | Mil   |           |     |           | 1   |           | 1   |           | 1   |           | 2   |      |
| $t_{PRE}$ | Asynchronous Register Preset Time           | Com'l |           | 3   |           | 3   |           | 5   |           | 6   |           | 7   | ns   |
|           |                                             | Mil   |           |     |           | 3   |           | 5   |           | 6   |           | 7   |      |
| $t_{CLR}$ | Asynchronous Register Clear Time            | Com'l |           | 3   |           | 3   |           | 5   |           | 6   |           | 7   | ns   |
|           |                                             | Mil   |           |     |           | 3   |           | 5   |           | 6   |           | 7   |      |
| $t_{PCW}$ | Asynchronous Preset and Clear Pulse Width   | Com'l | 3         |     | 4         |     | 5         |     | 6         |     | 7         |     | ns   |
|           |                                             | Mil   |           |     | 4         |     | 5         |     | 6         |     | 7         |     |      |
| $t_{PCR}$ | Asynchronous Preset and Clear Recovery Time | Com'l | 3         |     | 4         |     | 5         |     | 6         |     | 7         |     | ns   |
|           |                                             | Mil   |           |     | 4         |     | 5         |     | 6         |     | 7         |     |      |
| $t_{PIA}$ | Programmable Interconnect Array Delay       | Com'l |           | 10  |           | 12  |           | 14  |           | 16  |           | 20  | ns   |
|           |                                             | Mil   |           |     |           |     |           |     |           | 16  |           | 20  |      |

Shaded areas contain preliminary information.

**Switching Waveforms**
**Internal Combinatorial**


C341B-10

**Switching Waveforms (continued)**
**Internal Asynchronous**

**Internal Synchronous**

**Internal Synchronous**




## Ordering Information

| Speed (ns) | Ordering Code    | Package Name | Package Type                         | Operating Range       |
|------------|------------------|--------------|--------------------------------------|-----------------------|
| 15         | CY7C341B-15HC/HI | H84          | 84-Lead Windowed Leaded Chip Carrier | Commercial/Industrial |
|            | CY7C341B-15JC/JI | J83          | 84-Lead Plastic Leaded Chip Carrier  |                       |
|            | CY7C341B-15RC/RI | R84          | 84-Lead Windowed Pin Grid Array      |                       |
| 20         | CY7C341B-20HC/HI | H84          | 84-Lead Windowed Leaded Chip Carrier | Commercial/Industrial |
|            | CY7C341B-20JC/JI | J83          | 84-Lead Plastic Leaded Chip Carrier  |                       |
|            | CY7C341B-20RC/RI | R84          | 84-Lead Windowed Pin Grid Array      |                       |
|            | CY7C341B-20HMB   | H84          | 84-Lead Windowed Leaded Chip Carrier | Military              |
|            | CY7C341B-20RMB   | R84          | 84-Lead Windowed Pin Grid Array      |                       |
|            |                  |              |                                      |                       |
| 25         | CY7C341B-25HC/HI | H84          | 84-Lead Windowed Leaded Chip Carrier | Commercial/Industrial |
|            | CY7C341B-25JC/JI | J83          | 84-Lead Plastic Leaded Chip Carrier  |                       |
|            | CY7C341B-25RC/RI | R84          | 84-Lead Windowed Pin Grid Array      |                       |
|            | CY7C341B-25HMB   | H84          | 84-Lead Windowed Leaded Chip Carrier | Military              |
|            | CY7C341B-25RMB   | R84          | 84-Lead Windowed Pin Grid Array      |                       |
| 30         | CY7C341B-30HC/HI | H84          | 84-Lead Windowed Leaded Chip Carrier | Commercial/Industrial |
|            | CY7C341B-30JC/JI | J83          | 84-Lead Plastic Leaded Chip Carrier  |                       |
|            | CY7C341B-30RC/RI | R84          | 84-Lead Windowed Pin Grid Array      |                       |
|            | CY7C341B-30HMB   | H84          | 84-Lead Windowed Leaded Chip Carrier | Military              |
|            | CY7C341B-30RMB   | R84          | 84-Lead Windowed Pin Grid Array      |                       |
| 35         | CY7C341B-35HC/HI | H84          | 84-Lead Windowed Leaded Chip Carrier | Commercial/Industrial |
|            | CY7C341B-35JC/JI | J83          | 84-Lead Plastic Leaded Chip Carrier  |                       |
|            | CY7C341B-35RC/RI | R84          | 84-Lead Windowed Pin Grid Array      |                       |
|            | CY7C341B-35HMB   | H84          | 84-Lead Windowed Leaded Chip Carrier | Military              |
|            | CY7C341B-35RMB   | R84          | 84-Lead Windowed Pin Grid Array      |                       |

Shaded areas contain preliminary information.

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

## DC Characteristics

| Parameter        | Subgroups |
|------------------|-----------|
| V <sub>OH</sub>  | 1, 2, 3   |
| V <sub>OL</sub>  | 1, 2, 3   |
| V <sub>IH</sub>  | 1, 2, 3   |
| V <sub>IL</sub>  | 1, 2, 3   |
| I <sub>IX</sub>  | 1, 2, 3   |
| I <sub>OZ</sub>  | 1, 2, 3   |
| I <sub>CC1</sub> | 1, 2, 3   |

## Switching Characteristics

| Parameter         | Subgroups       |
|-------------------|-----------------|
| t <sub>PD1</sub>  | 7, 8, 9, 10, 11 |
| t <sub>PD2</sub>  | 7, 8, 9, 10, 11 |
| t <sub>PD3</sub>  | 7, 8, 9, 10, 11 |
| t <sub>CO1</sub>  | 7, 8, 9, 10, 11 |
| t <sub>S1</sub>   | 7, 8, 9, 10, 11 |
| t <sub>H</sub>    | 7, 8, 9, 10, 11 |
| t <sub>ACO1</sub> | 7, 8, 9, 10, 11 |
| t <sub>ACO2</sub> | 7, 8, 9, 10, 11 |
| t <sub>AS1</sub>  | 7, 8, 9, 10, 11 |
| t <sub>AH</sub>   | 7, 8, 9, 10, 11 |

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