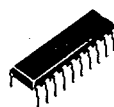


LC74HC373



3021B

CMOS High-Speed Standard Logic
LC74HC Series

Octal 3-State Noninverting D-Type Transparent Latch

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Features

- The LC74HC373 consists of 8 identical noninverting latches with 3-state outputs. The latch enable input (LE) and output control input (OC) are common to 8 latches. When the latch enable input (LE) goes low, the data is latched. When the output control input (OC) is high, the outputs are in the high impedance state.
- Uses CMOS structure to provide such features as wide operating voltage range (2 to 6V), low power dissipation, and high noise margin.
- The LC74HC373 is functionally as well as pin-out compatible with the 74LS-TTL (74HC373) and uses silicon gate process technology to achieve operating speeds similar to LS-TTL (74LS373).
- All inputs are protected from damage.

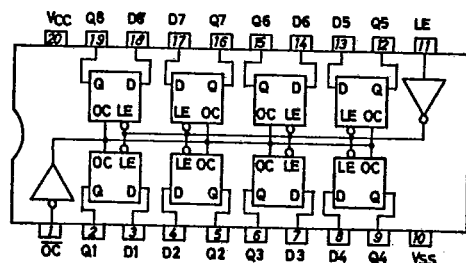
Absolute Maximum Ratings at $T_a=25^{\circ}\text{C} \pm 2^{\circ}\text{C}$, $V_{SS}=0\text{V}$

Maximum Supply Voltage	$V_{CC\text{max}}$	$V_{SS}-0.5$ to $V_{SS}+7.0$	V
Maximum Input Voltage	$V_{IN\text{max}}$	$V_{SS}-0.5$ to $V_{CC}+0.5$	V
Maximum Output Voltage	$V_{OUT\text{max}}$	$V_{SS}-0.5$ to $V_{CC}+0.5$	V
Maximum Output Current	I_{OUT}		Per output
Current Dissipation	I_{CC}/I_{GND}	± 35	mA
Clamp Diode Current	I_K	± 70	mA
Allowable Power	$P_{d\text{max}}$	± 20	mA
Dissipation		500	mW
Storage Temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Lead Temperature and Time	T_{sol}	300	$^{\circ}\text{C}$
		$t=10\text{sec}$	

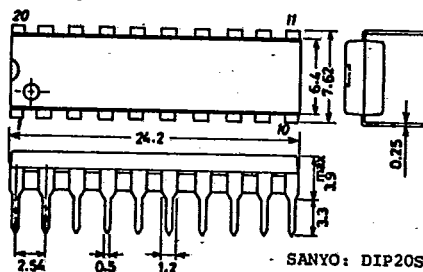
Allowable Operating Conditions at $V_{SS}=0\text{V}$

Supply Voltage	V_{CC}	2.0 to 6.0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Output Voltage	V_{OUT}	0 to V_{CC}	V
Operating Temperature	T_{opg}	-40 to +85	$^{\circ}\text{C}$
Input Rise/Fall Time	t_r, t_f	0 to 500	ns

Pin Assignment(top view)



Case Outline 3021B-D20SIC (unit:mm)



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Truth Table

Input			Output	Operation
$\overline{OC}$	LE	D	Q	
0	1	0	0	
0	1	1	1	
0	0	X	Qn	Latch
1	X	X	Z	3-state

0: "L" level Qn: Level of Q output before steady-state

1: "H" level input conditions were established

X: Don't Care

Z: 3-state

Electrical Characteristics at $T_a=25^{\circ}\text{C} \pm 2^{\circ}\text{C}$, $V_{SS}=0\text{V}$ "H"-Level Input Voltage V_{IH}

V_{CC}	min	typ	max	unit
2.0	1.5			V
4.5	3.15			V
5.0	3.5			V
5.5	3.85			V
6.0	4.2			V

"L"-Level Input Voltage V_{IL}

2.0			0.6	V
4.5			1.35	V
5.0			1.5	V
5.5			1.65	V
6.0			1.8	V

"H"-Level Output Voltage V_{OH} $I_{OH}=-20\mu\text{A}$

4.5	4.4	4.5		V
5.0	4.9	5.0		V
5.5	5.4	5.5		V

"L"-Level Output Voltage V_{OL} $I_{OL}=20\mu\text{A}$

4.5		0.0	0.1	V
5.0		0.0	0.1	V
5.5		0.0	0.1	V

Input Current I_{IN}

6.0			± 0.3	μA
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Quiescent Current I_{CC}

6.0			1.0	μA
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Electrical Characteristics at $T_a=-40^{\circ}\text{C}$, $V_{SS}=0\text{V}$ "H"-Level Input Voltage V_{IH}

V_{CC}	min	typ	max	unit
2.0	1.5			V
4.5	3.15			V
5.0	3.5			V
5.5	3.85			V
6.0	4.2			V

"L"-Level Input Voltage V_{IL}

2.0			0.6	V
4.5			1.35	V
5.0			1.5	V
5.5			1.65	V
6.0			1.8	V

"H"-Level Output Voltage V_{OH} $I_{OH}=-20\mu\text{A}$

4.5	4.4			V
5.0	4.9			V
5.5	5.4			V

"L"-Level Output Voltage V_{OL} $I_{OL}=20\mu\text{A}$

4.5			0.1	V
5.0			0.1	V
5.5			0.1	V

Input Current I_{IN}

6.0			± 0.3	μA
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Quiescent Current I_{CC}

6.0			1.0	μA
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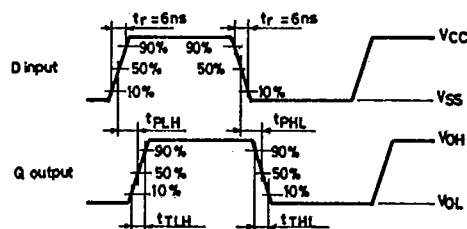
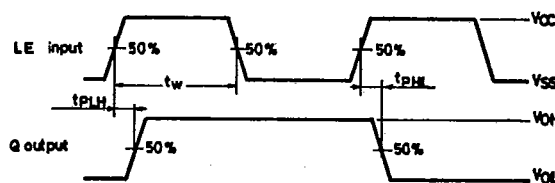
Electrical Characteristics at $T_a=+85^{\circ}\text{C}$, $V_{SS}=0\text{V}$

		V_{CC}	min	typ	max	unit
"H"-Level Input Voltage V_{IH}		2.0	1.5			V
		4.5	3.15			V
		5.0	3.5			V
		5.5	3.85			V
		6.0	4.2			V
"L"-Level Input Voltage V_{IL}		2.0		0.6		V
		4.5		1.35		V
		5.0		1.5		V
		5.5		1.65		V
		6.0		1.8		V
"H"-Level Output Voltage V_{OH} $I_{OH}=-20\mu\text{A}$		4.5	4.4			V
		5.0	4.9			V
		5.5	5.4			V
"L"-Level Output Voltage V_{OL} $I_{OL}=20\mu\text{A}$		4.5		0.1		V
		5.0		0.1		V
		5.5		0.1		V
Input Current I_{IN}		6.0		± 1.0		μA
Quiescent Current I_{CC}		6.0		10.0		μA

Switching Characteristics at $T_a=25\pm 2^{\circ}\text{C}$, $V_{SS}=0\text{V}$, Input: $t_r, t_f=6\text{n}$

		V_{CC}	min	typ	max	unit
Output Rise Time	t_{TLH} $C_L=50\text{pF}$	5.0		8	15	ns
Output Fall Time	t_{THL} $C_L=50\text{pF}$	5.0		8	15	ns
"H"-Level Propagation Delay Time(D $\rightarrow$ Q)	t_{PLH} $C_L=50\text{pF}$	5.0		20	30	ns
"L"-Level Propagation Delay Time(D $\rightarrow$ Q)	t_{PHL} $C_L=50\text{pF}$	5.0		20	30	ns
"H"-Level Propagation Delay Time(LE $\rightarrow$ Q)	t_{PLH} $C_L=50\text{pF}$	5.0		25	35	ns
"L"-Level Propagation Delay Time(LE $\rightarrow$ Q)	t_{PHL} $C_L=50\text{pF}$	5.0		25	35	ns
Output Disabling Time($\overline{\text{OC}}\rightarrow\text{Q}$)	t_{PHZ} $C_L=50\text{pF}, R_L=1\text{kohm}$	5.0		25	35	ns
Output Disabling Time($\text{OC}\rightarrow\text{Q}$)	t_{PLZ} $C_L=50\text{pF}, R_L=1\text{kohm}$	5.0		25	35	ns
Output Enabling Time($\overline{\text{OC}}\rightarrow\text{Q}$)	t_{PZH} $C_L=50\text{pF}, R_L=1\text{kohm}$	5.0		25	35	ns
Output Enabling Time($\text{OC}\rightarrow\text{Q}$)	t_{PZL} $C_L=50\text{pF}, R_L=1\text{kohm}$	5.0		25	35	ns
Minimum Setup Time	t_s	5.0		10	20	ns
Minimum Hold Time	t_h	5.0		0	5	ns
Minimum Pulse Width(LE Input)	t_w	5.0		8	15	ns
Input Capacitance	C_{in}			5	10	pF

Switching Waveforms

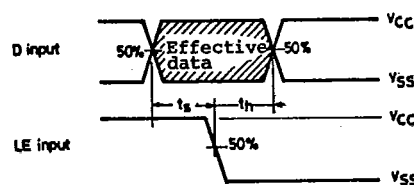
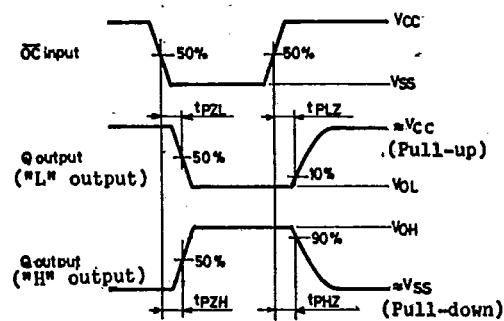
(1) D input $\rightarrow$ Q output(2) LE Input $\rightarrow$ Q output

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(3) $\overline{OC}$ input $\rightarrow$ Q output(4) t_s, t_h **Test Circuits (Load)**(1) $t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}$ (2) t_{PZL}, t_{PLZ} (3) t_{PZH}, t_{PHZ} 