



UltraLogic™ 64-Macrocell Flash CPLD

Features

- 64 macrocells in four logic blocks
- 32 I/O pins
- 5 dedicated inputs including 2 clock pins
- In-System Reprogrammable (ISR™) Flash technology
 - JTAG interface
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
 - $f_{MAX} = 125 \text{ MHz}$
 - $t_{PD} = 10 \text{ ns}$
 - $t_S = 5.5 \text{ ns}$
 - $t_{CO} = 6.5 \text{ ns}$
- Fully PCI compliant
- 3.3V or 5.0V I/O operation
- Available in 44-pin PLCC, TQFP, and CLCC packages
- Pin compatible with the CY7C371i

Functional Description

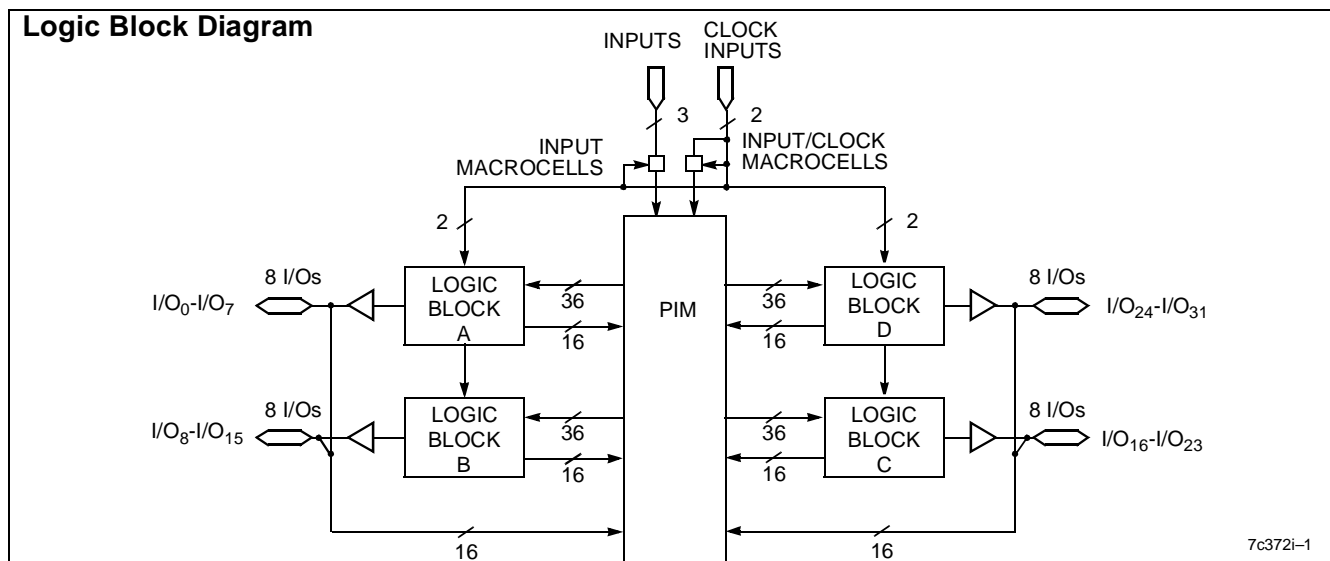
The CY7C372i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the

FLASH370i™ family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C372i is designed to bring the ease of use and high performance of the 22V10, as well as PCI Local Bus Specification support, to high-density CPLDs.

Like all of the UltraLogic™ FLASH370i devices, the CY7C372i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pins. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 64 macrocells in the CY7C372i are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.



Selection Guide

	7C372i-125	7C372i-100	7C372i-83	7C372iL-83	7C372i-66	7C372iL-66
Maximum Propagation Delay ^[1] , t_{PD} (ns)	10	12	15	15	20	20
Minimum Set-up, t_S (ns)	5.5	6.0	8	8	10	10
Maximum Clock to Output ^[1] , t_{CO} (ns)	6.5	6.5	8	8	10	10
Typical Supply Current, I_{CC} (mA)	75	75	75	45	75	45

Note:

1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when $V_{CCIO} = 3.3V$.

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

3.3V or 5.0V I/O operation

The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of V_{CC} pins: one set, V_{CCINT} , for internal operation and input buffers, and another set, V_{CCIO} , for I/O output drivers. V_{CCINT} pins must always be connected to a 5.0V power supply. However, the V_{CCIO} pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When V_{CCIO} pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When V_{CCIO} pins are connected to a 3.3V source, the input voltage levels are compatible with both 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

ducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C372i is available from Cypress's *Warp*™, *Warp Professional*™, and *Warp Enterprise*™ software packages. Please refer to the data sheets on these products for more details. Cypress also actively supports almost all third-party design tools. Please refer to third-party tool support for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied.....	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State.....	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Program Voltage.....	12.5V
Output Current into Outputs	16 mA
Static Discharge Voltage	>2001V (per MIL–STD–883, Method 3015)
Latch-Up Current.....	>200 mA

Operating Range

Range	Ambient Temperature	V_{CC} V_{CCINT}	V_{CCIO}
Commercial	0°C to +70°C	5V ± 0.25V	5V ± 0.25V OR 3.3V ± 0.3V
Industrial	–40°C to +85°C	5V ± 0.5V	5V ± 0.5V OR 3.3V ± 0.3V
Military ^[2]	–55°C to +125°C	5V ± 0.5V	

Note:

- T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -3.2 mA (Com'I/Ind) ^[5]	2.4			V
			I _{OH} = -2.0 mA (Mil)	2.4			V
V _{OHZ}	Output HIGH Voltage with Output Disabled ^[8]	V _{CC} = Max.	I _{OH} = 0 μ A (Com'I/Ind) ^[5, 6]			4.0	V
			I _{OH} = -50 μ A (Com'I/Ind) ^[5, 6]			3.6	V
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 16 mA (Com'I/Ind) ^[5]			0.5	V
			I _{OL} = 12 mA (Mil)			0.5	V
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs ^[7]		2.0		7.0	V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs ^[7]		-0.5		0.8	V
I _{IX}	Input Load Current	V _I = Internal GND, V _I = V _{CC}		-10		+10	μ A
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _O = GND or V _O = V _{CC} , Output Disabled		-50		+50	μ A
		V _{CC} = Max., V _O = 3.3V, Output Disabled ^[6]		0	-70	-125	μ A
I _{OS}	Output Short Circuit Current ^[8, 9]	V _{CC} = Max., V _{OUT} = 0.5V		-30		-160	mA
I _{CC}	Power Supply Current ^[10]	V _{CC} = Max., I _{OUT} = 0 mA, f = 1 MHz, V _{IN} = GND, V _{CC}	Com'I/Ind.		75	125	mA
			Com'I "L" -66		45	75	mA
			Military		75	200	mA
I _{BHL}	Input Bus Hold LOW Sustaining Current	V _{CC} = Min., V _{IL} = 0.8V		+75			μ A
I _{BHH}	Input Bus Hold HIGH Sustaining Current	V _{CC} = Min., V _{IH} = 2.0V		-75			μ A
I _{BHLO}	Input Bus Hold LOW Overdrive Current	V _{CC} = Max.				+500	μ A
I _{BHHO}	Input Bus Hold HIGH Overdrive Current	V _{CC} = Max.				-500	μ A

Capacitance^[9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C _{I/O} ^[11, 12]	Input Capacitance	V _{IN} = 5.0V at f = 1 MHz		8	pF
C _{CLK}	Clock Signal Capacitance	V _{IN} = 5.0V at f = 1 MHz	5	12	pF

Inductance^[9]

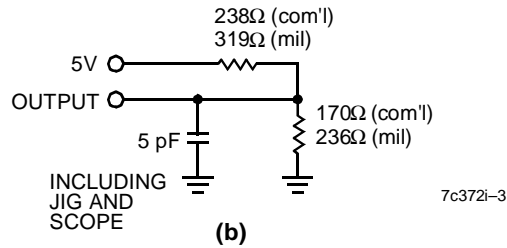
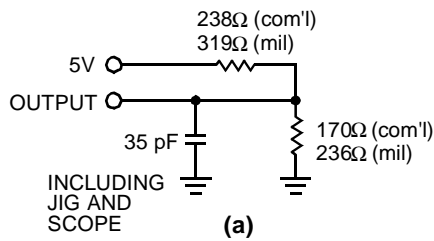
Parameter	Description	Test Conditions	44-Lead CLCC	44-Lead PLCC	Unit
L	Maximum Pin Inductance	V _{IN} = 5.0V at f = 1 MHz	2	5	nH

Notes:

- See the last page of this specification for Group A subgroup testing information.
- If V_{CCIO} is not specified, the device can be operating in either 3.3V or 5V I/O mode; V_{CC}=V_{CCINT}.
- For SDO: I_{OH} = -2 mA, I_{OL} = 2 mA.
- When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.
- Measured with 16-bit counter programmed into each logic block.
- C_{I/O} for dedicated Inputs, and for I/O pins with JTAG functionality is 12 pF Max., and for ISR_{EN} is 15pF Max.
- C_{I/O} for CLCC package is 15 pF Max.

Endurance Characteristics^[9]

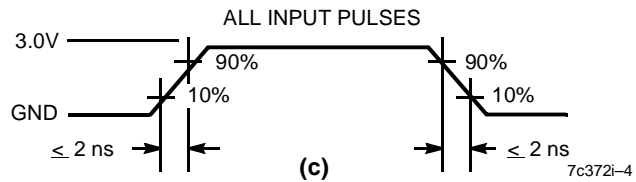
Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

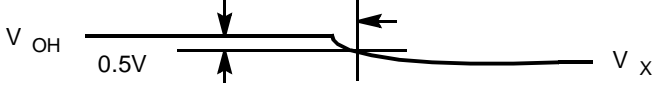
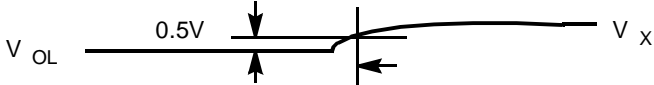
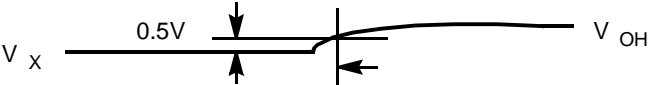
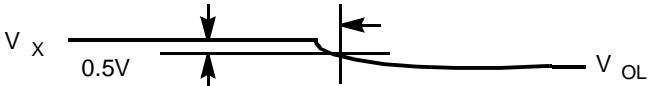
AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

99Ω (com'l) 2.08V (com'l)
136Ω (mil) 2.13V (mil)

OUTPUT



Parameter ^[13]	V _x	Output Waveform Measurement Level
t _{ER(-)}	1.5V	
t _{ER(+)}	2.6V	
t _{EA(+)}	1.5V	
t _{EA(-)}	V _{the}	

(d) Test Waveforms

Note:

13. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range^[14]

Parameter	Description	7C372i-125		7C372i-100		7C372i-83 7C372iL-83		7C372i-66 7C372iL-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t _{PD}	Input to Combinatorial Output ^[1]		10		12		15		20	ns
t _{PDL}	Input to Output Through Transparent Input or Output Latch ^[1]		13		15		18		22	ns
t _{PDLL}	Input to Output Through Transparent Input and Output Latches ^[1]		15		16		19		24	ns
t _{EA}	Input to Output Enable ^[1]		14		16		19		24	ns
t _{ER}	Input to Output Disable		14		16		19		24	ns
Input Registered/Latched Mode Parameters										
t _{WL}	Clock or Latch Enable Input LOW Time ^[9]	3		3		4		5		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[9]	3		3		4		5		ns
t _{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t _{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t _{ICO}	Input Register Clock or Latch Enable to Combinatorial Output ^[1]		14		16		19		24	ns
t _{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch ^[1]		16		18		21		26	ns
Output Registered/Latched Mode Parameters										
t _{CO}	Clock or Latch Enable to Output ^[1]		6.5		6.5		8		10	ns
t _S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns
t _H	Register or Latch Data Hold Time	0		0		0		0		ns
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array) ^[1]		14		16		19		24	ns
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	10		12		15		20		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f _{MAX1}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[9]	125		100		83		66		MHz
f _{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO}) ^[9]	153.8		153.8		125		100		MHz
f _{MAX3}	Maximum Frequency with External Feedback (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH})) ^[9]	83.3		80		62.5		50		MHz
t _{OH} -t _{IH} 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x ^[9, 15]	0		0		0		0		ns

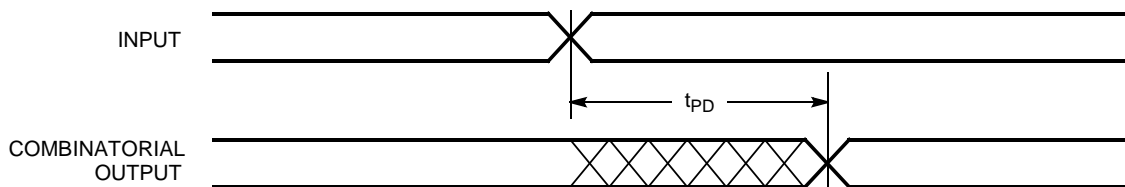
Notes:

14. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.

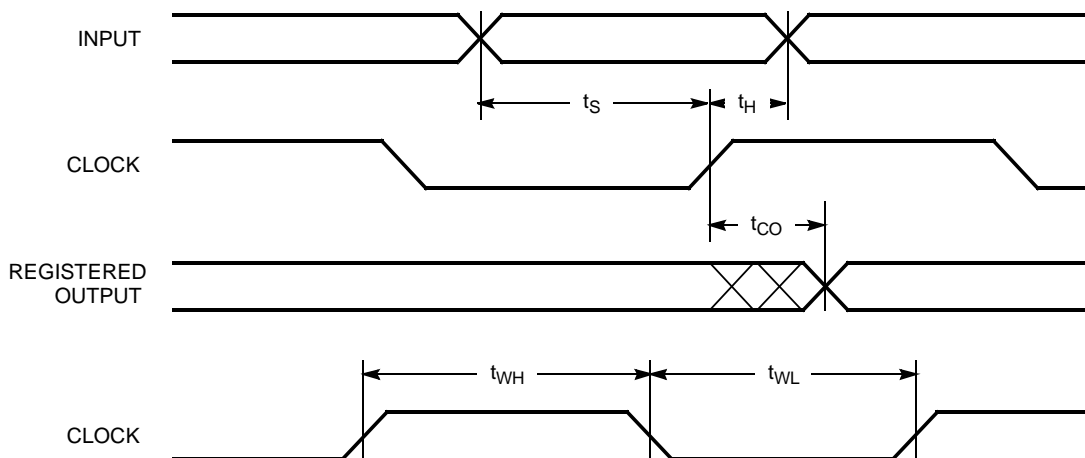
15. This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C372i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

Switching Characteristics Over the Operating Range^[14] (continued)

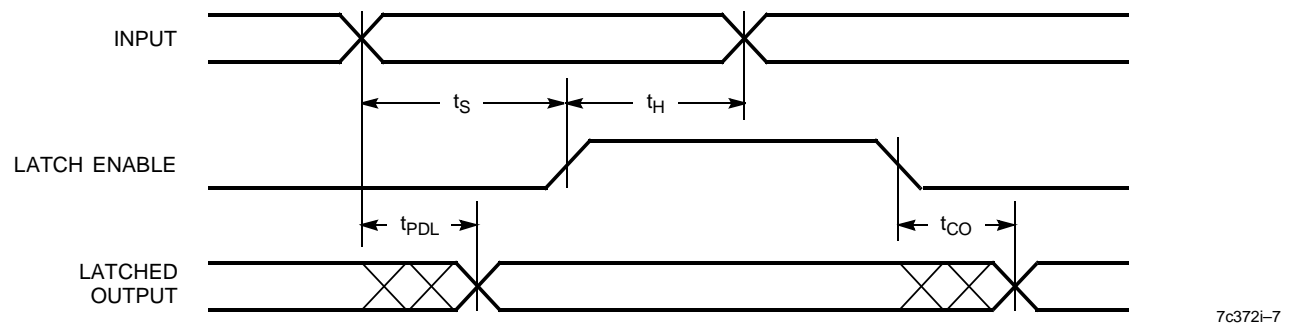
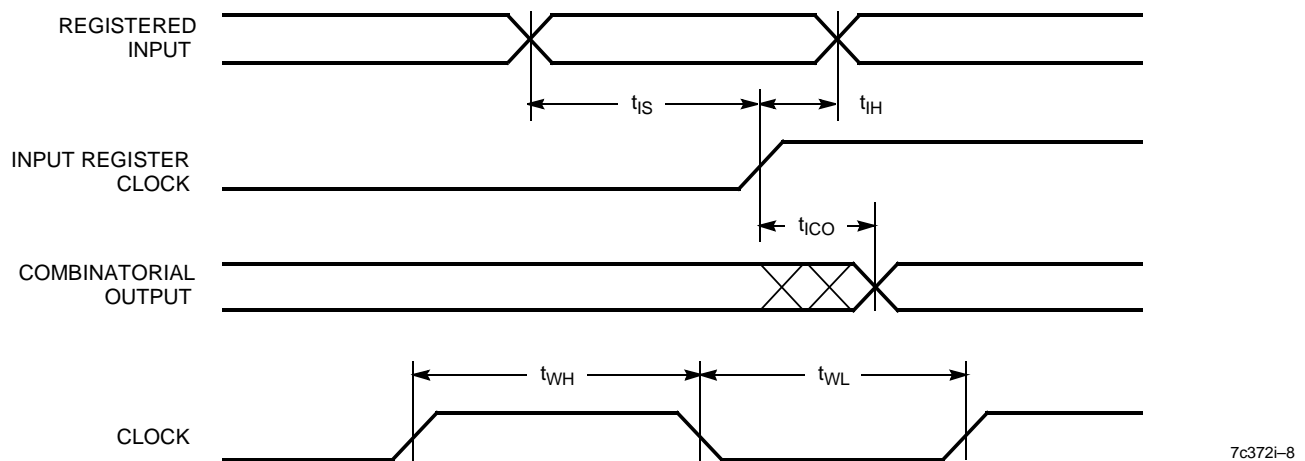
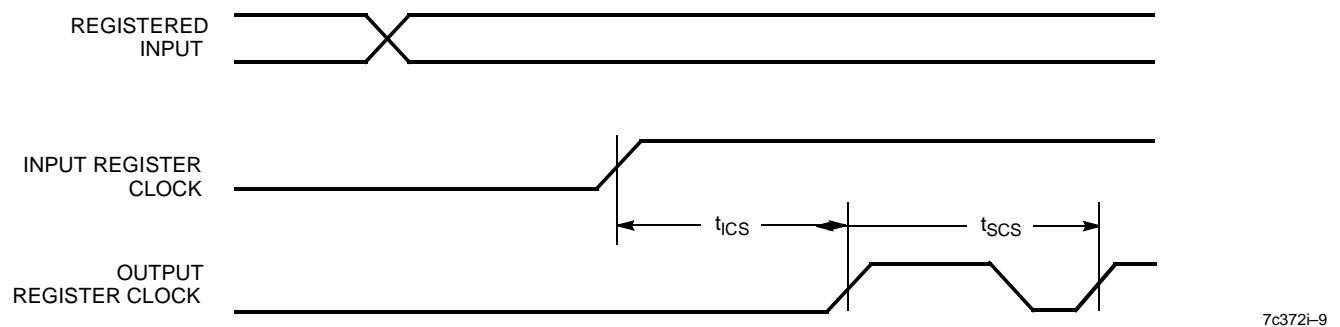
Parameter	Description	7C372i-125		7C372i-100		7C372i-83 7C372iL-83		7C372i-66 7C372iL-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipelined Mode Parameters										
t _{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f _{MAX4}	Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}), or 1/t _{SCS}) ^[9]	125		100		83.3		66.6		MHz
Reset/Preset Parameters										
t _{RW}	Asynchronous Reset Width ^[9]	10		12		15		20		ns
t _{RR}	Asynchronous Reset Recovery Time ^[9]	12		14		17		22		ns
t _{RO}	Asynchronous Reset to Output ^[1]		16		18		21		26	ns
t _{PW}	Asynchronous Preset Width ^[9]	10		12		15		20		ns
t _{PR}	Asynchronous Preset Recovery Time ^[9]	12		14		17		22		ns
t _{PO}	Asynchronous Preset to Output ^[1]		16		18		21		26	ns
Tap Controller Parameter										
f _{TAP}	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mode Parameters										
t _{3,3IO}	3.3V I/O Mode Timing Adder		1		1		1		1	ns

Switching Waveforms
Combinatorial Output


7c372i-5

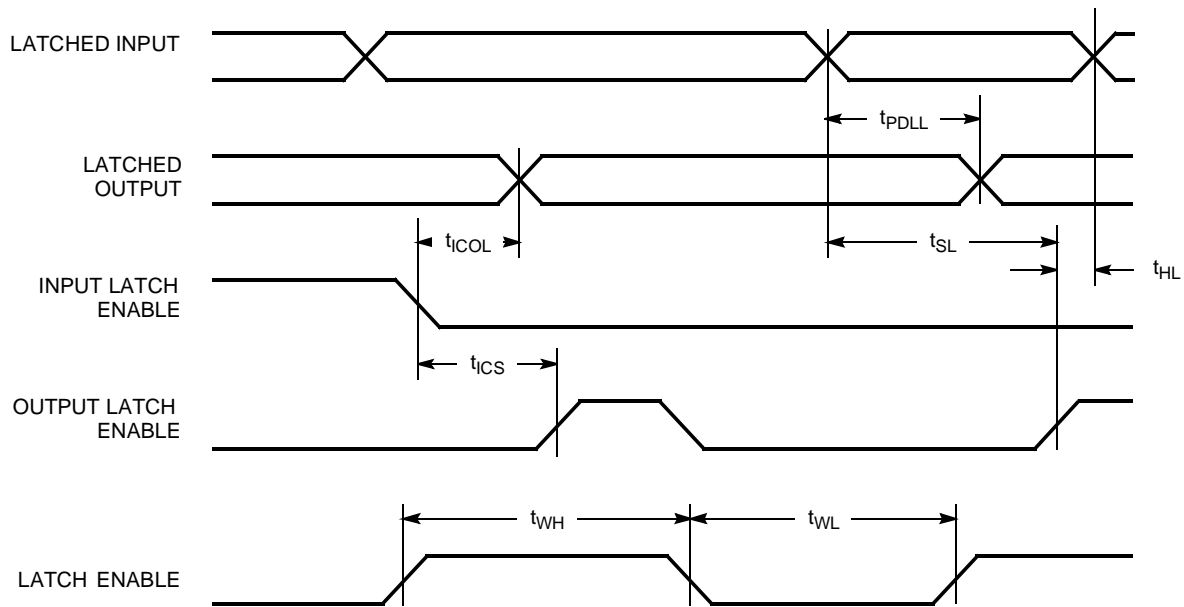
Registered Output


7c372i-6

Switching Waveforms (continued)
Latched Output

Registered Input

Clock to Clock


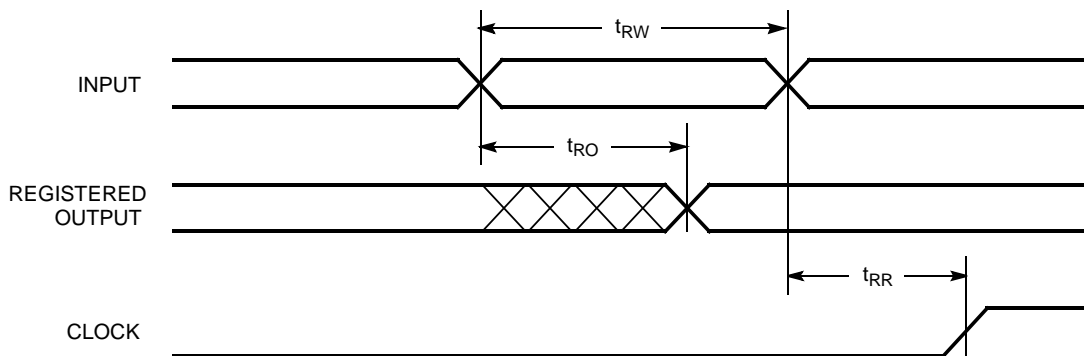
Switching Waveforms (continued)

Latched Input and Output



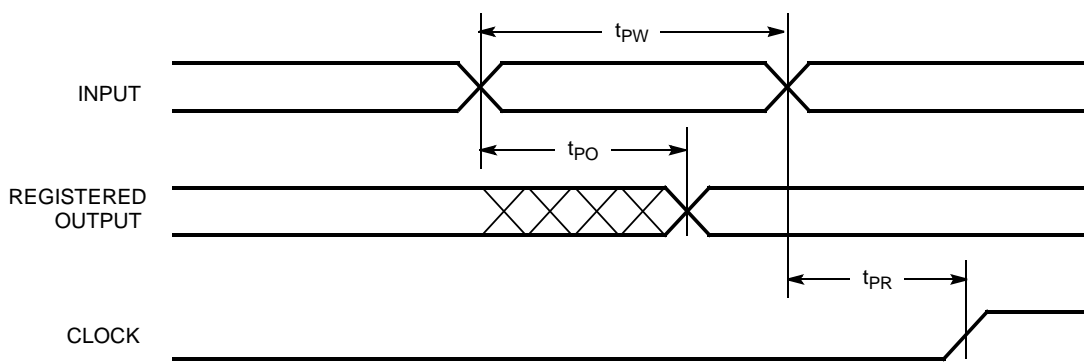
7c372i-11

Asynchronous Reset



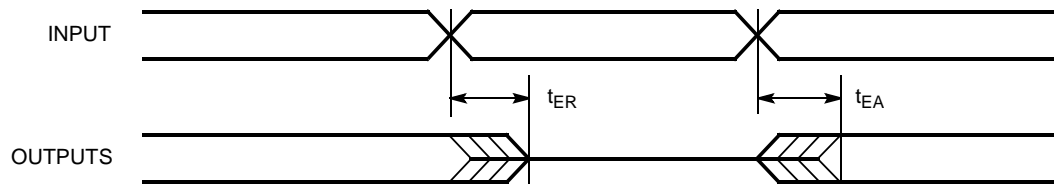
7c372i-12

Asynchronous Preset



7c372i-13

Switching Waveforms (continued)

Output Enable/Disable


7c372i-15

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C372i-125JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
100	CY7C372i-100JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372i-100JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
83	CY7C372i-83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372i-83JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C372i-83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
83	CY7C372iL-83JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
66	CY7C372i-66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C372i-66JI	J67	44-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C372i-66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C372iL-66JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

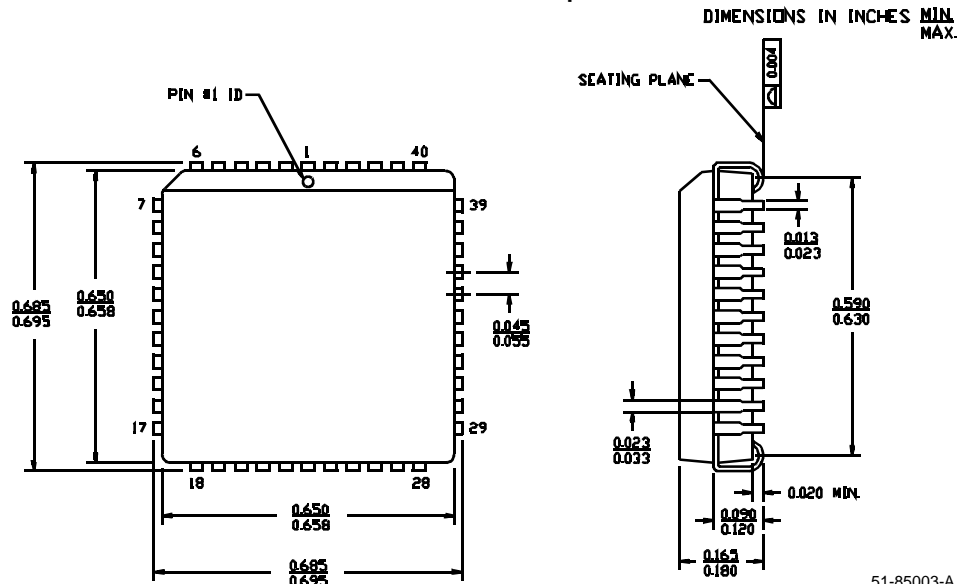
Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Document #: 38-00498-F

ISR, UltraLogic, FLASH370, FLASH370i, *Warp*, *Warp* Professional, and *Warp* Enterprise, are trademarks of Cypress Semiconductor Corporation.

Package Diagrams

44-Lead Plastic Leaded Chip Carrier J67



44-P in Ceramic Leaded Chip Carrier Y67

