PRELIMINARY

CY7C373

CYPRESS SEMICONDUCTOR

64-Macrocell Flash PLD

Features

- **64 macrocells in four logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **No hidden delays**
- **High speed**
  - **— t_{PD} = 12 ns**
  - **— t_S = 9 ns**
  - **— t_{CO} = 9 ns**
- **Electrically alterable Flash technology**
- **Available in 84-pin PLCC, CLCC, and CPGA packages**
- **Pin compatible with the CY7C374**

Functional Description

The CY7C373 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C373 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 64 macrocells in the CY7C373 are divided between four logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C373 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 64 I/O pins on the CY7C373. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C373 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C373 remain the same.

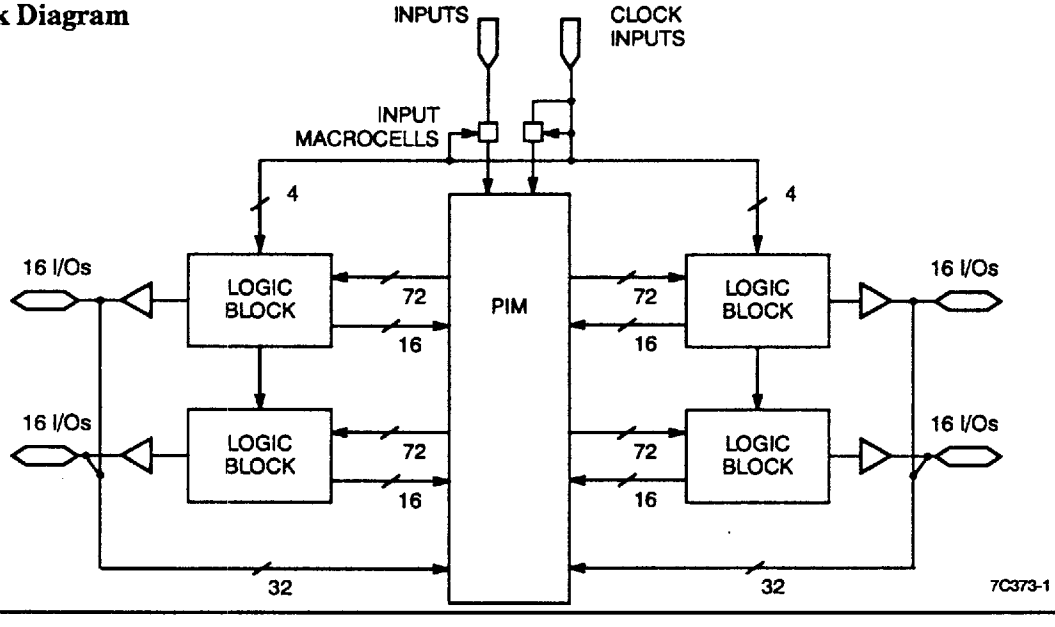
Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C373 includes four logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Logic Block Diagram



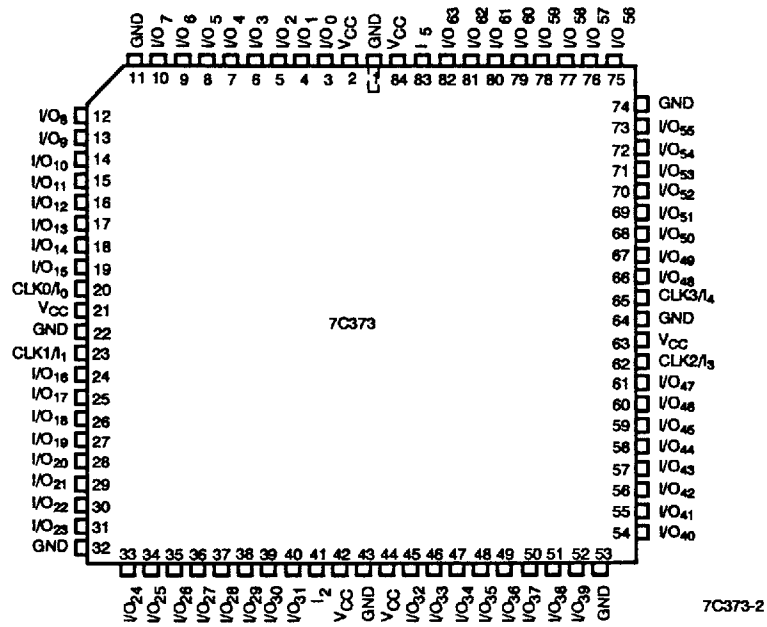
Selection Guide

		7C373–12	7C373–15	7C373–20
Maximum Propagation Delay t_{PD} (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	250	250	250
	Military		300	300
Maximum Operating Current, I_{CC2} (mA)	Commercial	280	280	280
	Military		330	330

Shaded area contains preliminary information.

Pin Configuration

PLCC/CLCC/CQFP
Top View



Functional Description (continued)

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product term resources to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that the product term allocator is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C373 has a separate I/O pin assoicated with it. In other words, each I/O pin is shared by two macrocells. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the four logic blocks on the CY7C373 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C373 is available from Cypress's *Warp2* and *Warp3* software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL, CUPL, and LOG/iC. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

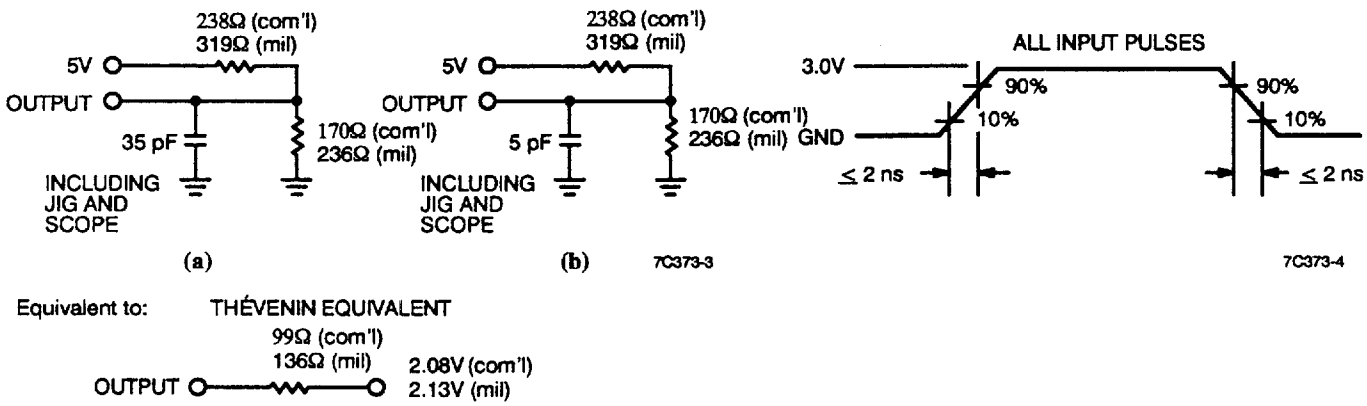
Parameter	Description	Test Conditions			7C373 Min.	7C373 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)		2.4		V
			I_{OL} = −2.0 mA (Mil)				V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OH} = 16 mA (Com'l/Ind)			0.5	V
			I_{OL} = 12 mA (Mil)				V
V_{IH}	Input HIGH Voltage				2.0	7.0	V
V_{IL}	Input LOW Voltage				−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.5V			−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_{CC} = Max., I_{OUT} = 0 mA, f = 0 mHz, V_{IN} = GND, V_{CC}		Com'l		250	mA
				Mil		300	
I_{CC2}	Power Supply Current	V_I = V_{CC} or GND, f = 40 MHz		Com'l		280	mA
				Mil		330	

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

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Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C373–12		7C373–15		7C373–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t_{PD}	Input to Combinatorial Output		12		15		20	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{EA}	Input to Output Enable		16		19		24	ns
t_{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t_{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t_{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t_{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f_{MAX1}	Maximum Frequency of (2) CY7C373s in Input Registered Mode (Lesser of $1/(t_{ICO} + t_{IS})$ and $1/(t_{WL} + t_{WH})$)	55.5		45.5		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of $1/t_{ICO}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$)	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t_{CO}	Clock or Latch Enable to Output		9		12		15	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t_H	Register or Latch Data Hold Time	0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	12		15		20		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f_{MAX3}	Maximum Frequency of (2) CY7C373s in Output Registered Mode (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	55.5		41.7		33.3		MHz
f_{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	100		83.3		62.5		MHz
f_{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	83.3		66.6		50		MHz
Pipelined Mode Parameters								
t_{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f_{MAX6}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:

5. All AC parameters are measured with 16 outputs switching.

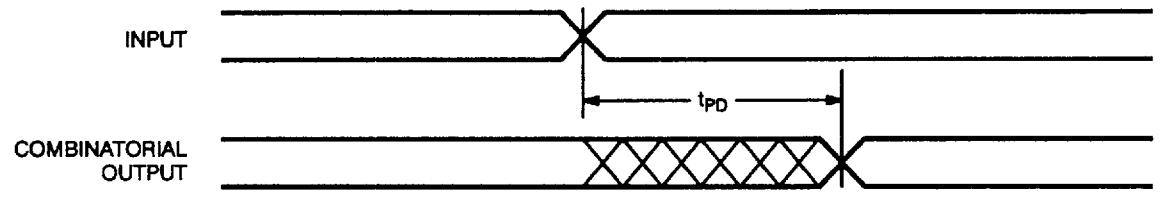
Switching Characteristics Over the Operating Range[5] (continued)

Parameter	Description	7C371–12		7C371–15		7C371–20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t_{RW}	Asynchronous Reset Width	12		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time	14		17		22		ns
t_{RO}	Asynchronous Reset to Output		18		21		26	ns
t_{PW}	Asynchronous Preset Width	12		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time	14		17		22		ns
t_{PO}	Asynchronous Preset to Output		18		21		26	ns

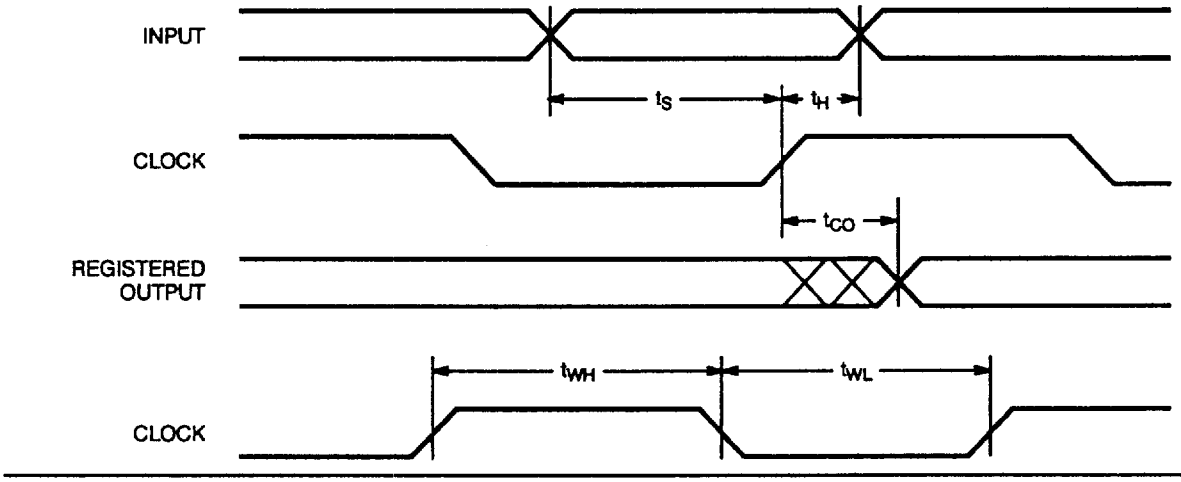
Shaded area contains advanced information.

Switching Waveforms

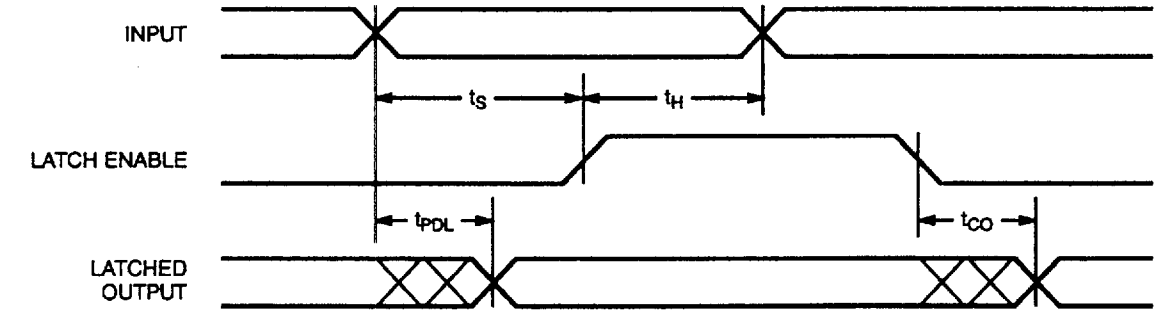
Combinatorial Output



Registered Output

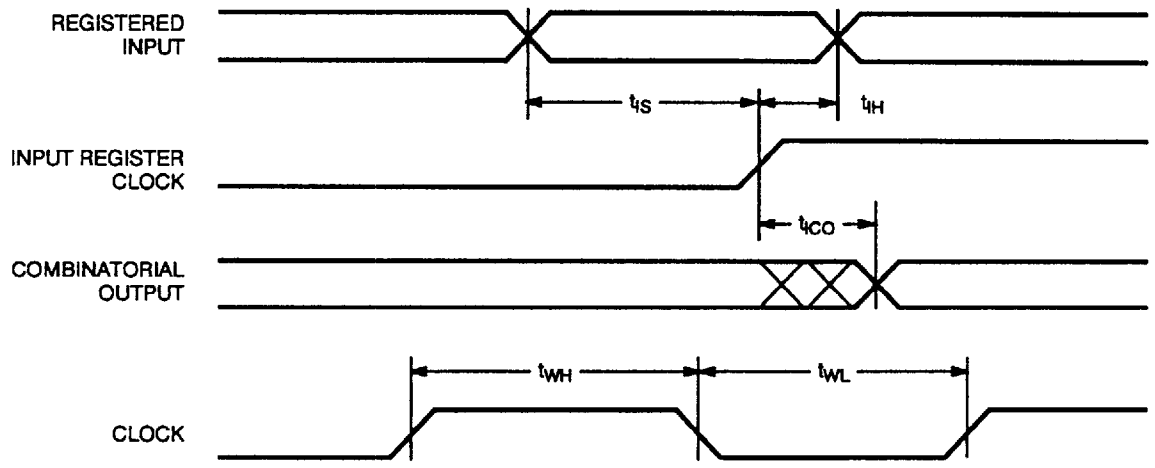


Latched Output



Switching Waveforms (continued)

Registered Input



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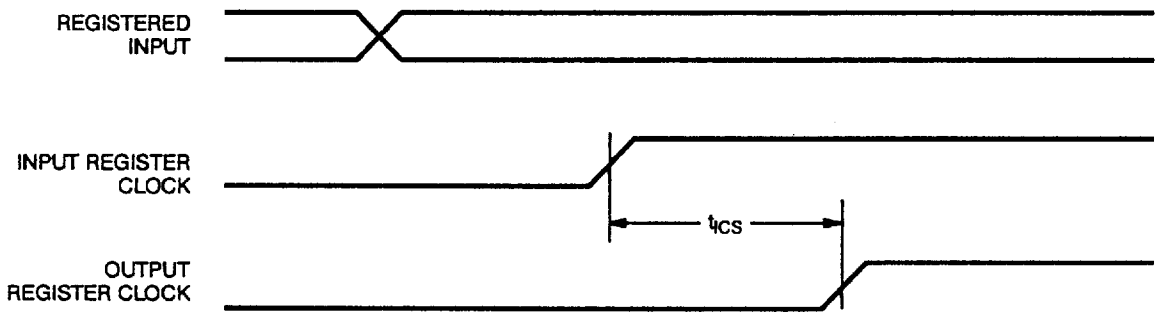
Input Clock to Output Clock



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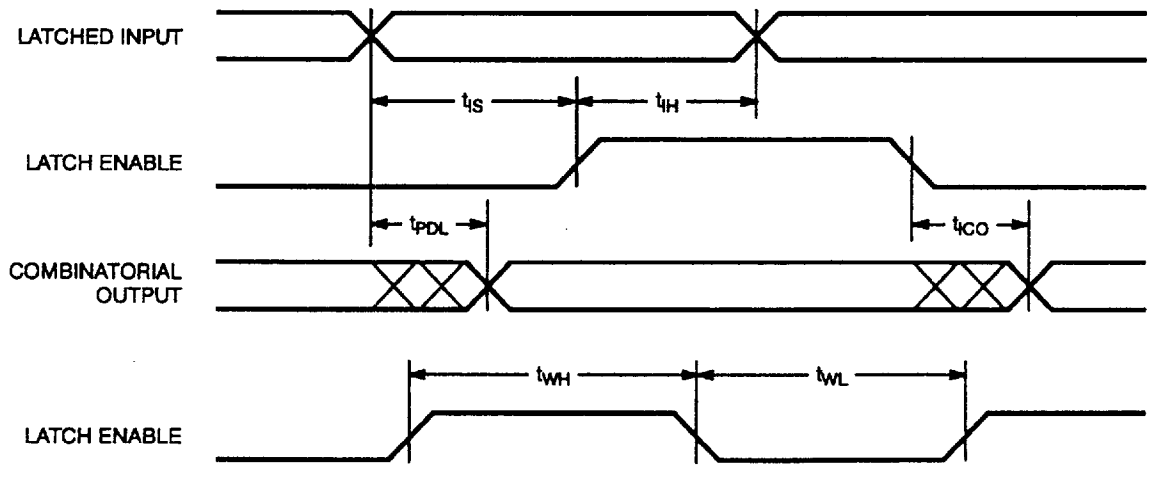
Latched Input



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Switching Waveforms (continued)

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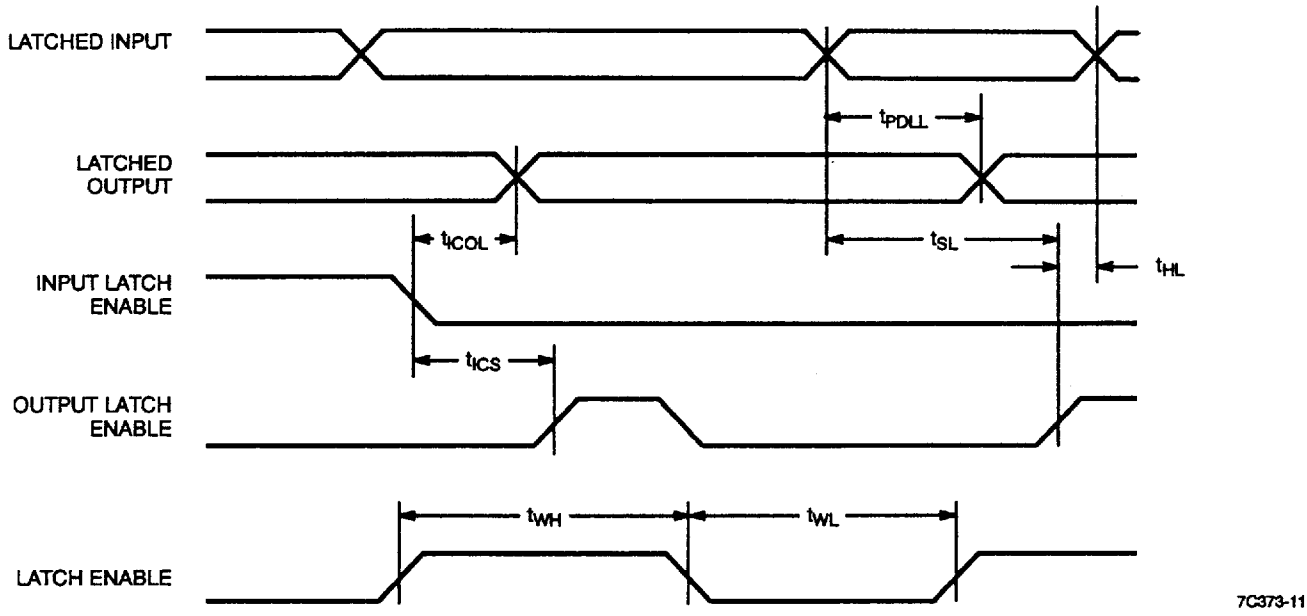
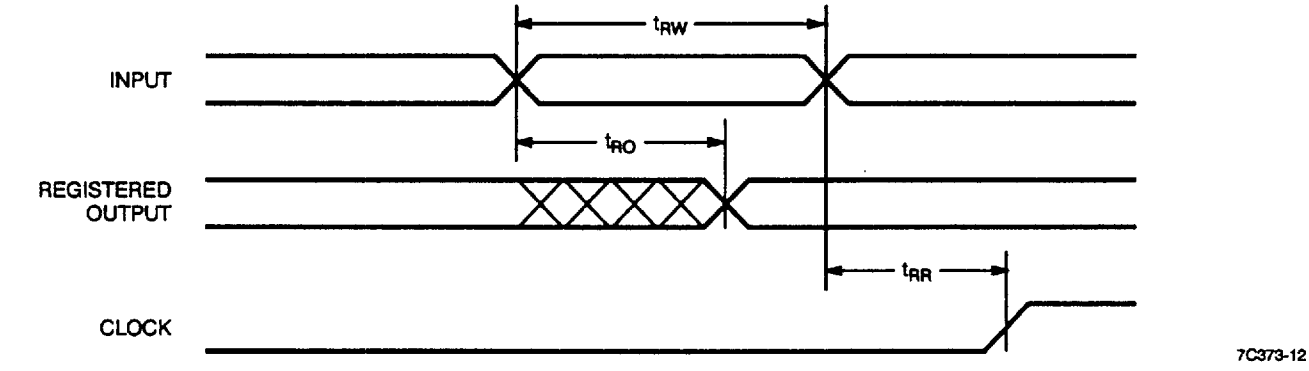
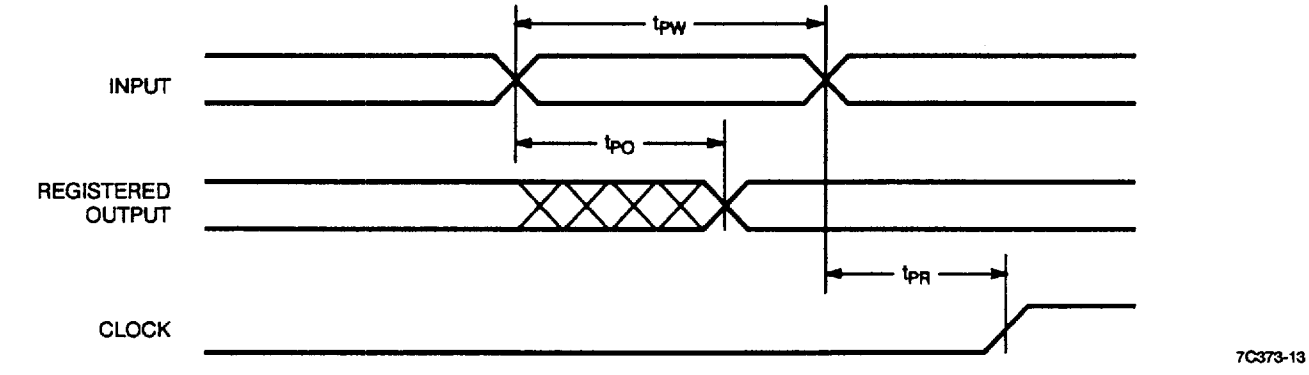
Latched Input and Output



Asynchronous Reset



Asynchronous Preset



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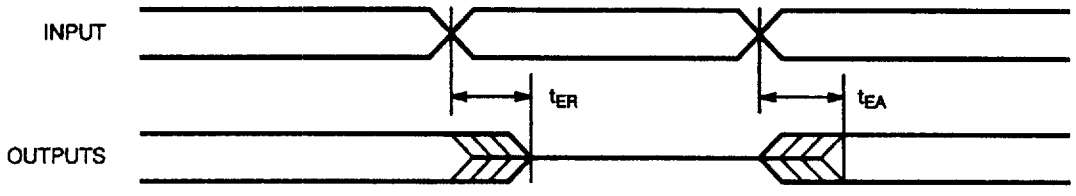
Switching Waveforms (continued)

Output Enable/Disable



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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C373–12GC	G84	Commercial
	CY7C373–12JC	J83	
15	CY7C373–15GC	G84	Commercial
	CY7C373–15JC	J83	
	CY7C373–15YMB	Y84	Military
20	CY7C373–20GC	G84	Commercial
	CY7C373–20JC	J83	
	CY7C373–20YMB	Y84	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11

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Package Diagrams

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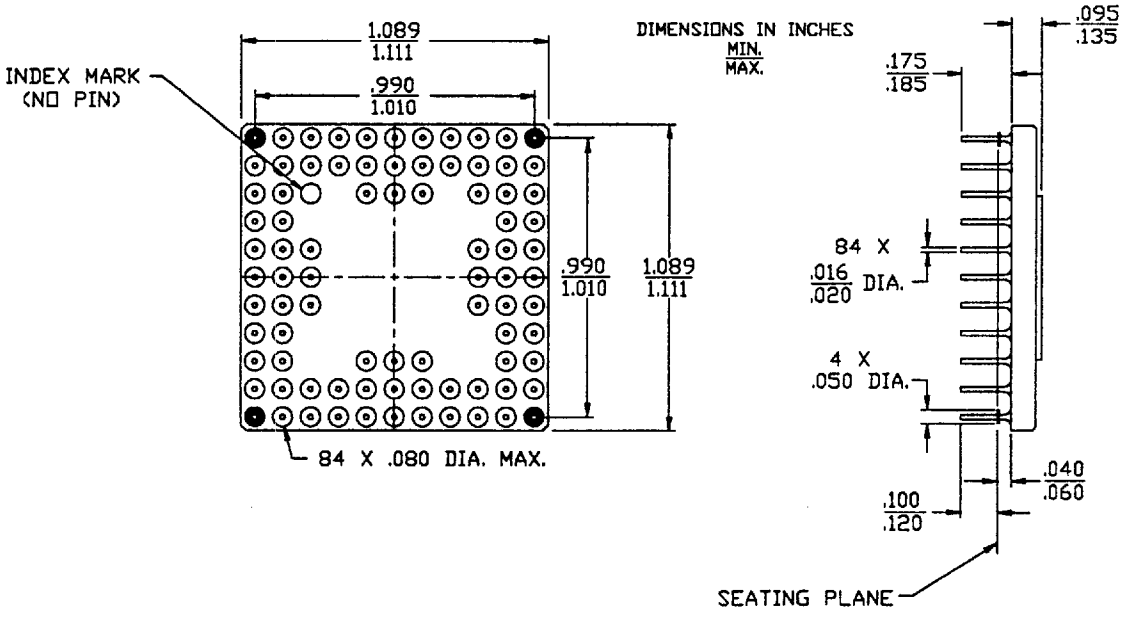
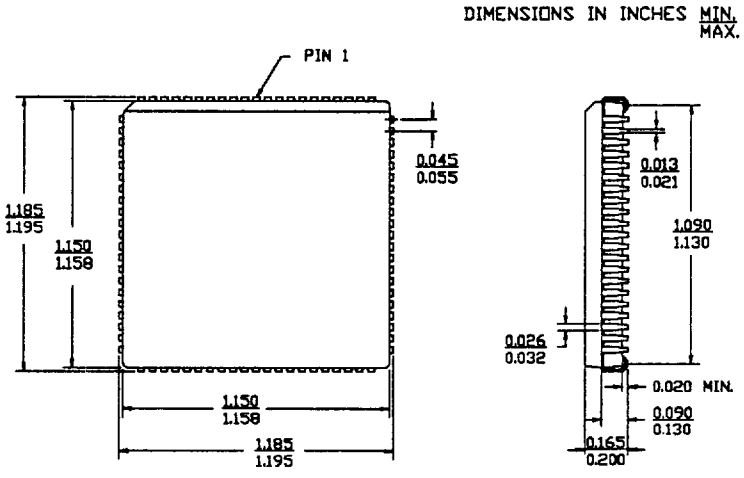
84-Pin Grid Array (Cavity Up) G84



84-Lead Plastic Leaded Chip Carrier J83



Package Diagrams (continued)

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84-Pin Ceramic Leaded Chip Carrier Y84