Very High Speed 8K (24K) Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 100 MHz
  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 7 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 24 x 32 array of 768 logic cells provides 24,000 total available gates
  - 8,000 typically usable "gate array" gates in 145-pin and 245-pin CPGA, 144-pin TQFP, 208-pin PQFP, 160-pin CQFP, and 225-pin BGA packages
- PCI compliant I/O pins
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} of 12 mA and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns)
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or mixed
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 132 (7C387A) to 172 (7C388A) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built-in scan path permits 100 percent factory testing of logic and I/O cells
  - Automatic Test Vector Generation (ATVG) software supports user testing after programming
- 0.65μ CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 144-pin TQFP, 145-pin CPGA, and 160-pin CQFP are pin compatible with the CY7C386A

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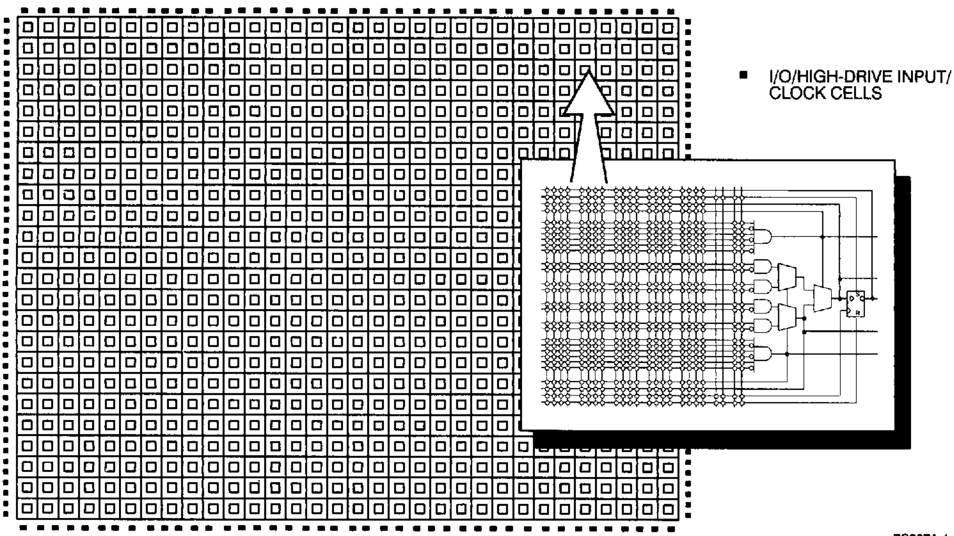
Logic Block Diagram



144 and 208 PINS, 172 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS

Functional Description

The CY7C387A and CY7C388A are very high speed, CMOS, user-programmable ASIC (pASIC™) devices. The 768 logic cell field-programmable gate array (FPGA) offers 8,000 typically usable "gate array" gates. This is equivalent to 24,000 EPLD or LCA gates. The CY7C387A is available in a 145-pin CPGA, 160-pin CQFP, and 144-pin TQFP. The CY7C388A is available in 208-pin PQFP, 245-pin CPGA, and 225-pin BGA packages.

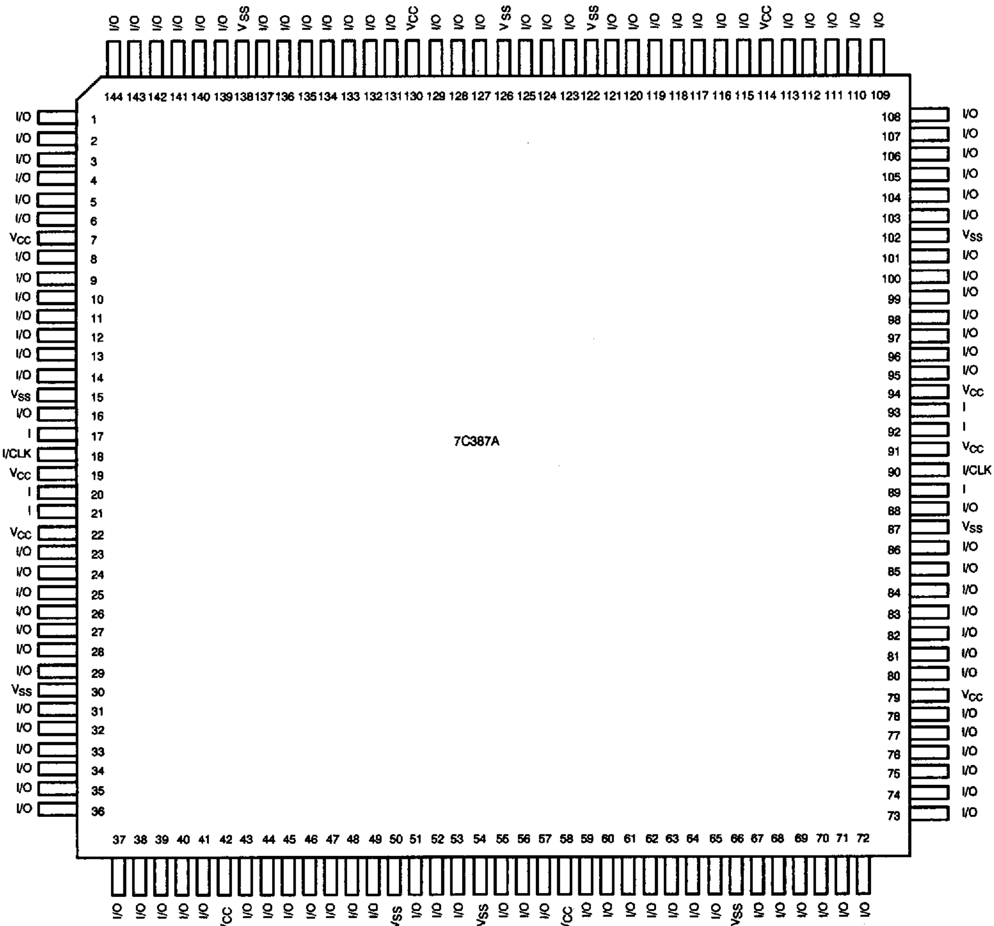
Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C387A and CY7C388A using Cypress *Warp3* software or one of several third-party tools. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C387A and CY7C388A feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

Pin Configurations

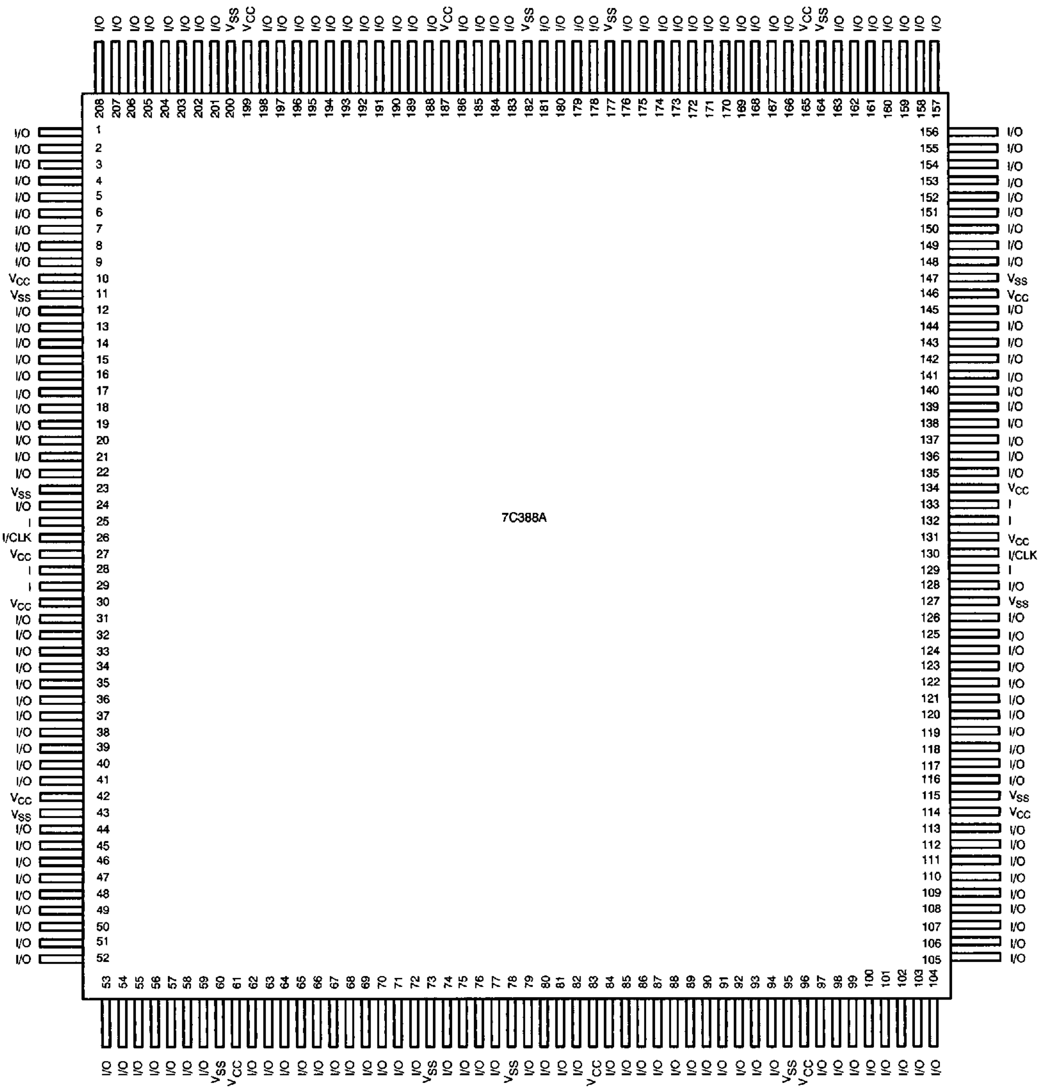
144-Pin Thin Quad Flat Pack (TQFP)
Top View



7C387A-2

Pin Configurations (continued)

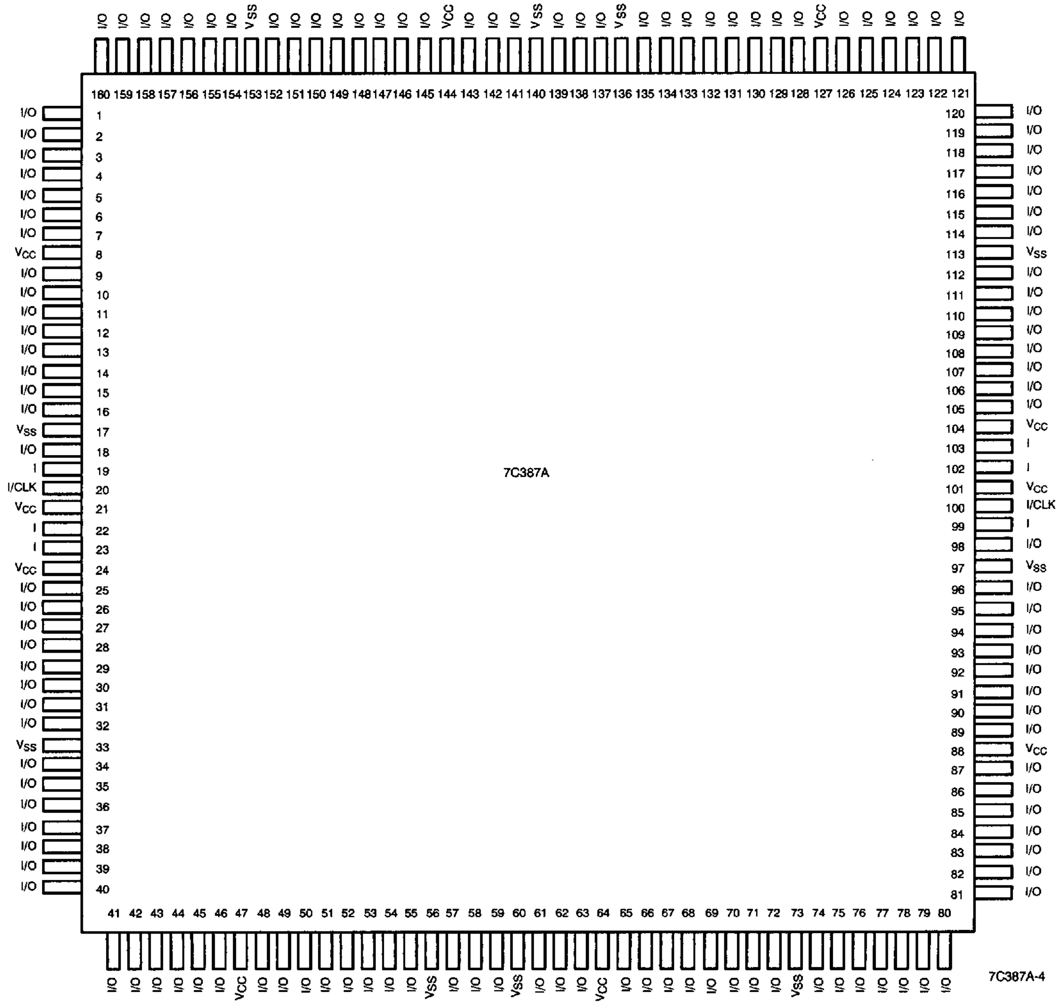
208-Pin Plastic Quad Flat Pack (PQFP)
Top View



7C387A-3

Pin Configurations (continued)

160-Pin CQFP
Top View



Pin Configurations (continued)

145-Pin CPGA
Bottom View

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
3	I/O	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	I/O
4	I/O	I/O	I/O										I/O	I/O	I/O
5	I/O	I/O	V_{CC}										V_{SS}	I/O	I/O
6	I/O	I/O	I/O										I/O	I/O	I/O
7	I	I	V_{SS}										V_{CC}	I/O	I/O
8	I/O	I	I/CLK					7C387A					I/CLK	I	I/O
9	I/O	I/O	V_{CC}										V_{SS}	I	I
10	I/O	I/O	I/O										I/O	I/O	I/O
11	I/O	I/O	V_{SS}										V_{CC}	I/O	I/O
12	I/O	I/O	I/O										I/O	I/O	I/O
13	I/O	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	I/O
14	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
- Ceramic .... −65°C to +150°C
- Plastic .... −40°C to +125°C

Lead Temperature .... 300°C

Supply Voltage .... −0.5V to +7.0V

Input Voltage .... −0.5V to V_{CC} +0.5V

ESD Pad Protection .... ±2000 V

DC Input Voltage .... −0.5V to 7.0V

Latch-Up Current .... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −8.0 mA	2.4		V
		I_{OH} = −10.0 µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA Military/Industrial I_{OL} = 12 mA Commercial		0.4	V
		I_{OL} = 10.0 µA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OZ}	Three-State Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Switching Characteristics Over the Operating Range

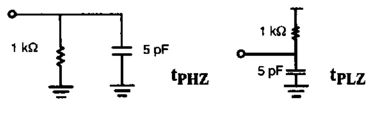
Parameter	Description	Propagation Delays[1] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[2]	1.7	2.2	2.6	3.2	5.3	ns
t_{SU}	Set-Up Time[2]	2.1	2.1	2.1	2.1	2.1	ns
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[1] with Fanout of 1	2	3	4	8	12	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.2	4.7	6.5	ns
t_{GCK}	Clock Buffer Delay[3]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t_{GCKHI}	Clock Buffer Min. HIGH[3]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW[3]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays[1] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[4]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[4]	3.3					ns

Notes:

1. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
2. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
3. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
4. The following loads are used for t_{PXZ}:



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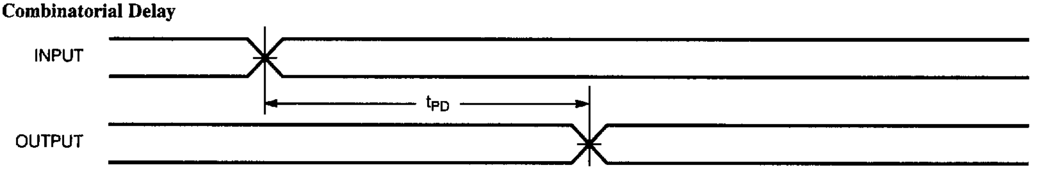
High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[1] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{INI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

Switching Waveforms

Combinatorial Delay



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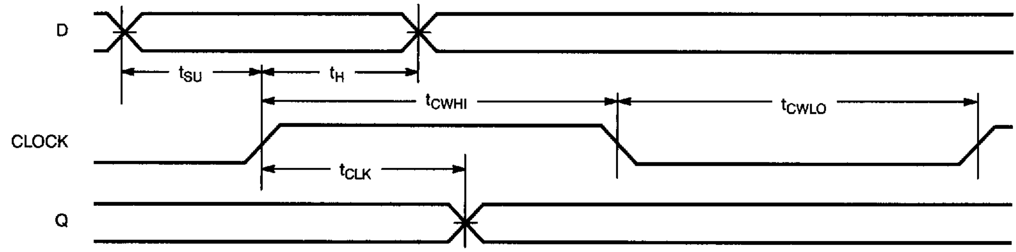
Set-Up and Hold Times



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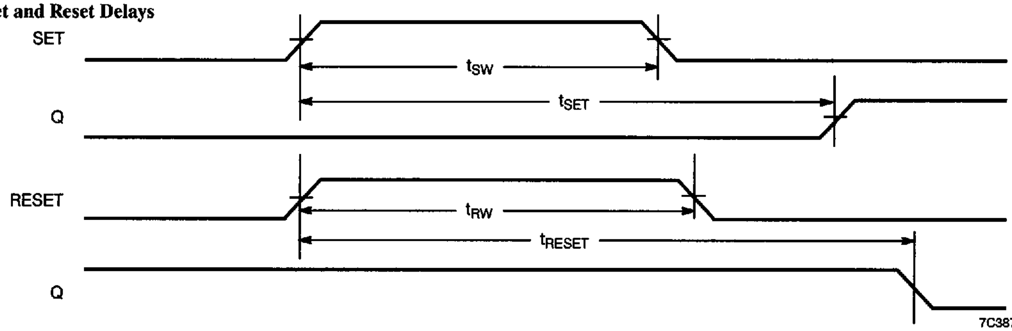
Set and Reset Delays



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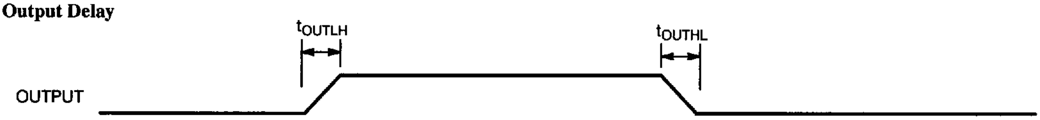
Output Delay



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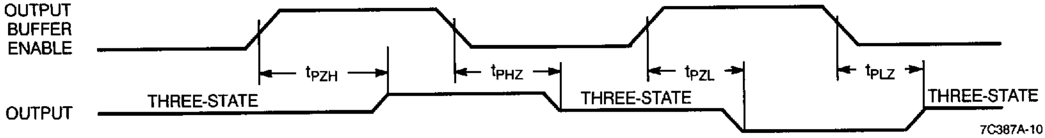
Switching Waveforms (continued)

Three-State Delay

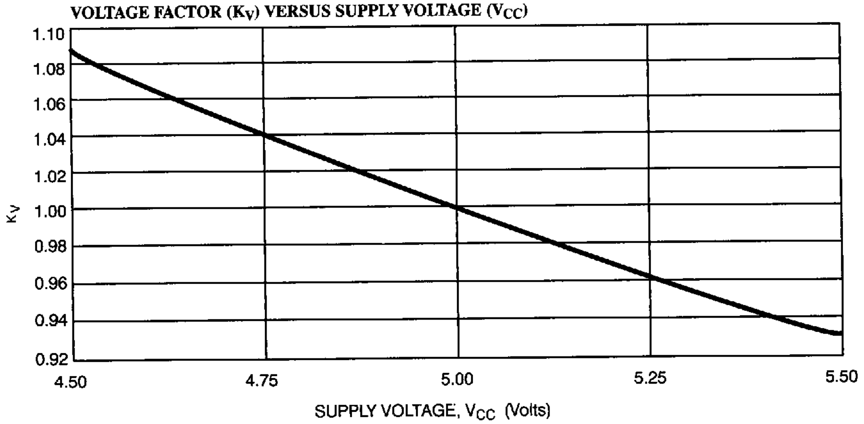


7C387A-10

Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. *Warp3* incorporates datasheet AC Characteristics into the design database for pre–place-and-route simulations. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

VOLTAGE FACTOR (K_V) VERSUS SUPPLY VOLTAGE (V_{CC})



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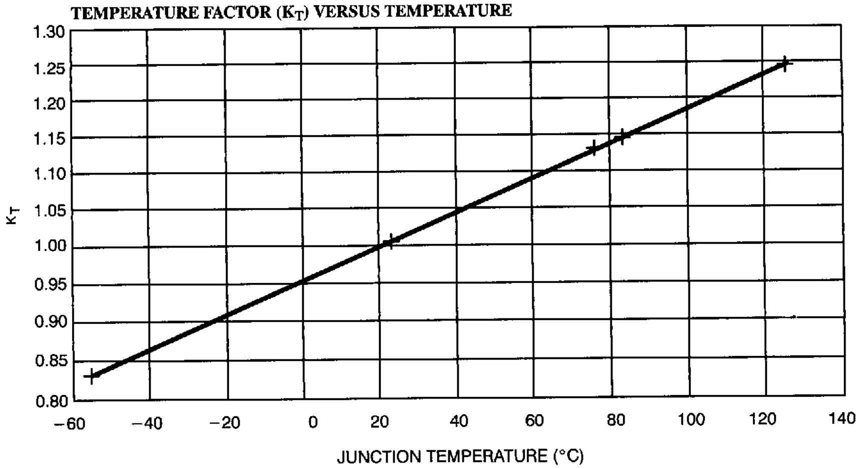
TEMPERATURE FACTOR (K_T) VERSUS TEMPERATURE



7C387A-12

*THETA JA = 45 °C/WATT FOR PLCC

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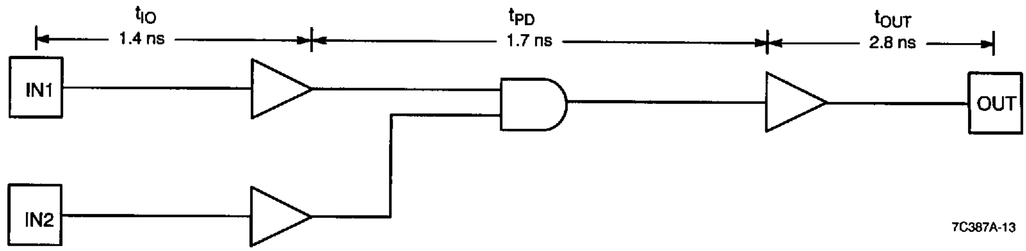
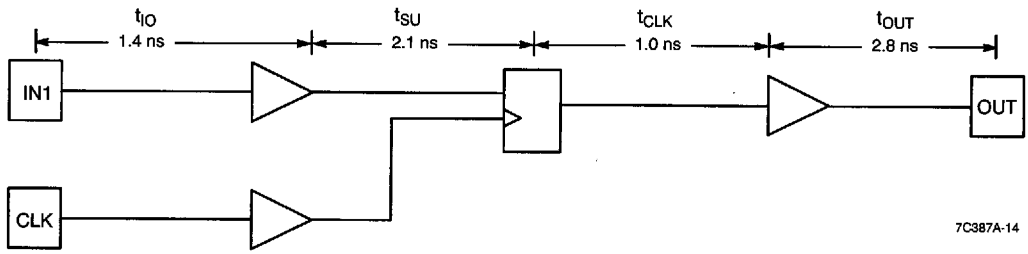
Combinatorial Delay Example (Load = 30 pF)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF)



INPUT DELAY + REG SET-UP + CLOCK TO OUTPUT + OUTPUT DELAY = 7.3 ns

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C387A–2AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–2GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–2AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–2GI	G145	145-Pin Grid Array (Cavity Up)	
1	CY7C387A–1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–1GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–1GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–1GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C387A–1UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	
0	CY7C387A–0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C387A–0GC	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C387A–0GI	G145	145-Pin Grid Array (Cavity Up)	
	CY7C387A–0GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C387A–0UMB	U162	160-Lead Ceramic Quad Flatpack (Cavity Up)	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C388A–2AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–2BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–2GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–2AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–2GI	G245	245-Pin Grid Array (Cavity Up)	
1	CY7C388A–1AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–1BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–1GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–1AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–1GI	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–1GMB	G245	245-Pin Grid Array (Cavity Up)	Military
0	CY7C388A–0AC	A208	208-Pin Thin Quad Flat Pack	Commercial
	CY7C388A–0BGC	B225	225-Pin Ball Grid Array	
	CY7C388A–0GC	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–0AI	A208	208-Pin Thin Quad Flat Pack	Industrial
	CY7C388A–0GI	G245	245-Pin Grid Array (Cavity Up)	
	CY7C388A–0GMB	G245	245-Pin Grid Array (Cavity Up)	Military

Shaded area contains advanced information.

Military Specifications
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Document #: 38–00373

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  - Chip-to-chip operating frequencies up to 85 MHz
  - Input + logic cell + output delays under 7 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 32 x 36 array of 1152 logic cells provides 36,000 total available gates
  - 12,000 typically usable "gate array" gates in 208-pin PQFP, 313-pin BGA, and 245-pin CQFP packages
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 100 MHz consumes 50 mA
  - Minimum I_{OL} and I_{OH} of 8 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns)
- PCI compliant I/O pins
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or both
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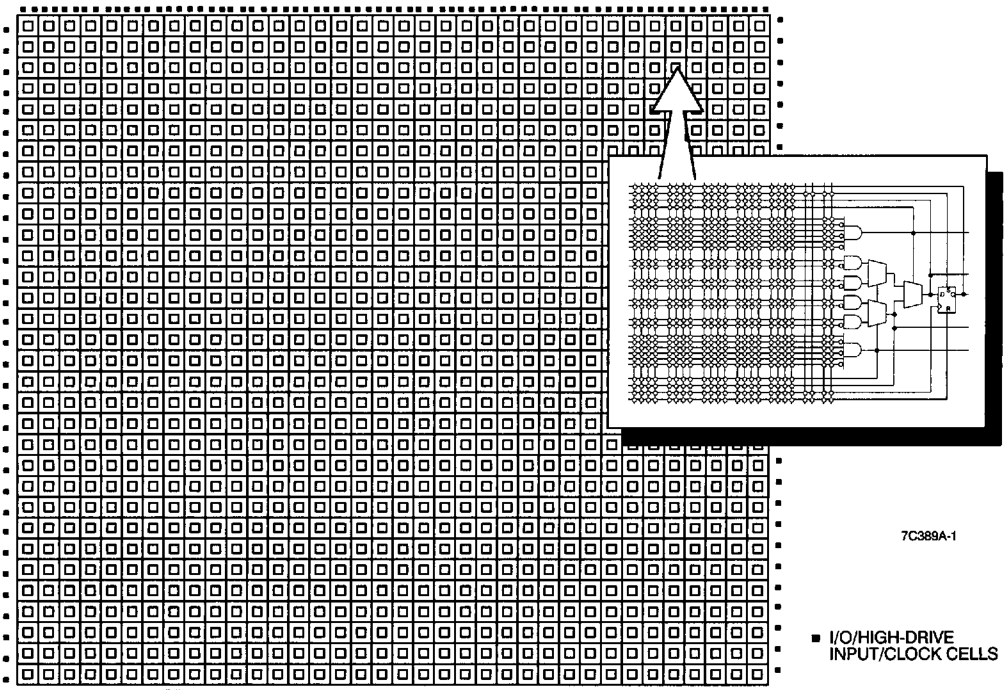

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