

LC7935

3057

CMOS LSI

32-Bit Thermal Printer Head Driver

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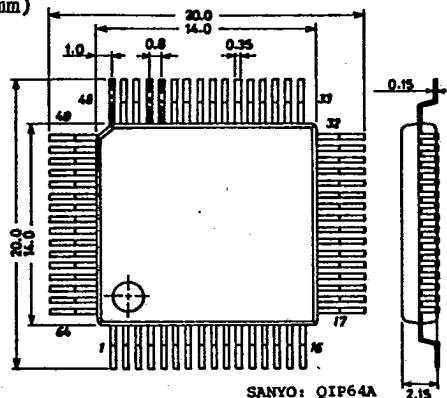
Features

- . High-speed, high-voltage silicon gate CMOS device
- . Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- . Serial shift data is shifted on the positive transition of the clock (CLOCK).
- . 32-bit latch data is changed on the negative transition of the LATCH pad and is held on the positive transition.
- . The STROBE pad, BEO pad can be used to exercise on/off control of the output driver.
- . Complete separation of logic circuit GND (pad 1) and thermal driver GND (pad 4)
- . Maximum ratings of driver output: $V_O=15V$, $I_{OL}=30mA$
- . Logic unit operating voltage: $V_{DD}=4.5V$ to $5.5V$

Absolute Maximum Ratings at Ta=25°C

Maximum Ratings at 100°C			Unit
Maximum Supply Voltage	V _{DD}	-0.3 to 7.0	V
Input Voltage	V _I	-0.3 to V _{DD} +0.3	V
Output Voltage	V _O (1)	-0.3 to V _{DD} +0.3	V
	V _O (2)	15	V
Output Circuit	I _O	D1 to D32 output Output Tr off D1 to D32 output, per output	30 mA
Allowable Power Dissipation of Package	P _{C(max)}	QIP-64 package at 70°C	450 mW
Operating Temperature	Topg	QIP-64 package	0 to +70 °C
Storage Temperature	Tstg	QIP-64 package	-35 to +125 °C

Case Outline 3057-Q64AIC
(unit:mm)



SANYO: OIP64A

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8077AT/9185MW, TS No. 2002-1/5

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Allowable Operating Conditions at Ta=0 to +70°C

	Pin Name	min	typ	max	unit
Supply Voltage	V _{DD}	4.5		5.5	V
"H"-Level Input Voltage	V _{IH}	0.8V _{DD}		V _{DD}	V
"L"-Level Input Voltage	V _{IL}	V _{SS} (L)		0.2V _{DD}	V
Clock Frequency	f _{CLK}			5.0	MHz
Clock Pulse Width	t _{Wd}	75			ns
Clock Rise/Fall Time	t _r , t _f			200	ns
Data Setup Time	t _{DS}	100			ns
Data Hold Time	t _{DH}	50			ns
Latch Pulse Width	t _{WL}	100			ns

Electrical Characteristics at Ta=25°C

			min	typ	max	unit
"H"-Level Input Current	I _{IN} (1)	S _{IN} , CLOCK LATCH			10	uA
"	I _{IN} (2)	BEO	12		72	uA
"L"-Level Input Current	I _{IL} (1)	S _{IN} , CLOCK LATCH	-10			uA
"	I _{IL} (2)	STROBE	-72		-12	uA
"H"-Level Output Voltage	V _{OH}	S _{OUT}	V _{DD} =5V, I _{OH} =-0.5mA	V _{DD} -0.5		V
"L"-Level Output Voltage	V _{OL} (1)	S _{OUT}	V _{DD} =5V, I _{OL} =0.5mA		0.5	V
"	V _{OL} (2)	D1toD32	V _{DD} =5V, I _{OL} =30mA		0.5	V
Output Off-State Leakage Current	I _{OFF}	D1toD32	V _O =15V		20	uA
Input Capacitance	C _{IN}	CLOCK		5.0		pF
Operating Current Dissipation	I _{DD}	V _{DD}	V _{DD} =5V, f _{CLK} =5MHz, all outputs: no load		5	mA

Switching Characteristics at Ta=25°C

	Pin Name	min	typ	max	unit
Clock Latch Delay Width	t _{CL}	CLOCK, LATCH	V _{DD} =5V	100	ns
Latch Clock Delay Width	t _{LC}	CLOCK, LATCH	V _{DD} =5V	0	ns
"H"-Level Output Propagation Delay Time	t _{PLH} (1)	LATCH, D1toD32	V _{DD} =5V, Dn: R _L =1.0kohm C _L =15pF	400	ns
	t _{PLH} (2)	BEO, STROBE	V _{DD} =5V, Dn: R _L =1.0kohm C _L =15pF	300	ns
	t _{PLH} (3)	CLOCK, S _{OUT}	V _{DD} =5V, S _{OUT} : C _L =15pF	200	ns
"L"-Level Output Propagation Delay Time	t _{PHL} (1)	LATCH, D1toD32	V _{DD} =5V, Dn: R _L =1.0kohm C _L =15pF	200	ns
	t _{PHL} (2)	BEO, STROBE D1toD32	V _{DD} =5V, Dn: R _L =1.0kohm C _L =15pF	100	ns
	t _{PHL} (3)	CLOCK, S _{OUT}	V _{DD} =5V, S _{OUT} : C _L =15pF	200	ns

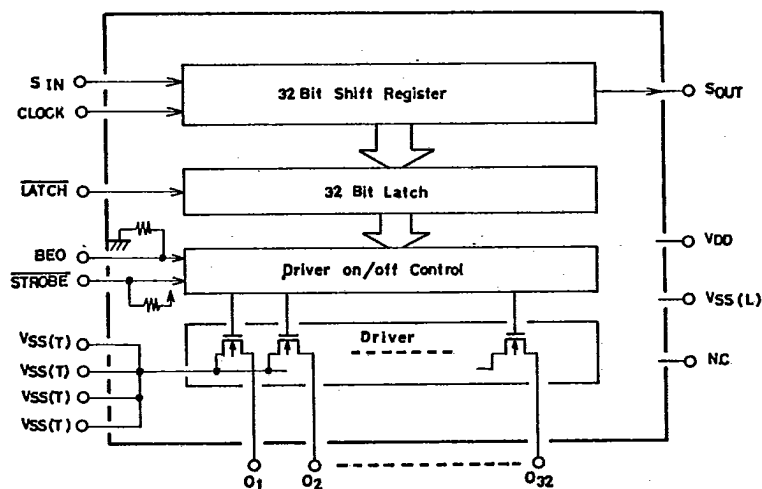
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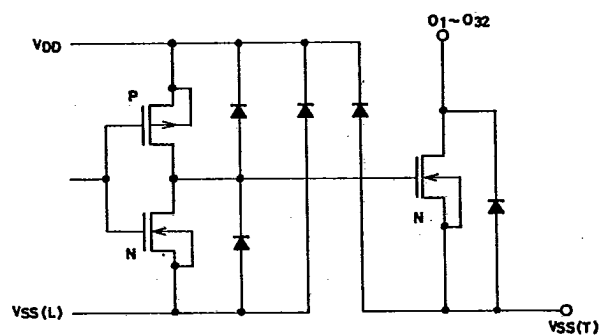
Thermal Driver On/Off Truth Table

Latch Data (Q)	BEO	STROBE	Thermal Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Thermal on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

Equivalent Circuit Block Diagram



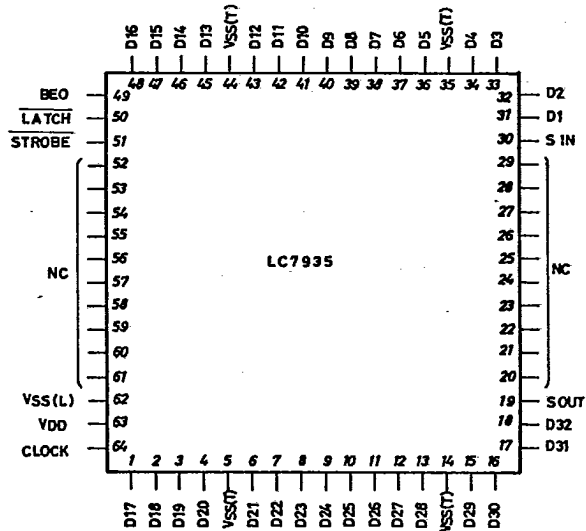
Output Driver Section Equivalent Circuit



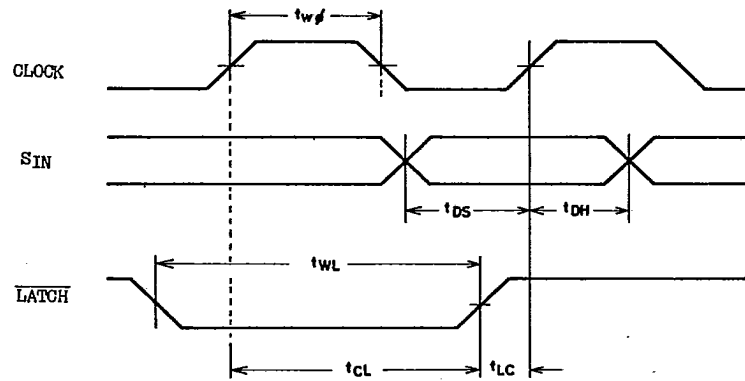
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Pin Assignment



Input Data Timing Chart



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Output Data Timing Chart

