CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C421A
CY7C425A

High-Speed Cascadable 512 x 9 FIFO 1K x 9 FIFO

Features

- **512 x 9 and 1K x 9 FIFO buffer memory**
- **Dual-port RAM cell**
- **Asynchronous read/write**
- **High-speed 66.6-MHz read/write independent of depth/width**
- **10-ns access time**
- **Half Full flag in standalone**
- **Empty and Full flags**
- **Retransmit in standalone mode**
- **Expandable in width and depth**
- **Parallel cascade minimizes bubble-through**
- **5V ± 10% supply**
- **300-mil 28-pin DIP and 32-pin PLCC packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7201 and IDT7202**

Functional Description

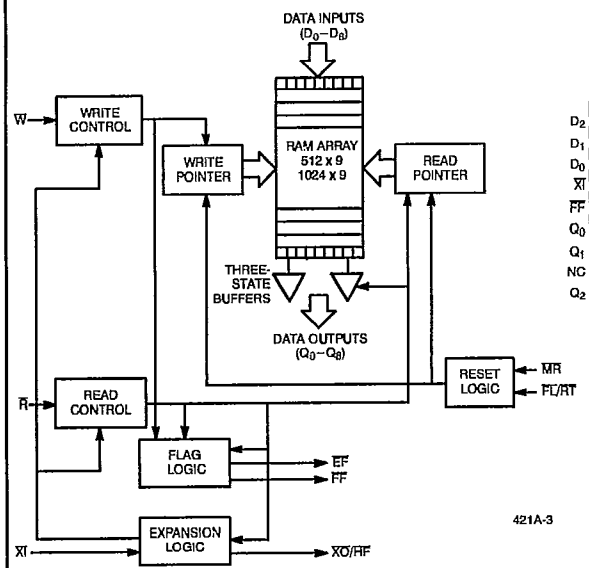
The CY7C421A and CY7C425A are first-in first-out (FIFO) memories. They are, respectively, 512 and 1,024 words by 9-bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 66.6 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

Logic Block Diagram



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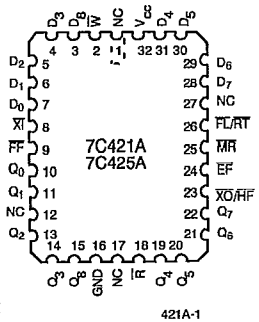
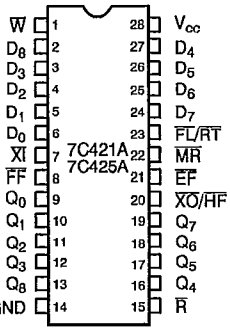
Pin Configurations

PLCC
Top View



421A-1

DIP
Top View



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CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C421A
CY7C425A

Selection Guide

		7C421A–10 7C425A–10	7C421A–15 7C425A–15
Frequency (MHz)		66.6	40
Maximum Access Time (ns)		10	15
Maximum Operating Current (mA)	Commercial	10	15

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C
Ambient Temperature with Power Applied ..... – 55°C to +125°C
Supply Voltage to Ground Potential ..... – 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V
DC Input Voltage ..... – 0.5V to +7.0V

Power Dissipation 1.0W
Output Current, into Outputs (LOW) ..... 20 mA
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C421A–10 7C425A–10 Min.	7C421A–10 7C425A–10 Max.	7C421A–15 7C425A–15 Min.	7C421A–15 7C425A–15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		– 1	+1	– 1	+1	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}, V_{CC} = Max.		– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		180		120	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		15		15	mA
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} – 0.2V	Com'l		5		5	mA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			– 90		– 90	mA

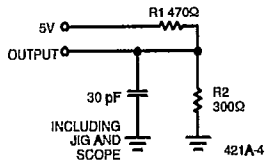
Capacitance[4]

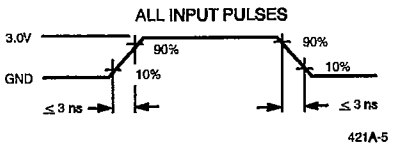
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

5 FIFOs

AC Test Loads and Waveforms



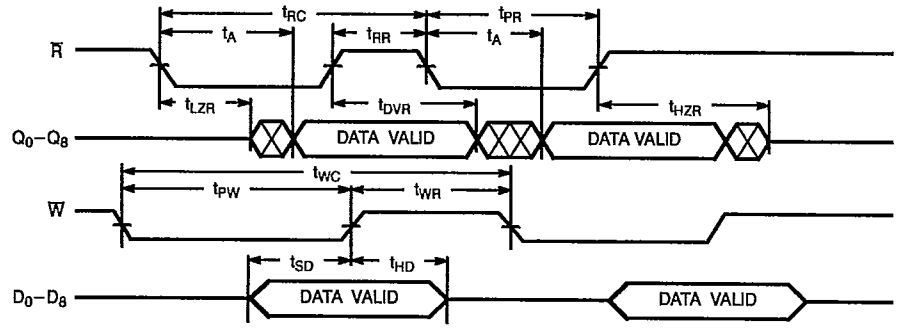


Switching Characteristics Over the Operating Range[5,6]

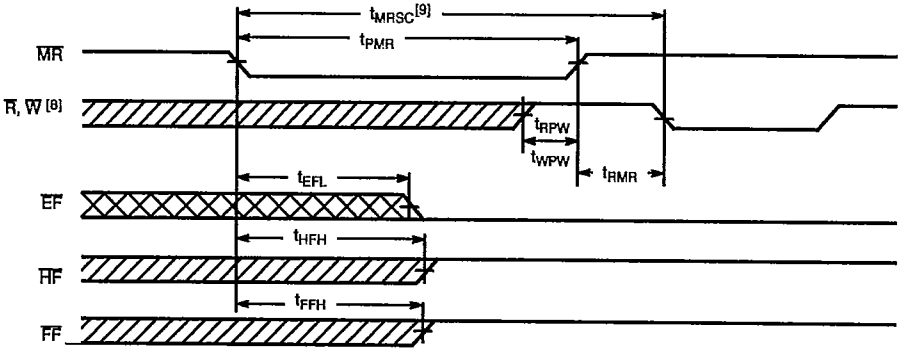
Parameter	Description	7C421A–10 7C425A–10 Min.	7C421A–10 7C425A–10 Max.	7C421A–15 7C425A–15 Min.	7C421A–15 7C425A–15 Max.	Unit
t_{RC}	Read Cycle Time	15		25		ns
t_A	Access Time		10		15	ns
t_{RR}	Read Recovery Time	5		10		ns
t_{PR}	Read Pulse Width	10		15		ns
t_{DVR}[7]	Data Valid After Read HIGH	5		5		ns
t_{HZR}[7]	Read HIGH to High Z		15		15	ns
t_{WC}	Write Cycle Time	15		25		ns
t_{PW}	Write Pulse Width	10		15		ns
t_{WR}	Write Recovery Time	5		10		ns
t_{SD}	Data Set-Up Time	8		10		ns
t_{HD}	Data Hold Time	0		0		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	15		25		ns
t_{PMR}	$\overline{MR}$ Pulse Width	10		15		ns
t_{RMR}	$\overline{MR}$ Recovery Time	5		10		ns
t_{RTC}	Retransmit Cycle Time	15		25		ns
t_{PRT}	Retransmit Pulse Width	10		15		ns
t_{RTR}	Retransmit Recovery Time	5		10		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		10		15	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		10		15	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		10		15	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		10		15	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		10		15	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		10		15	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		10		15	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		10		15	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		10		15	ns
t_{XOL}	Expansion Out LOW Delay from Clock		12		15	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		12		15	ns
t_{LZR}	Read LOW to Low Z	1		1		ns
t_{HWZ}	Write HIGH to Low Z	5		5		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	10		15		ns
t_{RAE}	Effective Read from Write HIGH		10		15	ns
t_{RPE}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns
t_{WAF}	Effective Write from Read HIGH		10		15	ns
t_{WPF}	Effective Read Pulse Width After $\overline{FF}$ HIGH	10		15		ns

Switching Waveforms

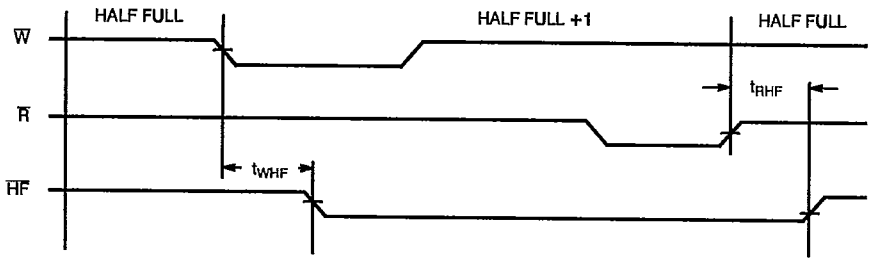
Asynchronous Read and Write



Master Reset



Half-Full Flag

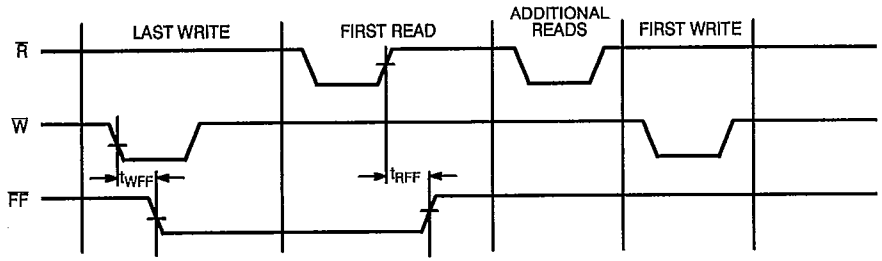


Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
8. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
9. $t_{MRSC} = t_{PMR} + t_{RMR}$.

Switching Waveforms (continued)

Last Write to First Read Full Flag



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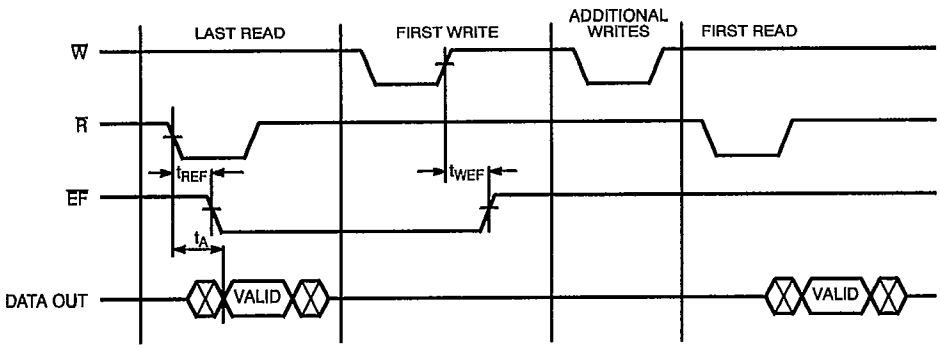
Last Read to First Write Empty Flag



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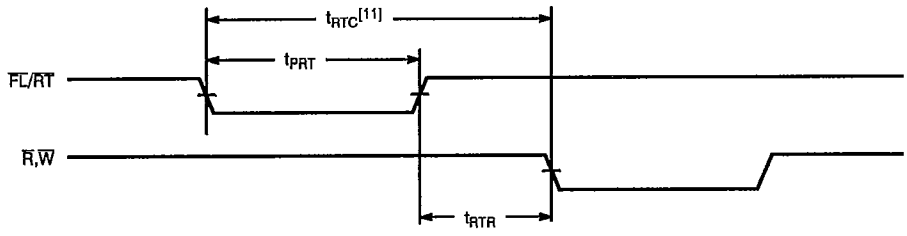
Retransmit[10]



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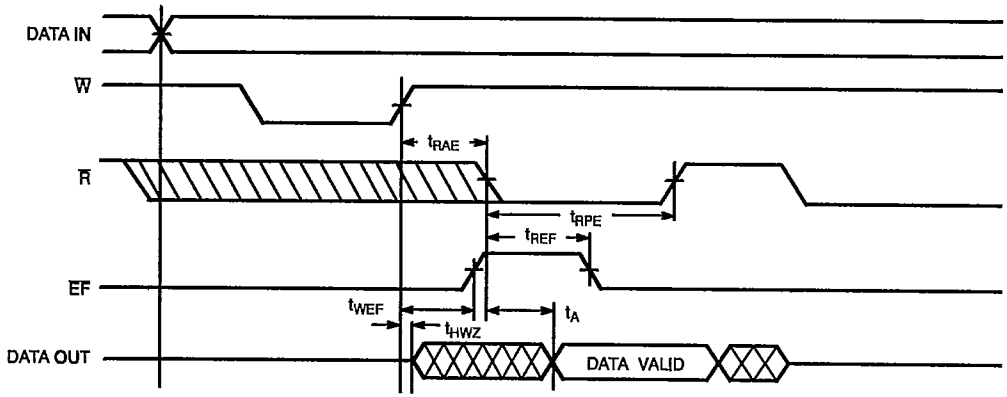
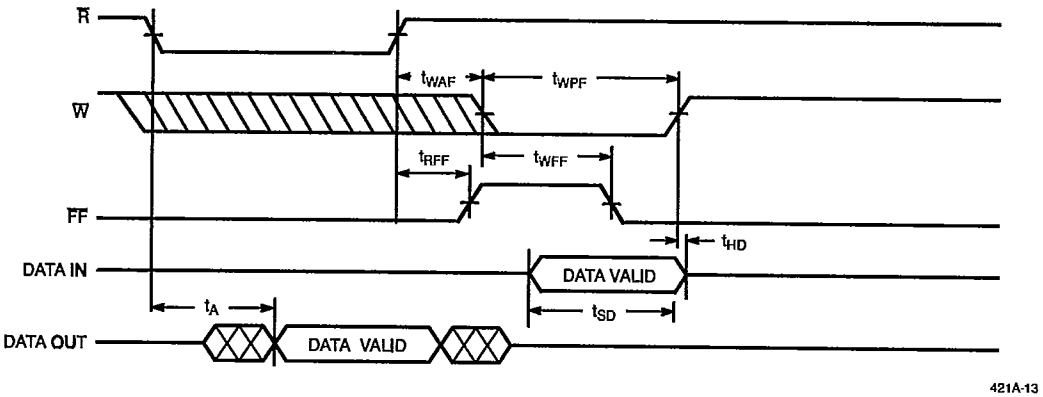
Notes:
10. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
11. $t_{RTC} = t_{PRT} + t_{RTR}$.

Switching Waveforms (continued)

Empty Flag and Empty Boundary Timing Diagram

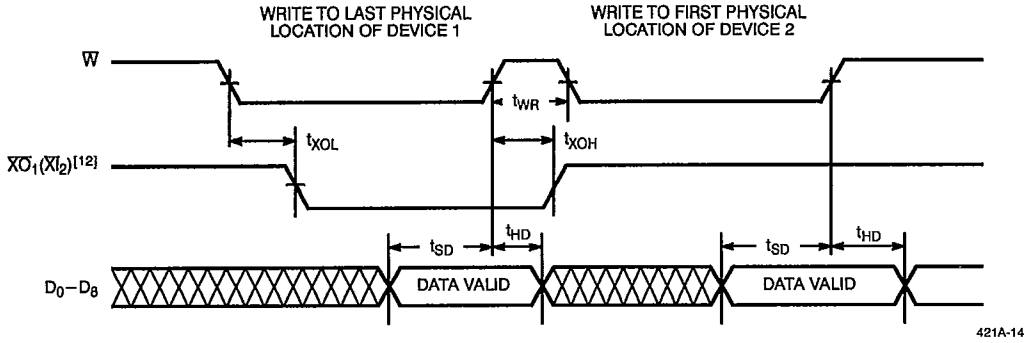


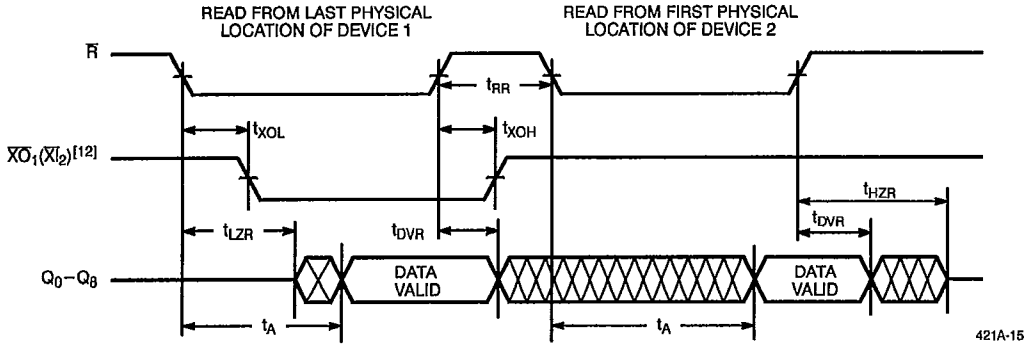
Full Flag and Full Boundary Timing Diagram



Switching Waveforms (continued)

Expansion Timing Diagrams





Note:
12. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

Architecture

The CY7C421A/425A FIFOs consist of an array of 512/1024 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data propagation through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs (D_0 - D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs t_{WEF} after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW t_{WHF} after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active once the FIFO is filled to half its capacity plus one word. $\overline{HF}$ will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs t_{RHF} after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW t_{WFF} after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH t_{REF} after a read from a full FIFO.

Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle if the $\overline{EF}$ is not LOW. Data outputs (Q_0 - Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH) when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH while and t_{RTR} after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also.

The full depth of the FIFO can be repeatedly transmitted.

Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to V_{CC}. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

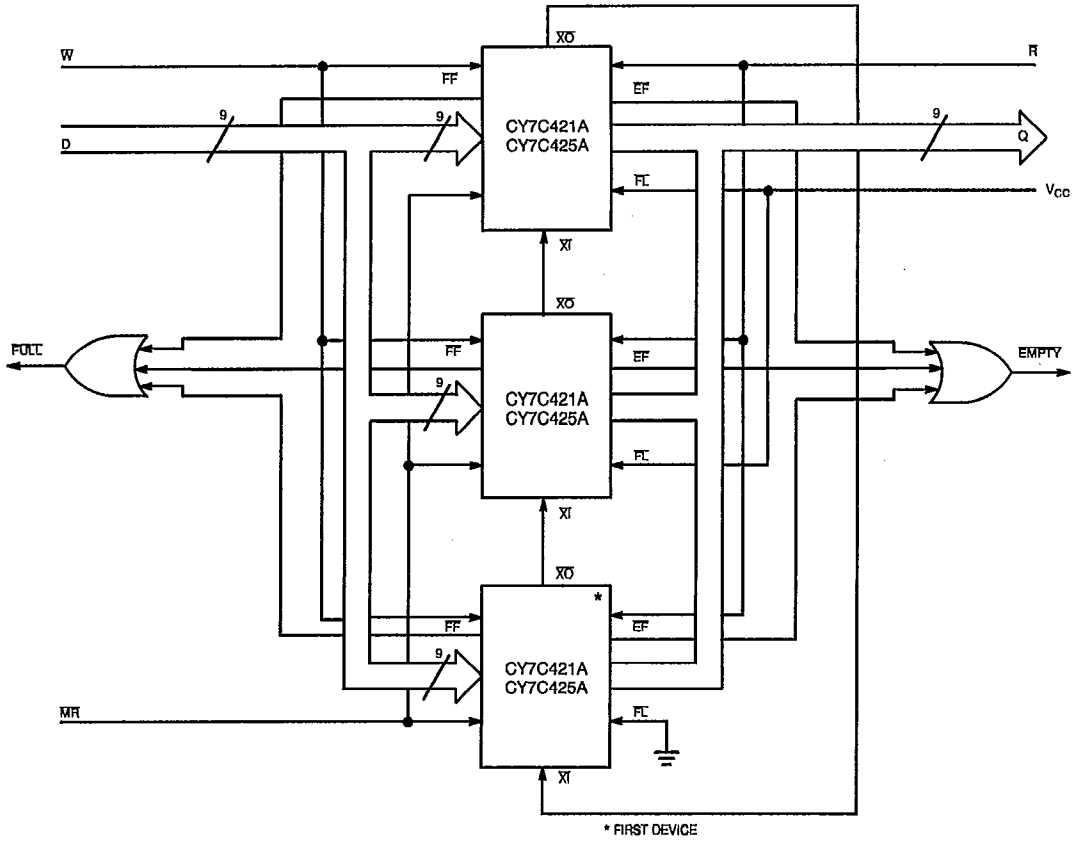


Figure 1. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C421A–10JC	J65	Commercial
	CY7C421A–10PC	P21	
15	CY7C421A–15JC	J65	Commercial
	CY7C421A–15PC	P21	

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C425A–10JC	J65	Commercial
	CY7C425A–10PC	P21	
15	CY7C425A–15JC	J65	Commercial
	CY7C425A–15PC	P21	

Document #: 38–00248

CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

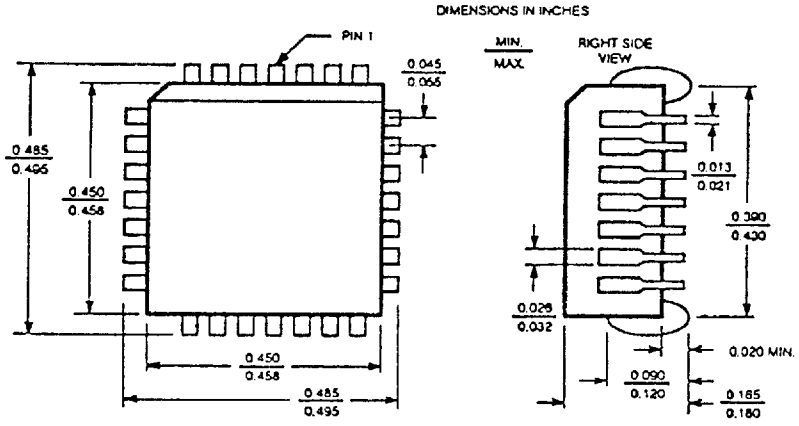
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

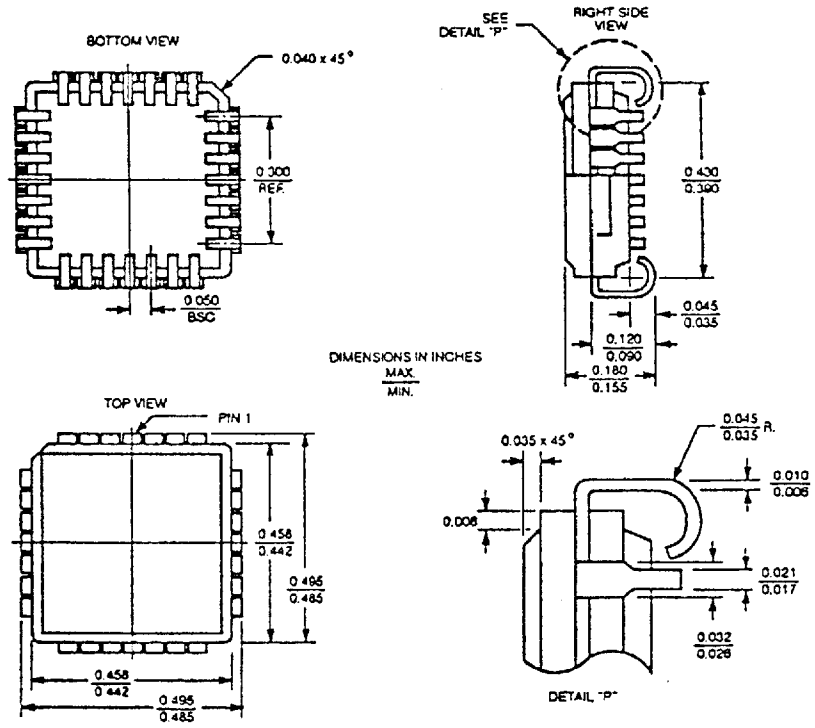


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

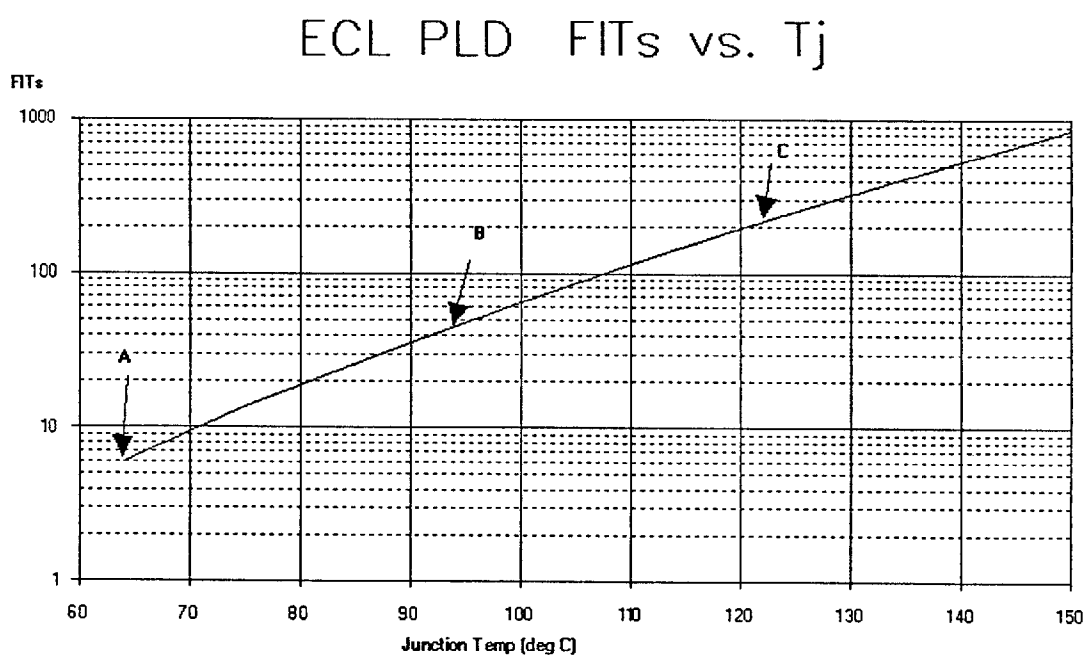


Figure 2. Failures in Time vs Junction Temperature

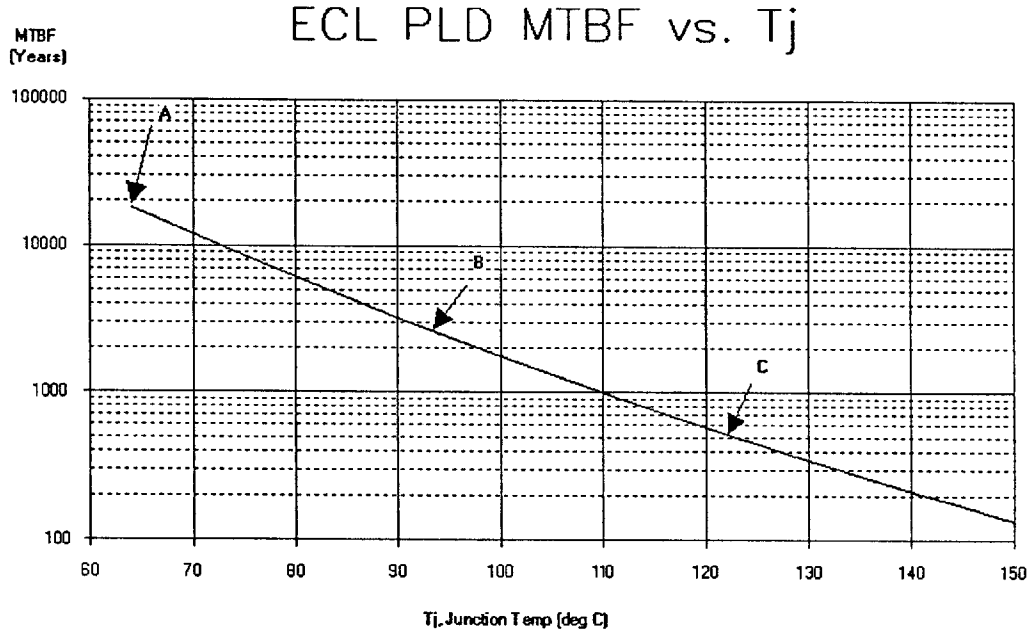


Figure 3. Mean Time Between Failures vs Junction Temp.

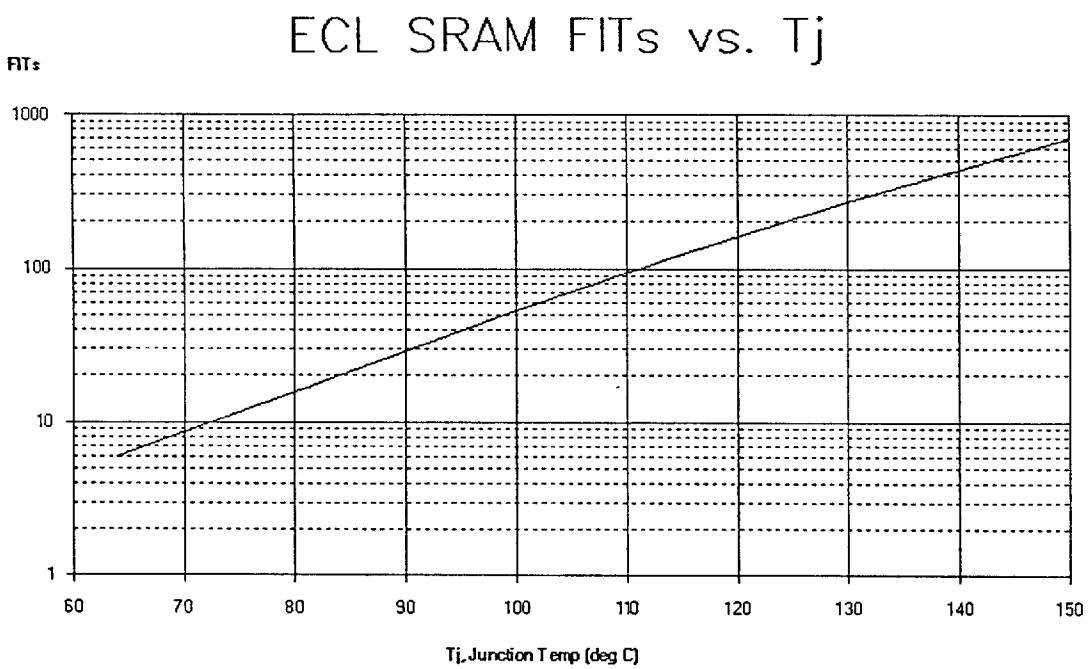


Figure 4. Failures in Time vs Junction Temperature

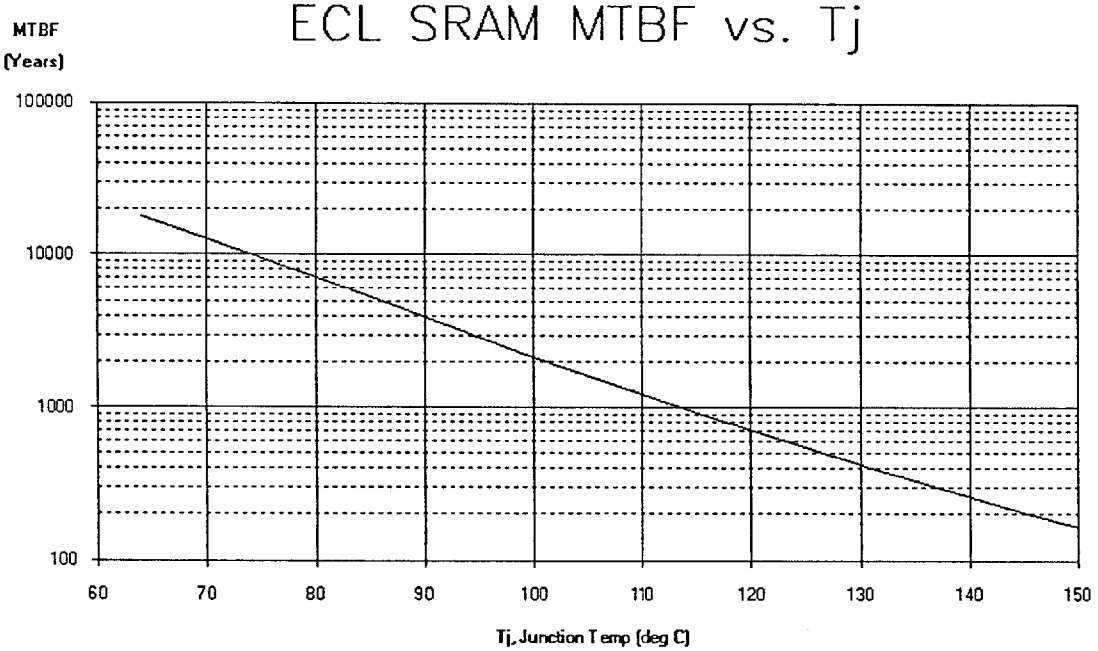


Figure 5. Mean Time Between Failure vs Junction Temp.