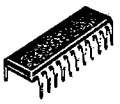
T-52-33-11

LC7990, 7990M


3059


3073A

CMOS LSI

Digital Servo Circuit for HDD, General-Purpose Use

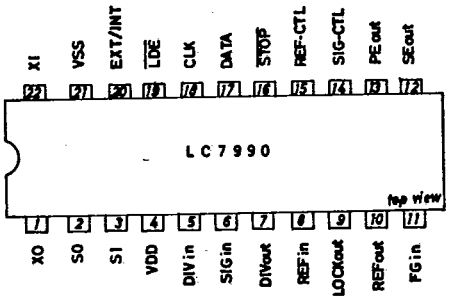
©2239A

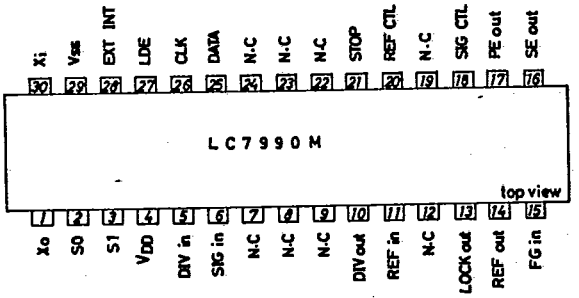
The LC7990, 7990M are digital servo LSIs for HDD (Hard Disk Drive) spindle motor use. Since the LC7990, 7990M contain a serial data input circuit, the servo characteristics can be set by an external microcomputer and the LC7990, 7990M may be also used as a general-purpose digital servo.

Features

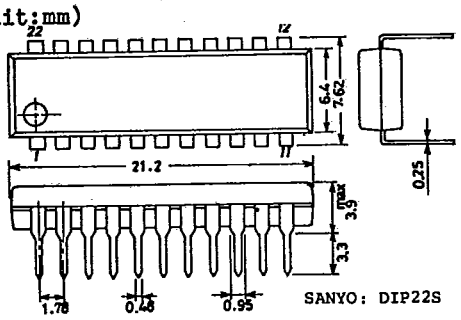
- On-chip speed control circuit and phase control circuit
- On-chip programmable divider for reference signal generation
- On-chip FG (Frequency Generator) signal divider
- Pin-selectable FG Frequency: 4 selections (Internal ROM mode)
- Pin-selectable phase control reference signal (Internal reference signal or external signal)
- Pin-selectable phase control comparison signal (FG division signal or external signal)
- The $\overline{\text{STOP}}$ pin can be used to set the PWM output to "L" level.
- Each control data and division data can be set externally. (External data mode)
- On-chip crystal oscillator. This oscillator can be used as an input amplifier to accept an external clock signal.
- Package: DIP22S (LC7990)
  MFP30 (LC7990M)

Pin Assignment

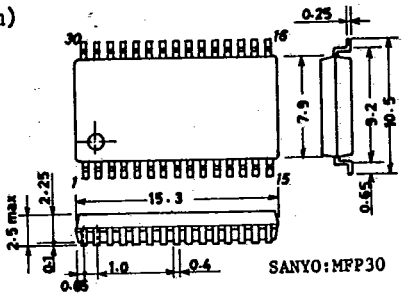




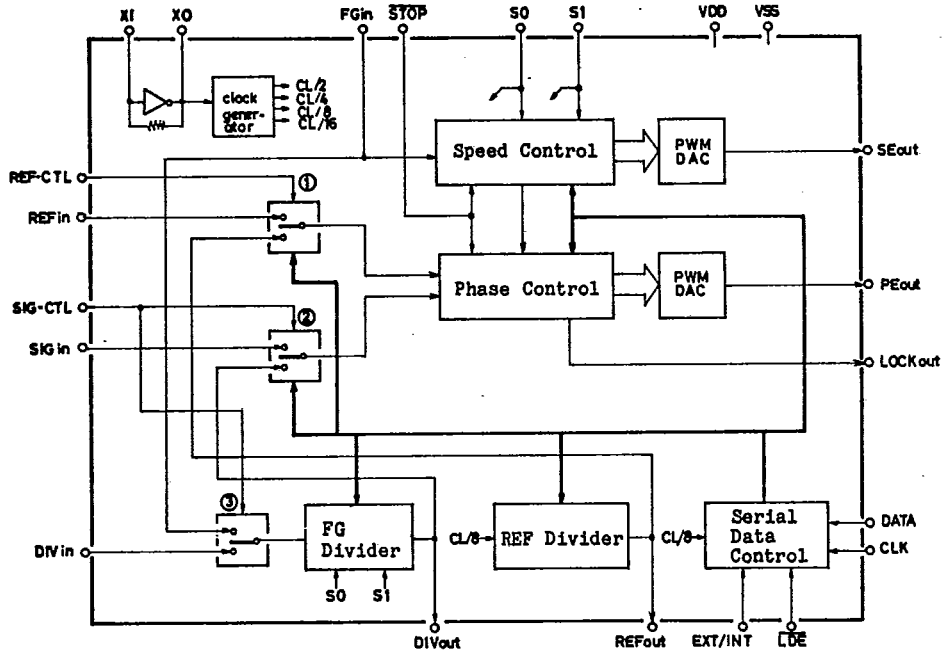
Case Outline 3059-D22SIC
(unit:mm)



Case Outline 3073A-M30IC
(unit:mm)



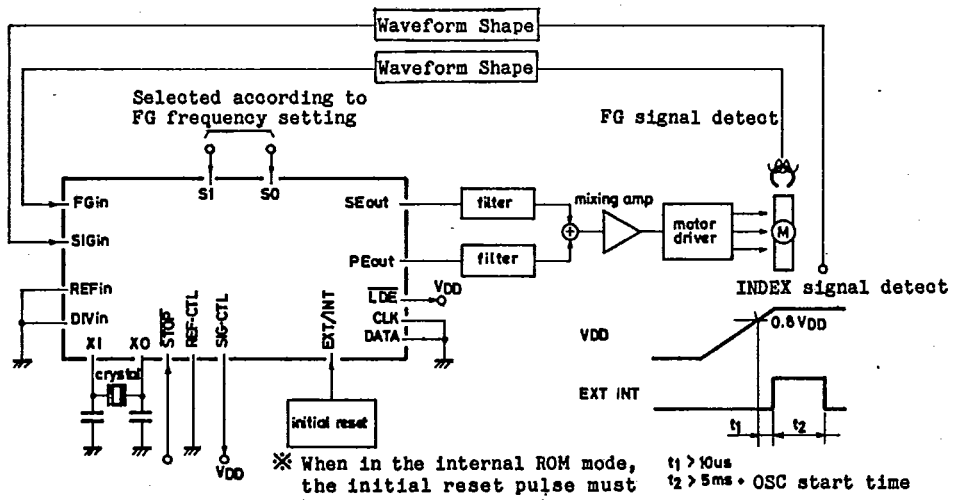
Equivalent Circuit Block Diagram



REF-CTL	①REF-SELECT
L	Internal REF
H	REFin

SIG-CTL	②SIG-SELECT	③DIV-SELECT
L	1/N FGin	FGin
H	SIGin	DIVin

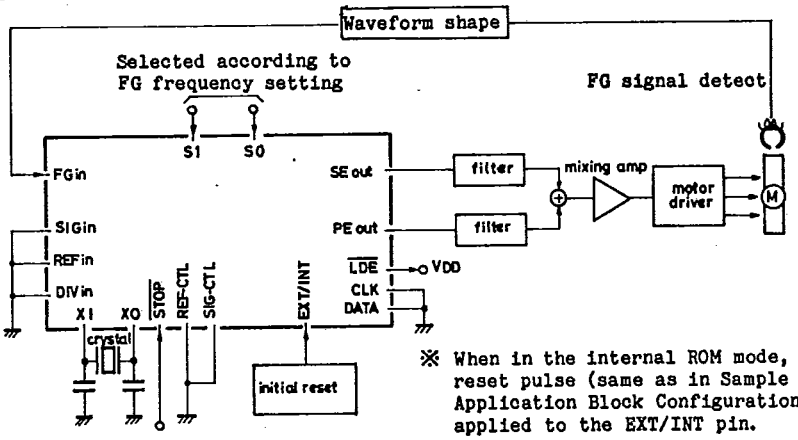
Sample Application Block Configuration 1: Internal ROM mode
(The FG signal, INDEX signal are used jointly.)



※ When in the internal ROM mode, the initial reset pulse must be applied to the EXT/INT pin.

$t_1 > 10us$
$t_2 > 5ms$ + OSC start time

Sample Application Block Configuration 2: Internal ROM mode (FG signal only)



※ When in the internal ROM mode, the initial reset pulse (same as in Sample Application Block Configuration 1) must be applied to the EXT/INT pin.

Pin Description ( ):LC7990M

Pin Name	Pin No.	Function	I/O Configuration
VDD	4(4)	Power supply for LSI V_{SS}=0V V_{DD}=4.5 to 5.5 V	
VSS	21(29)		
S0, S1	2,3(2,3)	Pin used to select the FG frequency	
SIG-CTL	14(18)	Pin used to select the phase control comparison signal "H"→SIGin signal "L"→Internal FG division signal	
REF-CTL	15(20)	Pin used to select the phase control reference signal "H"→REFin signal "L"→Internal REF division signal	
DATA	17(25)	Pin used to input the serial data externally.	
$\overline{LDE}$	19(27)	When inputting the serial data externally, set to "L" level. When in the internal ROM mode, set to "H" level.	
EXT/INT	20(28)	Pin used to select the internal ROM mode (INT)/external data mode (EXT). "H"→EXT mode. Initial reset pin when in the INT mode.	
DIVin	5(5)	Input pin for FG divider. When the SIG-CTL pin is set to "H", the division signal is output at the DIVout pin.	
SIGin	6(6)	Pin used to input the phase control comparison signal	
REFin	8(11)	Pin used to input the phase control reference signal	
FGin	11(15)	Pin used to input the FG signal (rotational speed detect signal) of a motor. This signal is used to provide speed control.	
$\overline{STOP}$	16(21)	Pin used to input the stop signal. The "L"-level input signal sets the SEout, PEout pins to "L".	

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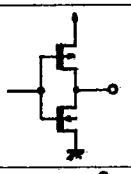
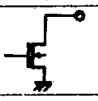
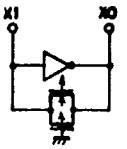
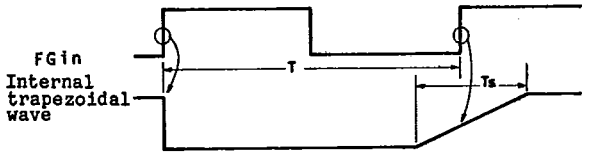
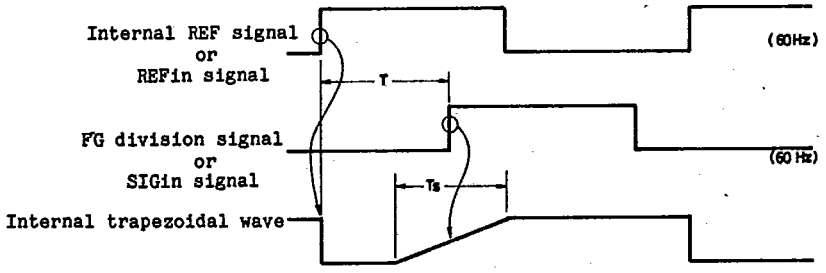
Pin Name	Pin No.	Function	I/O Configuration
CLK	18(26)	Clock pin used when the serial data is input. Fetches the data on the positive transition.	
DIVout	7(10)	Output pin for FG divider	
REFout	10(14)	Output pin for REF divider	
SEout	12(16)	Pin used to output the speed control error signal throught the PWM DAC	
PEout	13(17)	Pin used to output the phase control error signal throught the PWM DAC	
LOCKout	9(13)	Phase lock detect output. The N-ch Tr is turned OFF within the phase slope.	
XI XO	22(30) 1(1)	The crystal oscillator is formed by connecting a crystal resonator of 1MHz to 5MHz externally. The signal generated by this oscillator is used as the system clock. This oscillator may be also used as an input amplifier by capacitive-coupling a signal to the X_I pin.	

Internal Control Data (f_{IN}: X_I pin input frequency=4MHz)



S0	S1	1/T	Ts(ms)	FG signal division
0	0	120Hz	2.048ms	1/2
1	0	240Hz	1.024ms	1/4
0	1	180Hz	1.024ms	1/3
1	1	360Hz	1.024ms	1/6



T=8.333ms
Ts=8.192ms
Internal REF signal frequency=59.995Hz(f_{IN}/66672)

External Serial Data Input

When the EXT/INT pin is set to "H", the servo control characteristics can be set by the serial data externally, instead of the on-chip ROM data.

1. Speed control data

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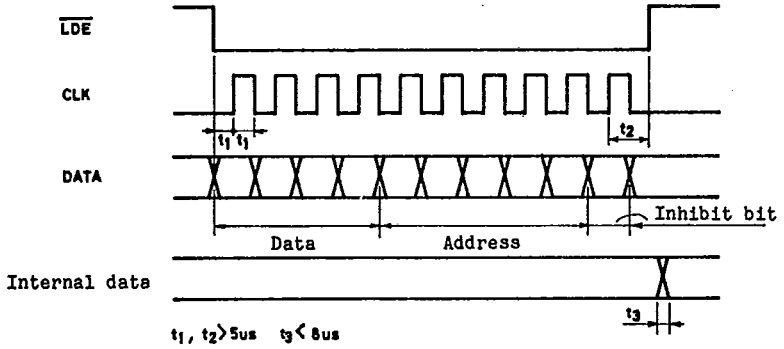
2. Phase control data
3. REF signal division data
4. FG signal division data
5. Selection of phase control reference signal (Same function as for the REF-CTL pin: The REF-CTL pin becomes invalid.)
6. Selection of phase control reference signal (Same function as for the SIG-CTL pin: The SIG-CTL pin becomes invalid.)

Each data is divided into 4-bit pieces. This 4 bits and the address data (5 bits) and the inhibit bit (1 bit) constitute one block (10 bits in all) to be input. When the inhibit bit is set to "1", both speed control and phase control are inhibited. This prevents malfunction which may occur while the data in plurality of blocks are changed.



Input Timing Chart

(1) Speed control data setting range

. Number of bits of Ts setting counter	8 to 11 bits (The number of bits of the PWM-DAC is also the same.)
. Clock of Ts setting counter	CL/2, CL/4, CL/8, CL/16 (CL: X_I input frequency)
. Clock of PWM-DAC	CL/2, CL/4, CL/8, CL/16
. Frequency setting	Approximately 10Hz to 6.25kHz (at 4MHz input)

(2) Phase control data setting range

. Number of bits of Ts setting counter	8 to 11 bits
. Clock of Ts setting counter	CL/2, CL/4, CL/8, CL/16
. Clock of PWM-DAC	CL/2, CL/4, CL/8, CL/16
. Difference in phase setting	Approximately 100us to 100ms (at 4MHz input)

(3) Setting range of REF signal division data

. Number of divisions N	10 to 16,383 division ratio
. Frequency	15.3Hz to 25kHz (at 4MHz input)

f_{REF}=(X_I input frequency) x 1/N x 1/16

(4) Setting range of FG signal division data

. Number of divisions	1 to 64 division ratio The 1/1 division signal is output bypassing the divider.

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +7.0	V
Input Voltage	$V_{I(1)}$	CLK,DATA,$\overline{LDE}$	-0.3 to +7.0	V
	$V_{I(2)}$	Input pins other than $V_{I(1)}$	-0.3 to V_{DD}+0.3	V
Output Voltage	$V_{O(1)}$	LOCKout	-0.3 to +7.0	V
	$V_{O(2)}$	Output pins other than $V_{O(1)}$	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-55 to +125	°C

Allowable Operating Conditions at Ta=-30 to +70°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
"H"-Level Input Voltage	$V_{IH(1)}$	SIG-CTL,$\overline{REF}$-CTL,EXT/$\overline{INT}$,DATA,$\overline{LDE}$	0.7V_{DD}		V_{DD}	V
	$V_{IH(2)}$	SO,S1,DIVin,FGin,SIGin REFin,CLK,$\overline{STOP}$,XI	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	Pin for $V_{IH(1)}$	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	Pin for $V_{IH(2)}$	V_{SS}		0.2V_{DD}	V
Operating Frequency	$F_{IN(1)}$	XI:Capacitive coupling, sine wave,V_{IN}≧0.5Vp-p	1.0		5.0	MHz
	$F_{IN(2)}$	DIVin,FGin:t_{IWH}≧80us			6250	Hz
	$F_{IN(3)}$	SIGin,REFin:t_{IWH}≧100us			1000	Hz
	$F_{IN(4)}$	CLK:t_{IWH}≧5us			100	kHz
Input Amplitude	V_{INP-P}	XI:Capacitive coupling, sine wave input	0.5			Vp-p
"L"-Level Input Pulse Width	t_{WIL}	$\overline{LDE}$	50			us
External Capacitance for Oscillator	Ci	f_{OSC}=4MHz,resonator=X'tal		22		pF
	Co	f_{OSC}=4MHz,resonator=X'tal		22		pF

Electrical Characteristics at Ta=25°C, V_{DD}=5V±10%, V_{SS}=0V

			min	typ	max	unit
"H"-Level Input Current	I_{IH}	Input pins:V_{IN}=V_{DD}			10	uA
"L"-Level Input Current	I_{IL}	Input pins:V_{IN}=V_{SS}	-10			uA
"H"-Level Output Voltage	$V_{OH(1)}$	REFout,DIVout:I_{OH}=-0.3mA	V_{DD}-0.6			V
	$V_{OH(2)}$	SEout,PEout:I_{OH}=-0.3mA	V_{DD}-0.3			V
"L"-Level Output Voltage	$V_{OL(1)}$	Pin for $V_{OH(1)}$:I_{OL}=0.3mA			0.6	V
	$V_{OL(2)}$	Pin for $V_{OH(2)}$:I_{OL}=0.3mA			0.3	V
Oscillation Frequency	f_{OSC}	XI,XO:Resonator=X'tal	1.0		5.0	MHz