



CYPRESS

PRELIMINARY

CY7C455
CY7C456
CY7C457

512 x 18, 1K x 18, and 2K x 18 Cascadable Clocked FIFOs with Programmable Flags

Features

- 512 x 18 (CY7C455), 1,024 x 18 (CY7C456), 2,048 x 18 (CY7C457) FIFO buffer memory
- Expandable in width
- Expandable in depth
- High-speed 70-MHz standalone; 50-MHz cascaded
- Supports free-running 50% duty cycle clock inputs
- Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags
- Parity generation/checking
- Fully asynchronous and simultaneous read and write operation
- Output Enable (OE) pin
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- 52-pin PLCC and 52-pin PQFP
- Proprietary 0.8μ CMOS technology
- TTL compatible

Functional Description

The CY7C455, CY7C456, and CY7C457 are high-speed, low-power, first-in-first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide. The CY7C455 has a 512-word memory array, the CY7C456 has a 1,024-word memory array, and the CY7C457 has a 2,048-word memory array. The CY7C455, CY7C456, and CY7C457 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Empty flags and generation/checking of parity. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

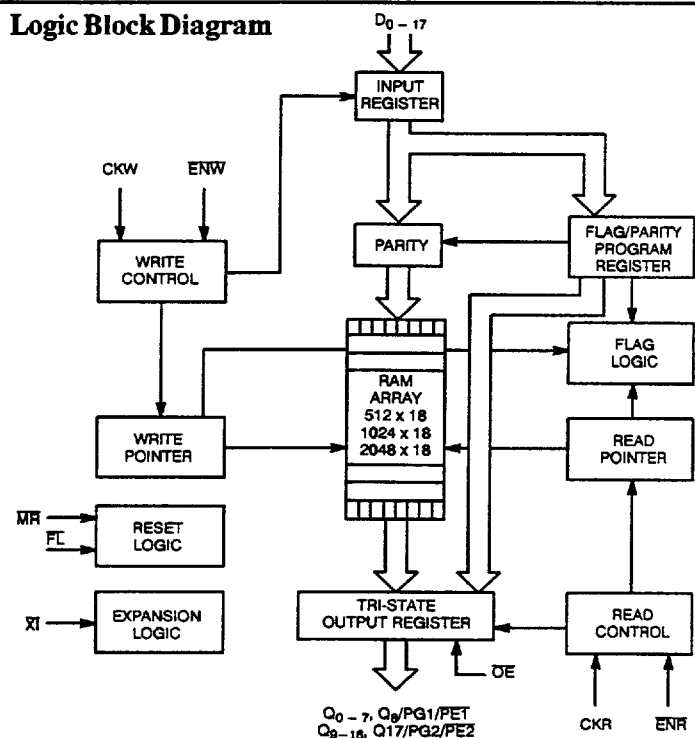
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (CKW) and a write enable pin (ENW).

When ENW is asserted, data is written into the FIFO on the rising edge of the

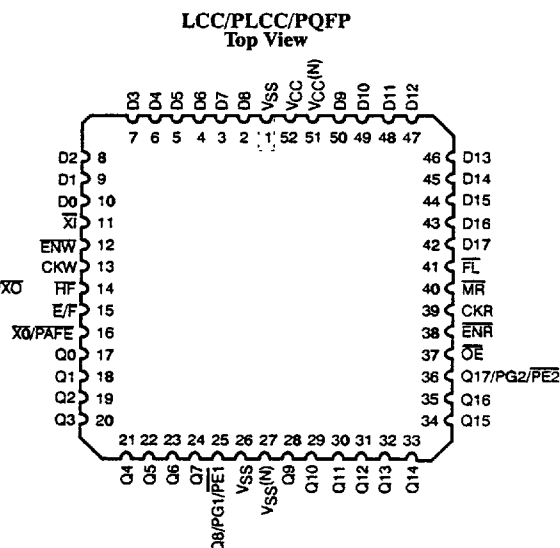
CKW signal. While ENW is held active, data is continually written into the FIFO on each CKW cycle. The output port is controlled in a similar manner by a free-running read clock (CKR) and a read enable pin (ENR). In addition, the CY7C455, CY7C456, and CY7C457 have an output enable pin (OE). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 71.4 MHz are achievable in the standalone configuration, and up to 50 MHz is achievable when FIFOs are cascaded for depth expansion.

Depth expansion is possible using the cascade input (XI), cascade output (XO), and First Load (FL) pins. The XO pin is connected to the XI pin of the next device, and the XO pin of the last device should be connected to the XI pin of the first device. The FL pin of the first device is tied to V_{SS}.

Logic Block Diagram



Pin Configuration



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Functional Description (continued)

The CY7C455, CY7C456, and CY7C457 provide three status pins. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than or Equal to Half Full, Greater than Half Full, Almost Full, and Full (see *Table 1*). The Almost Empty/Full flag (PAFE) shares the \overline{XO} pin on the CY7C455, CY7C456, and CY7C457. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out (\overline{XO}) information that is used to signal the next FIFO when it will be activated.

The flags are synchronous, i.e., they change state relative to either the read clock (CKR) or the write clock (CKW). When entering or exiting the Empty and Almost Empty states, the flags are updated

exclusively by the CKR. The flags denoting Half Full, Almost Full, and Full states are updated exclusively by CKW. The synchronous flag architecture guarantees that the flags maintain their status for some minimum time. This time is typically equal to approximately one cycle time.

The CY7C45X uses center power and ground for reduced noise. All configurations are fabricated using an advanced 0.8 μ N-well CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings and a substrate bias generator.

Selection Guide

		7C45X-14	7C45X-20	7C45X-30
Maximum Frequency (MHz)		71.4 ^[1]	50	33.3
Maximum Cascadable Frequency		N/A	50	33.3
Maximum Access Time (ns)		10	15	20
Minimum Cycle Time (ns)		14	20	30
Minimum Clock HIGH Time (ns)		6.5	9	12
Minimum Clock LOW Time (ns)		6.5	9	12
Minimum Data or Enable Set-Up (ns)		5	7	9
Minimum Data or Enable Hold (ns)		1	1	1
Maximum Flag Delay (ns)		10	15	20
Maximum Current (mA)	Commercial	160	140	120
	Military/Industrial	180	160	140

	CY7C455	CY7C456	CY7C457
Density	512 x 18	1,024 x 18	2,048 x 18
\overline{OE} , Depth Cascadable	Yes	Yes	Yes
Package	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP	52-Pin LCC/PLCC/PQFP

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 65°C to +150°C
Ambient Temperature with
Power Applied - 55°C to +125°C
Supply Voltage to Ground Potential - 0.5V to +7.0V
DC Voltage Applied to Outputs
in High Z State - 0.5V to +7.0V
DC Input Voltage - 3.0V to +7.0V
Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V \pm 10%
Industrial	- 40°C to +85°C	5V \pm 10%
Military ^[2]	- 55°C to +125°C	5V \pm 10%

Note:

- 71.4-MHz operation is available only in the standalone configuration.
- T_A is the "instant on" case temperature.



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Pin Definitions

Signal Name	I/O	Description
D ₀ – 17	I	Data Inputs: When the FIFO is not full and ENW is active, CKW (rising edge) writes data (D ₀ – 17) into the FIFO's memory. If MR is asserted at the rising edge of CKW, data is written into the FIFO's programming register. D ₈ , 17 are ignored if the device is configured for parity generation.
Q ₀ – 7 Q ₉ – 16	O	Data Outputs: When the FIFO is not empty and ENR is active, CKR (rising edge) reads data (Q ₀ – 7, Q ₉ – 16) out of the FIFO's memory. If MR is active at the rising edge of CKR, data is read from the programming register.
Q ₈ /PG1/PE1 Q ₁₇ /PG2/PE2	O	Function varies according to mode: Parity disabled – same function as Q ₀ – 7 and Q ₉ – 16 Parity enabled, generation – parity generation bit (PG _x) Parity enabled, check – Parity Error Flag (PE _x)
ENW	I	Enable Write: Enables the CKW input (for both non-program and program modes).
ENR	I	Enable Read: Enables the CKR input (for both non-program and program modes).
CKW	I	Write Clock: The rising edge clocks data into the FIFO when ENW is LOW; updates Half Full, Almost Full, and Full flag states. When MR is asserted, CKW writes data into the program register.
CKR	I	Read Clock: The rising edge clocks data out of the FIFO when ENR is LOW; updates the Empty and Almost Empty flag states. When MR is asserted, CKR reads data out of the program register.
HF	O	Half Full Flag: Synchronized to CKW.
E/F	O	Empty or Full Flag: E is synchronized to CKR; F is synchronized to CKW.
PAFE/XO	O	Dual-Mode Pin: Not Cascaded – programmable Almost Full is synchronized to CKW; Programmable Almost Empty is synchronized to CKR. Cascaded – expansion out signal, connected to XI of next device.
XI	I	Expansion-In Pin: Not Cascaded – XI is tied to V _{SS} . Cascaded – expansion Input, connected to XO of previous device.
FL	I	First Load Pin: Cascaded – the first device in the daisy chain will have FL tied to V _{SS} ; all other devices will have FL tied to V _{CC} (Figure 1). Not Cascaded – tied to V _{CC} .
MR	I	Master Reset: Resets device to empty condition. Non-Programming Mode: Program register is reset to default condition of no parity and PAFE active at 16 or less locations from Full/Empty. Programming Mode: Data present on D ₀ – 8 is written into the programmable register on the rising edge of CKW. Program register contents appear on Q ₀ – 8 after the rising edge of CKR.
OE	I	Output Enable for Q ₀ – 7, Q ₉ – 16, Q ₈ /PG1/PE1 and Q ₁₇ /PG2/PE2 pins.



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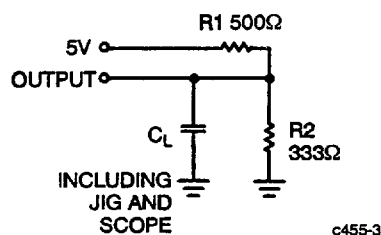
Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C45X-14		7C45X-20		7C45X-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 2.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH} ^[4]	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL} ^[4]	Input LOW Voltage		- 3.0	0.8	- 3.0	0.8	- 3.0	0.8	V
I _{IX}	Input Leakage Current	V _{CC} = Max.	- 10	+10	- 10	+10	- 10	+10	μA
I _{OS} ^[5]	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND	- 90		- 90		- 90		mA
I _{OZL} I _{OZH}	Output OFF, High Z Current	OE ≥ V _{IH} , V _{SS} < V _O < V _{CC}	- 10	+ 10	- 10	+ 10	- 10	+ 10	μA
I _{CC1} ^[6]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	160		140		120	mA
			Mil/Ind	180		160		140	mA
I _{CC2} ^[7]	Operating Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	90		90		90	mA
			Mil/Ind	100		100		100	mA
I _{SB} ^[8]	Standby Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	40		40		40	mA
			Mil/Ind	40		40		40	mA

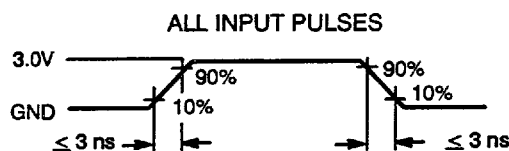
Capacitance^[9]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		12	pF

AC Test Loads and Waveforms^[10, 11, 12, 13, 14]



Equivalent to: THÉVENIN EQUIVALENT
200Ω
OUTPUT — 2V



Notes:

- See the last page of this specification for Group A subgroup testing information.
- The V_{IH} and V_{IL} specifications apply for all inputs except **XI** and **FL**. The **XI** pin is not a TTL input. It is connected to either **XO** of the previous device or V_{SS}. **FL** must be connected to either V_{SS} or V_{CC}.
- Test no more than one output at a time for not more than one second.
- Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at f_{MAX}/2. Outputs are unloaded.
- Input signals switch from 0V to 3V with a rise/fall time less than 3 ns, clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz. Outputs are unloaded.
- All input signals are connected to V_{CC}. All outputs are unloaded. Read and write clocks switch at maximum frequency (f_{MAX}).
- Tested initially and after any design or process changes that may affect these parameters.
- C_L = 30 pF for all AC parameters except for t_{OHZ}.
- C_L = 5 pF for t_{OHZ}.
- All AC measurements are referenced to 1.5V except t_{OE}, t_{OLZ}, and t_{OHZ}.
- t_{OE} and t_{OLZ} are measured at ± 100 mV from the steady state.
- t_{OHZ} is measured at +500 mV from V_{OL} and - 500 mV from V_{OH}.



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Switching Characteristics Over the Operating Range^[3, 15]

Parameter	Description	7C45X-14		7C45X-20		7C45X-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CKW}	Write Clock Cycle	14		20		30		ns
t _{CKR}	Read Clock Cycle	14		20		30		ns
t _{CKH}	Clock HIGH	6.5		9		12		ns
t _{CKL}	Clock LOW	6.5		9		12		ns
t _A	Data Access Time		10		15		20	ns
t _{OH}	Previous Output Data Hold After Read HIGH	0		0		0		ns
t _{FH}	Previous Flag Hold After Read/Write HIGH	0		0		0		ns
t _{SD}	Data Set-Up	5		7		9		ns
t _{HD}	Data Hold	1		1		1		ns
t _{SEN}	Enable Set-Up	5		7		9		ns
t _{HEN}	Enable Hold	1		1		1		ns
t _{OE}	\overline{OE} LOW to Output Data Valid		10		15		20	ns
t _{OLZ} ^[9, 16]	\overline{OE} LOW to Output Data in Low Z	0		0		0		ns
t _{OHZ} ^[9, 16]	\overline{OE} HIGH to Output Data in High Z		10		15		20	ns
t _{PG}	Read HIGH to Parity Generation		10		15		20	ns
t _{PE}	Read HIGH to Parity Error Flag		10		15		20	ns
t _{FD}	Flag Delay		10		15		20	ns
t _{SKEW1} ^[17]	Opposite Clock After Clock	0		0		0		ns
t _{SKEW2} ^[18]	Opposite Clock Before Clock	14		20		30		ns
t _{PMR}	Master Reset Pulse Width (\overline{MR} LOW)	14		20		30		ns
t _{SCMR}	Last Valid Clock Low Set-Up to \overline{MR} LOW	0		0		0		ns
t _{OHMR}	Data Hold From \overline{MR} LOW	0		0		0		ns
t _{MRR}	Master Reset Recovery (\overline{MR} HIGH Set-Up to First Enabled Write/Read)	14		20		30		ns
t _{MRF}	\overline{MR} HIGH to Flags Valid		14		20		30	ns
t _{AMR}	\overline{MR} HIGH to Data Outputs LOW		14		20		30	ns
t _{SMRP}	Program Mode— \overline{MR} LOW Set-Up	14		20		30		ns
t _{HMRP}	Program Mode— \overline{MR} LOW Hold	10		15		20		ns
t _{FTP}	Program Mode—Write HIGH to Read HIGH	14		20		30		ns
t _{AP}	Program Mode—Data Access Time		14		20		30	ns
t _{OHP}	Program Mode—Data Hold Time from \overline{MR} HIGH	0		0		0		ns

Notes:

15. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and output loading as shown in AC Test Loads and Waveforms and capacitance as in notes 10 and 11, unless otherwise specified.
16. At any given temperature and voltage condition, t_{OLZ} is greater than t_{OHZ} for any given device.
17. t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. Note: The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite

clock for Empty and Almost Empty flags, and CKR is the the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, and CKR is the clock for Empty and Almost Empty flags.

18. t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. See Note 17 for definition of clock and opposite clock.

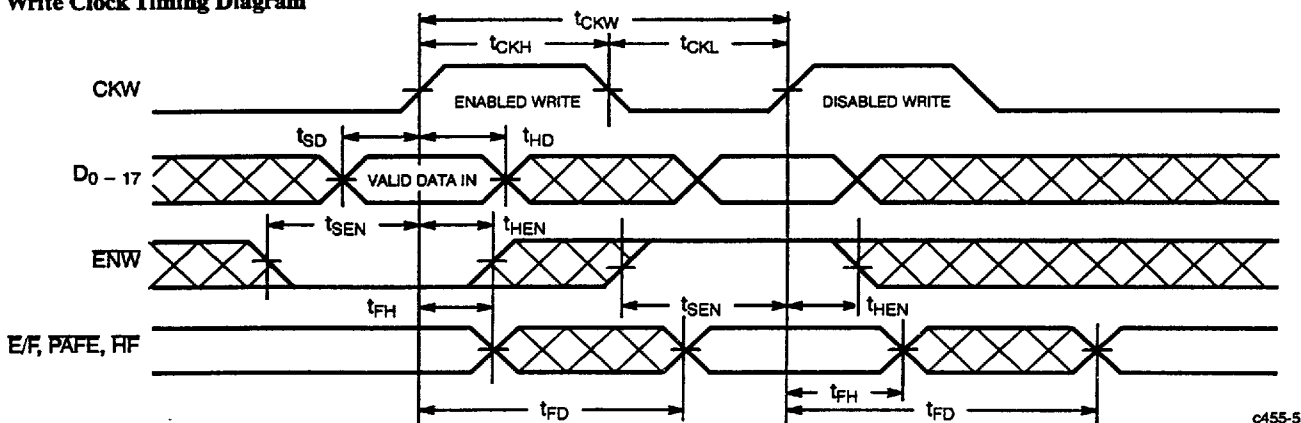


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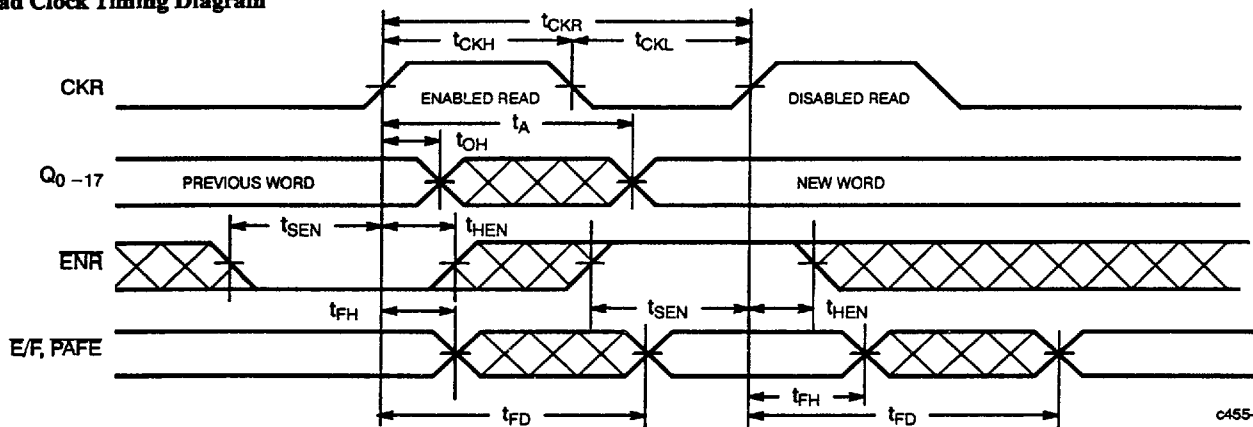
Switching Waveforms

Write Clock Timing Diagram



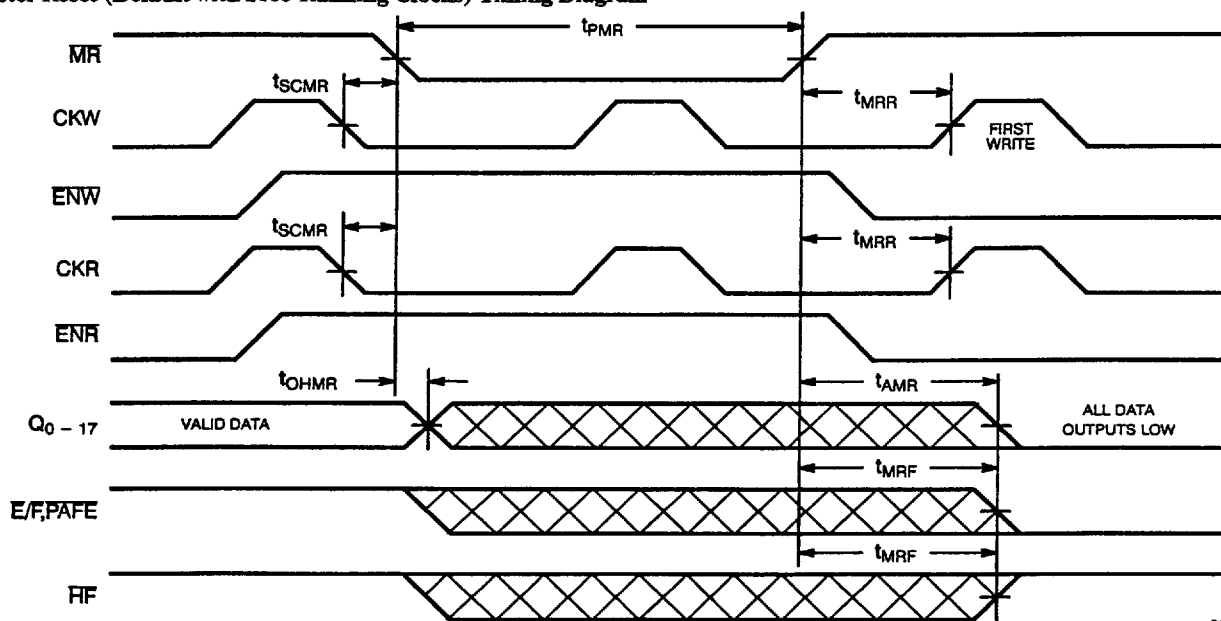
c455-5

Read Clock Timing Diagram



c455-6

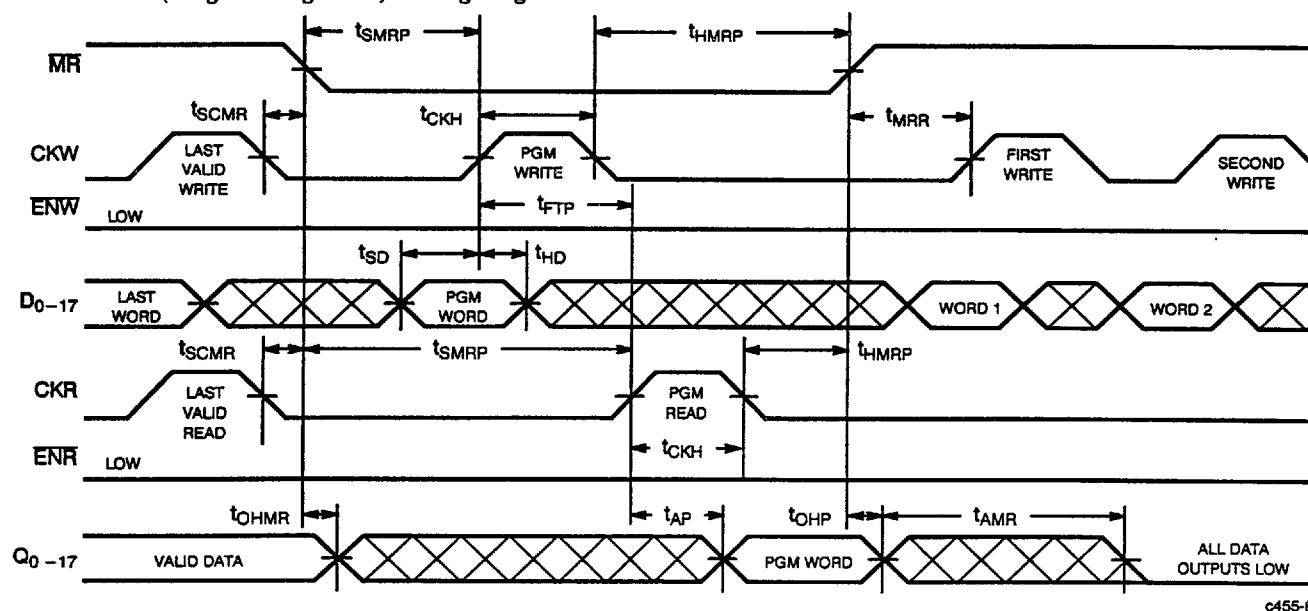
Master Reset (Default with Free-Running Clocks) Timing Diagram^[19, 20, 21, 22]



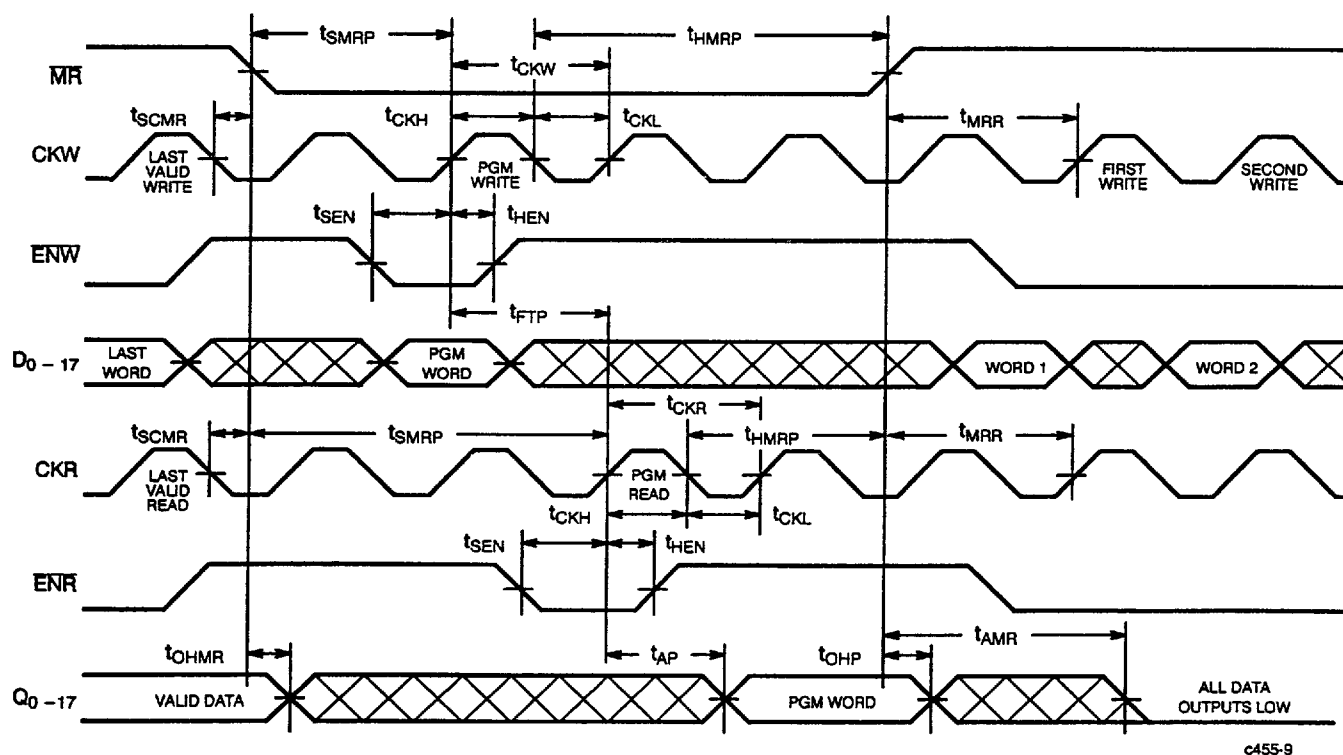
c455-7



Master Reset (Programming Mode) Timing Diagram^[21, 22]



Master Reset (Programming Mode with Free-Running Clocks) Timing Diagram^[21, 22]



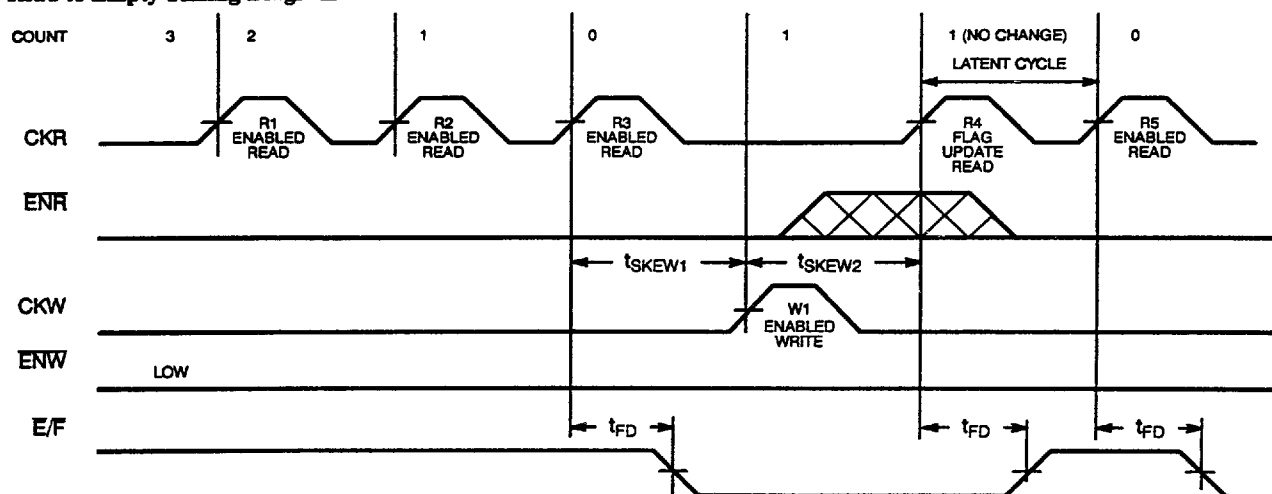
21. All data outputs ($Q_0 - 17$) go LOW as a result of the rising edge of \overline{MR} after t_{AMR} .
22. In this example, $Q_0 - 17$ will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.



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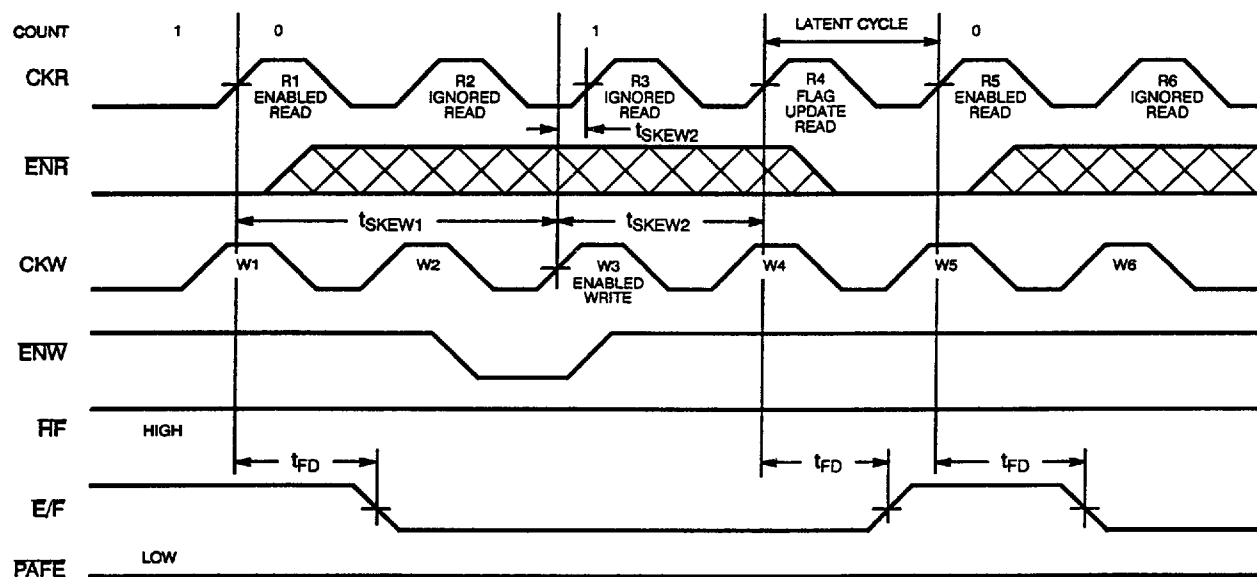
Switching Waveforms (continued)

Read to Empty Timing Diagram^[23, 26, 27]



c455-11

Read to Empty Timing Diagram with Free-Running Clocks^[23, 24, 25, 26]



c455-10

Notes:

23. "Count" is the number of words in the FIFO.
24. The FIFO is assumed to be programmed with $P > 0$ (i.e., PAFE does not transition at Empty or Full).
25. R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.
26. CKR is clock and CKW is opposite clock.
27. R3 updates the flag to the Empty state by asserting E/F. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to Almost Empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of ENR. It does not change the count or the FIFO's data outputs.

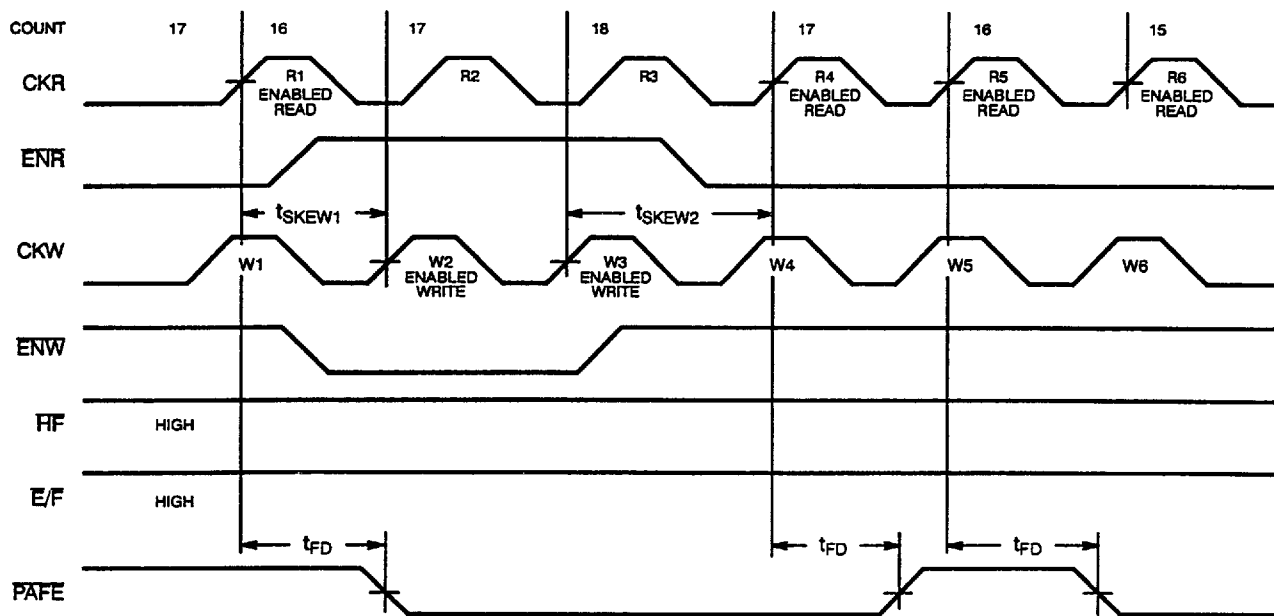


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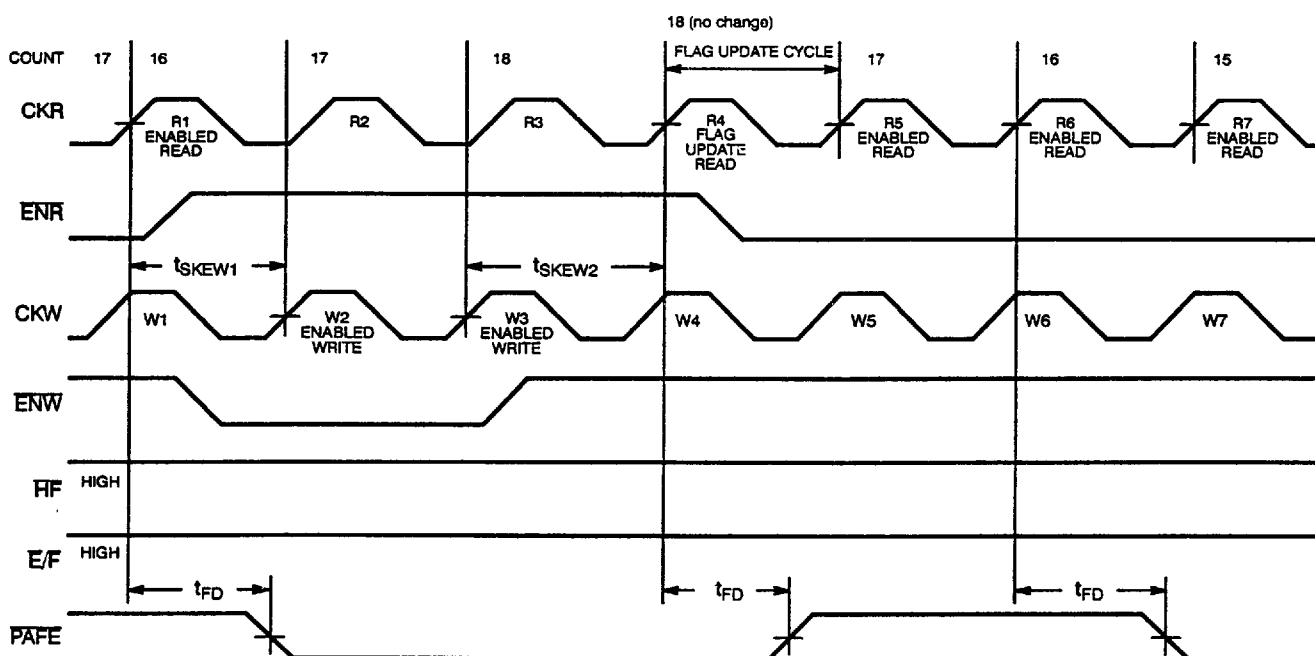
Switching Waveforms (continued)

Read to Almost Empty Timing Diagram with Free-Running Clocks^[23, 26, 28]



c455-13

Read to Almost Empty Timing Diagram with Read Flag Update Cycle with Free-Running Clocks^[23, 26, 28, 29, 30]



c455-12

Notes:

28. The FIFO in this example is assumed to be programmed to its default flag values. Almost Empty is 16 words from Empty; Almost Full is 16 locations from Full.
29. R4 only updates the flag status. It does not affect the count because ENR is HIGH.
30. When making the transition from Almost Empty to Intermediate, the count must increase by two (16 + 18; two enabled writes: W2, W3) before a read (R4) can update flags to the Less Than Half Full state.

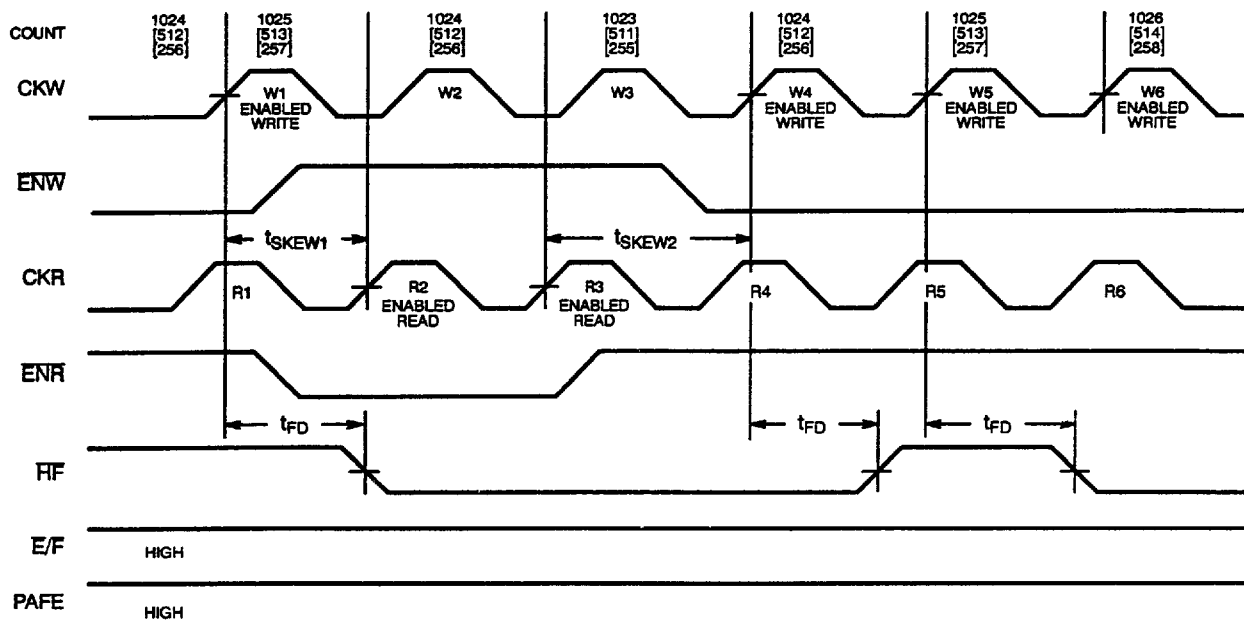


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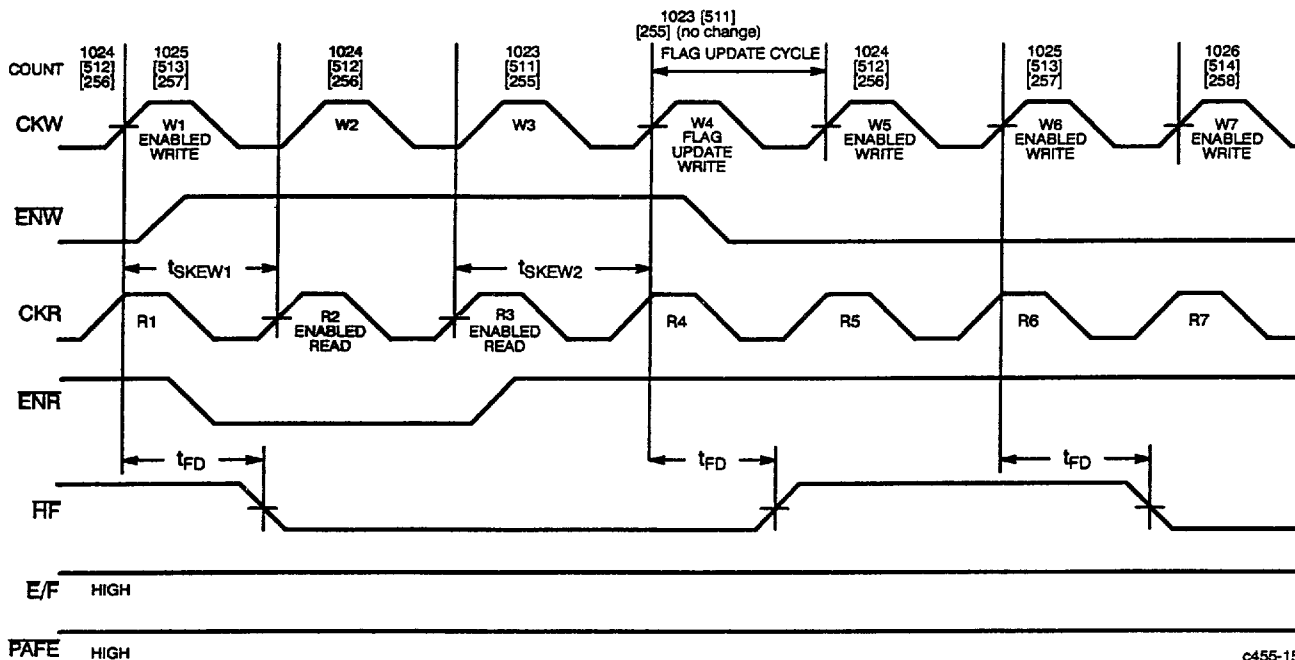
Switching Waveforms (continued)

Write to Half Full Timing Diagram with Free-Running Clocks^[23, 31, 32, 33]



c455-14

Write to Half Full Timing Diagram with Write Flag Update Cycle with Free-Running Clocks^[23, 31, 32, 33, 34, 35]



c455-15

Notes:

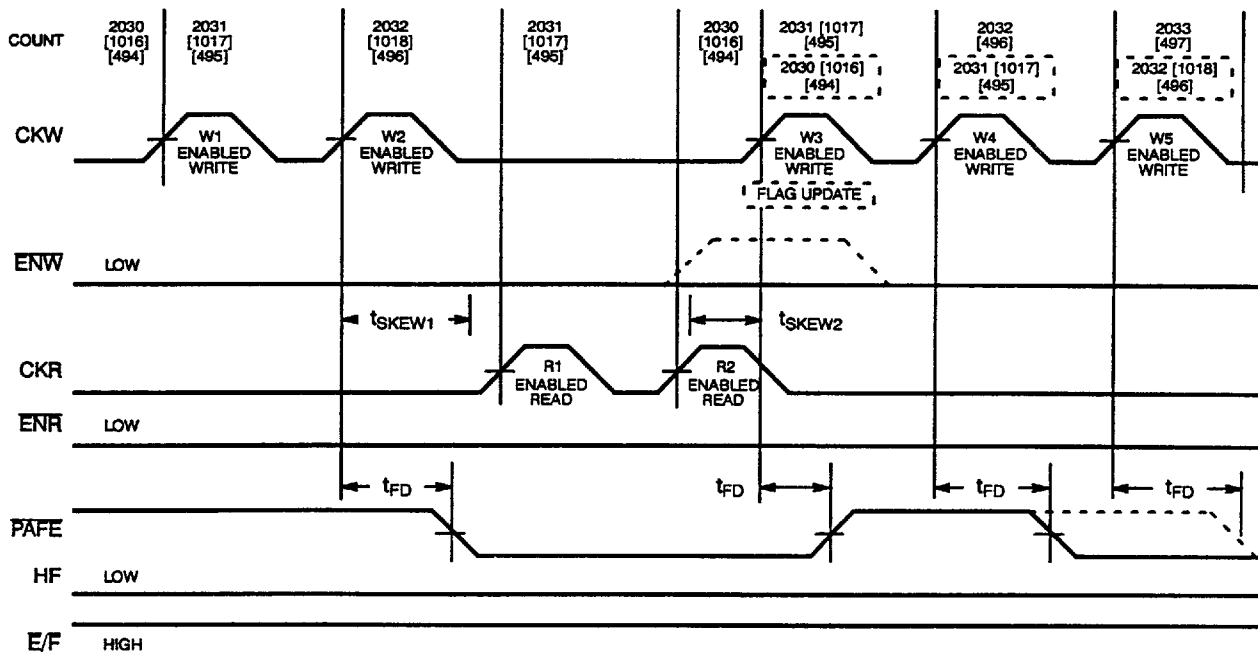
31. CKW is clock and CKR is opposite clock.
32. Count = 1,025 indicates Half Full for the CY7C446 and CY7C456. Count = 513 indicates Half Full for the CY7C447 and CY7C457. Count = 257 indicates Half Full for the CY7C448 and CY7C458.
33. When the FIFO contains 1,024 [512] [256] words, the rising edge of the next enabled write causes the HF to be true (LOW).
34. The HF write flag update cycle does not affect the count because ENW is HIGH. It only updates HF to HIGH.
35. When making the transition from Half Full to Less Than Half Full, the count must decrease by two (i.e., 1,025 to 1,023; two enabled reads: R2 and R3) before a write (W4) can update flags to less than Half Full.



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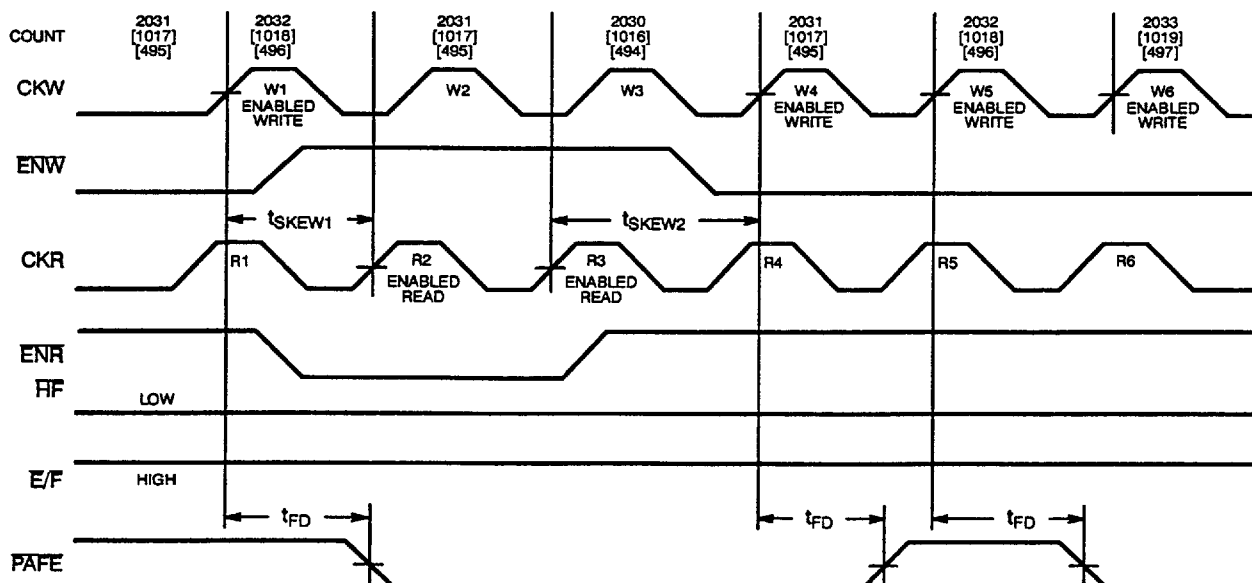
Switching Waveforms (continued)

Write to Almost Full Timing Diagram^[23, 28, 31, 36, 37]



c455-17

Write to Almost Full Timing Diagram with Free-Running Clocks^[23, 28, 31]



c455-16

Notes:

36. W2 updates the flag to the Almost Full state by asserting PAFE. Because R1 occurs greater than t_{SKEW1} after W2, W2 does not recognize R1 when updating flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.

37. The dashed lines show W3 as a flag update write rather than an enabled write because ENW is HIGH.

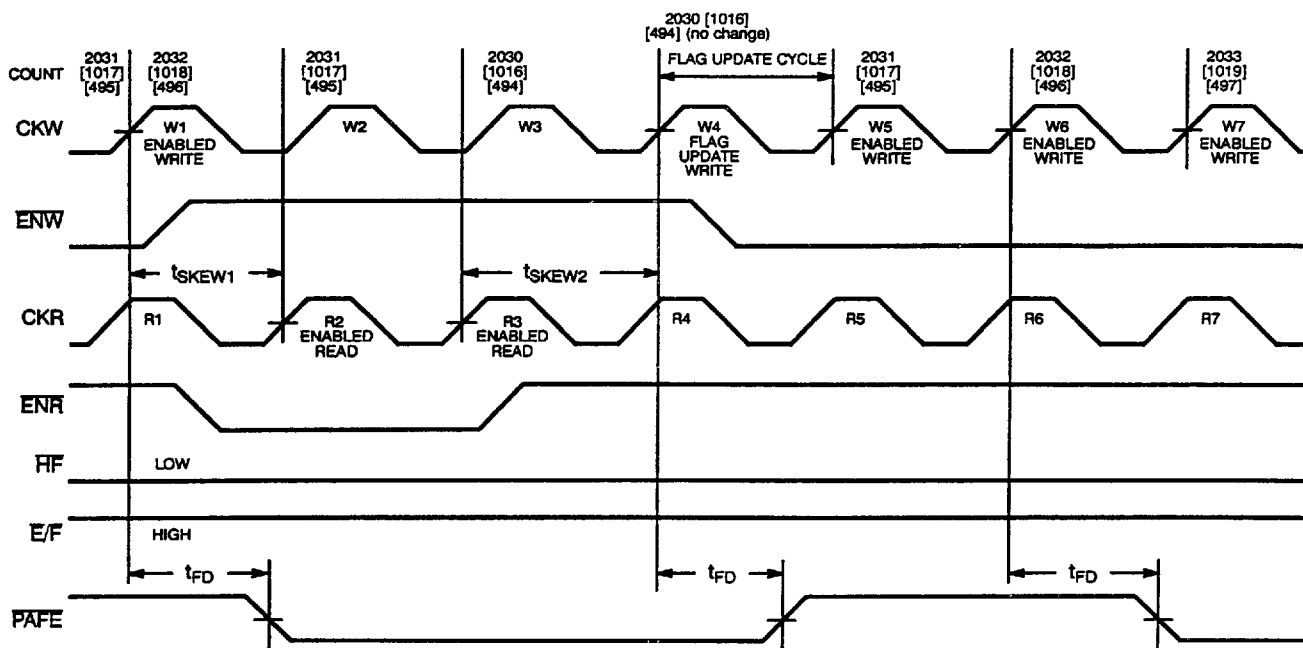


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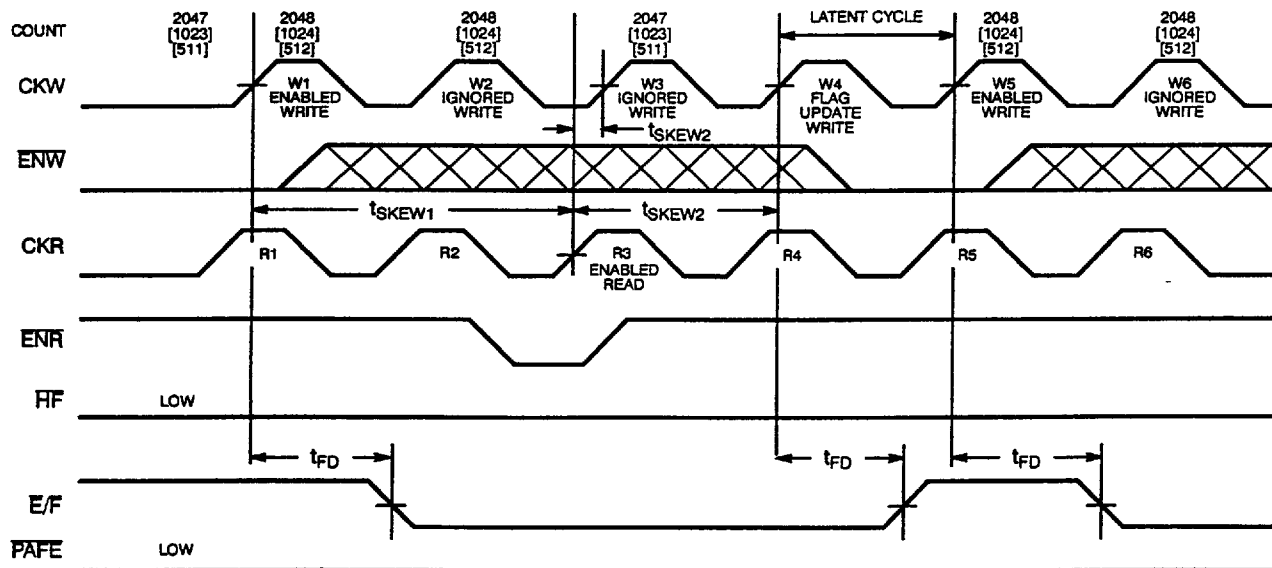
Switching Waveforms (continued)

Write to Almost Full Timing Diagram with Write Flag Update Cycle and Free-Running Clocks^[23, 28, 31]



c455-18

Write to Full Flag Timing Diagram with Free-Running Clocks^[23, 31, 38]



c455-19

Note:

38. W2 is ignored because the FIFO is full (count = 2,048 [1,024] [512]). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore,

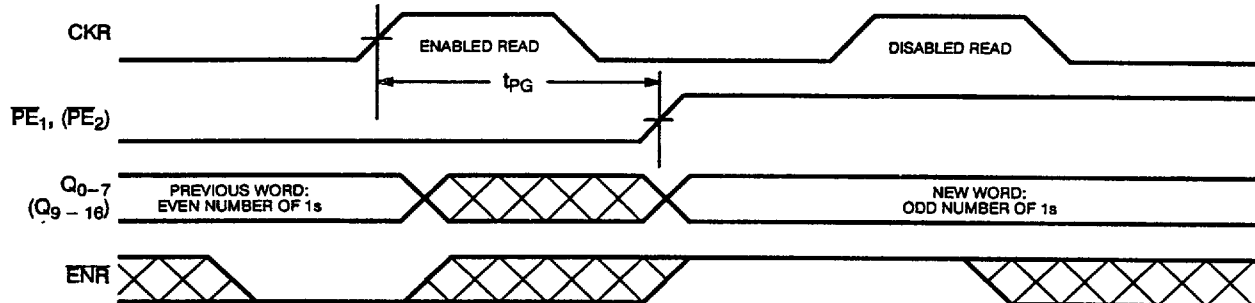
the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.



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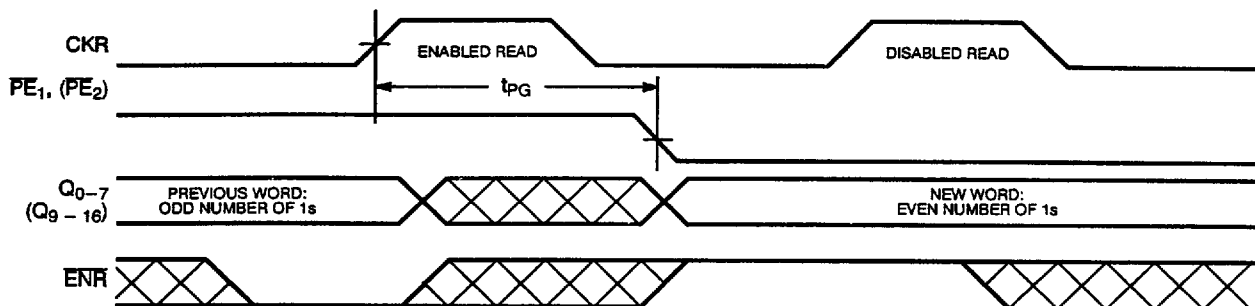
Switching Waveforms (continued)

Even Parity Generation Timing Diagram^[39, 40]



c455-20

Even Parity Generation Timing Diagram^[39, 41]



c455-21

Notes:

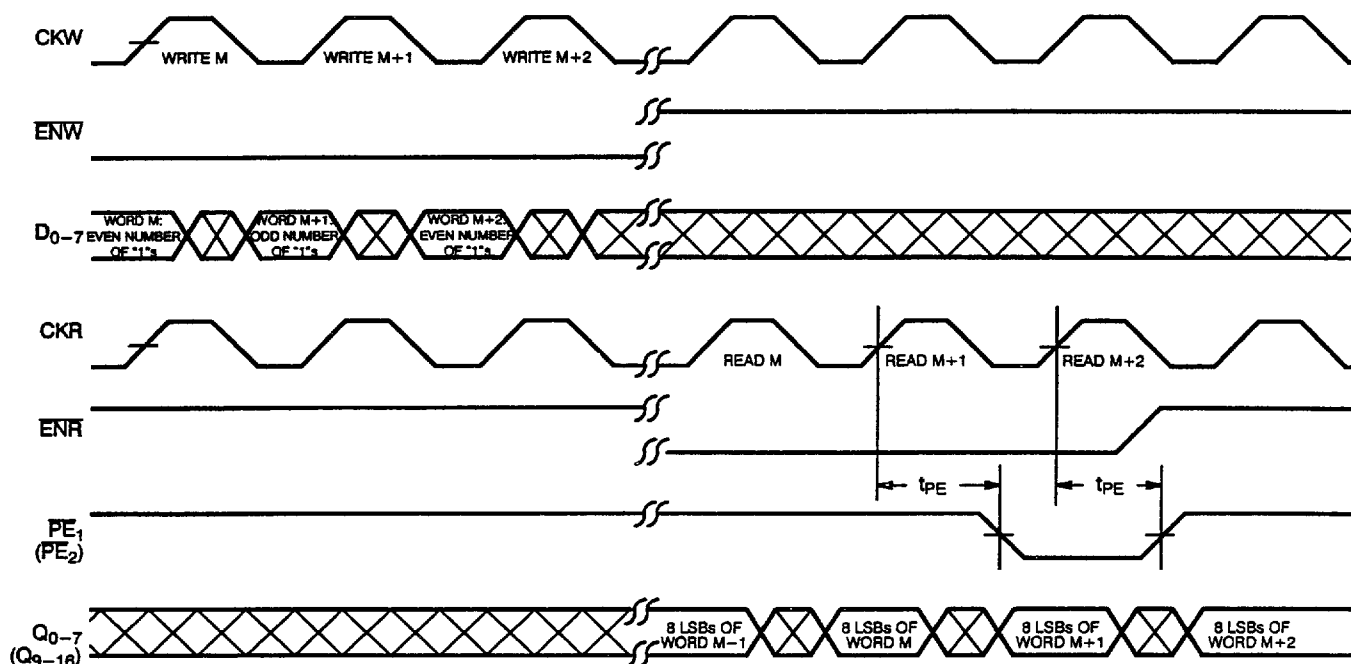
39. In this example, the FIFO is assumed to be programmed to generate even parity. The Q₀₋₇ word is shown. The example is similar for the Q₉₋₁₆ word.
40. If Q₀₋₇ "new word" also has an even number of 1s, then PG1 stays LOW.
41. If Q₀₋₇ "new word" also has odd number of 1s, then PG1 stays HIGH.



PRELIMINARY

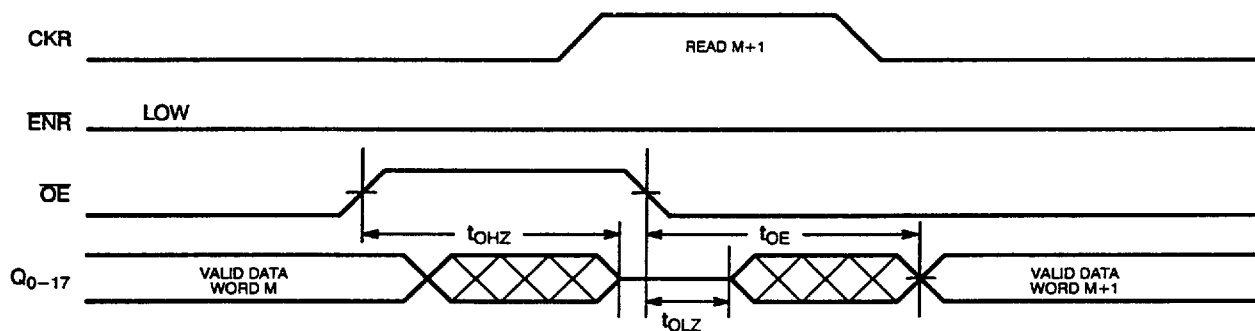
Switching Waveforms (continued)

Even Parity Checking^[42]



c455-22

Output Enable Timing^[43, 44]



c455-23

Notes:

42. In this example, the FIFO is assumed to be programmed to check for even parity. The Q₀₋₇ word is shown.
43. This example assumes that the time from the CKR rising edge to valid word M+1 $\geq t_A$. The Q₀₋₇ word is shown.
44. If ENR was HIGH around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of word M+1.



PRELIMINARY

CY7C455
CY7C456
CY7C457

Architecture

The CY7C45X consists of an array of 512, 1,024, or 2,048 words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (CKR, CKW, ENR, ENW, and MR), and flags (HF, E/F, PAFE). The CY7C45X also includes the control signals OE, FL, XI, and XO for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset (MR) cycle. This causes the FIFO to enter the Empty condition signified by E/F and PAFE being LOW and HF being HIGH. All data outputs (Q₀ - 17) go low at the rising edge of MR. In order for the FIFO to reset to its default state, a falling edge must occur on MR and the user must not read or write while MR is LOW (unless ENR and/or ENW are HIGH or unless the device is being programmed). Upon completion of the master reset cycle, all data outputs will go LOW t_{AMR} after MR is deasserted. All flags are guaranteed to be valid t_{MRF} after MR is taken HIGH.

FIFO Operation

When the ENW signal is active (LOW), data present on the D₀ - 17 pins is written into the FIFO on each rising edge of the CKW signal. Similarly, when the ENR signal is active, data in the FIFO memory will be presented on the Q₀ - 17 outputs. New data will be presented on each rising edge of CKR while ENR is active. ENR must set up t_{SEN} before CKR for it to be a valid read function. ENW must occur t_{SEN} before CKW for it to be a valid write function.

An output enable (OE) pin is provided to three-state the Q₀ - 17 outputs when OE is asserted. When OE is enabled (low), data in the output register will be available to the Q₀ - 17 outputs after t_{OE}. If devices are cascaded, the OE function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q₀ - 17 outputs even after additional reads occur.

Programming

The CY7C45X is programmed during a master reset cycle. If MR and ENW are LOW, a rising edge on CKW will write the D₀ - 9, 10 or 11 inputs into the programming register^[45]. MR must be set up a minimum of t_{SMRP} before the program write rising edge and held

t_{HMRP} after the program write falling edge. The user has the ability to also perform a program read during the master reset cycle. This will occur at the rising edge of CKR when MR and ENR are asserted. The program read must be performed a minimum of t_{FTP} after a program write, and the program word will be available t_{AP} after the read occurs. If a program write does not occur, a program read may occur a minimum of t_{SMRP} after MR is asserted. This will read the default program value.

When free-running clocks are tied to CKW and CKR, programming can still occur during a master reset cycle with the adherence to a few additional timing parameters. The enable pins must be set-up t_{SEN} before the rising edge of CKW or CKR. Hold times of t_{HEN} must also be met for ENW and ENR.

Data present on D₀ - 9 during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags will become active. See Table 1 for a description of the six possible FIFO states. P in Table 1 refers to the decimal equivalent of the binary number represented by D₀ - 7, 8 or 9. Programming options for the CY7C45X are listed in Table 4.

The programmable PAFE function on the CY7C45X is only valid when not cascaded. If the user elects not to program the FIFO's flags, the default is as follows: the Almost Empty condition (Almost Full condition) is activated when the FIFO contains 16 or less words (empty locations).

Parity is programmed with the D₁₅ - 17 bits. See Table 4 for a summary of the various parity programming options. Data present on D₁₅ - 17 during a program write will determine whether the FIFO will generate or check even/odd parity for the data present on D₀ - 7 and D₉ - 16 thereafter. If the user elects not to program the FIFO, the parity function is disabled. Flag operation and parity are described in greater detail in subsequent sections.

Flag Operation

The CY7C45X provides three status pins when not cascaded. The three pins, E/F, PAFE, and HF, allow decoding of six FIFO states (Table 1). PAFE is not available when the CY7C45X is cascaded for depth expansion. All flags are synchronous, meaning that the change of states is relative to one of the clocks (CKR or CKW, as appropriate).^[46] The Empty and Almost Empty flag states are exclusively updated by each rising edge of the read clock (CKR). For example, when the FIFO contains 1 word, the next read (rising edge of CKR while ENR=LOW) causes the flag pins to output a state that represents Empty. The Half Full, Almost Full, and Full flag states are updated exclusively by the write clock

Table 1. Flag Truth Table^[47]

E/F	PAFE	HF	State	7C455 Words in FIFO	7C456 Words in FIFO	7C457 Words in FIFO
0	0	1	Empty	0	0	0
1	0	1	Almost Empty	1 ♦ P	1 ♦ P	1 ♦ P
1	1	1	Less than or Equal to Half Full	P + 1 ♦ 256	P + 1 ♦ 512	P + 1 ♦ 1024
1	1	0	Greater than Half Full	257 ♦ 511 - P	513 ♦ 1023 - P	1025 ♦ 2047 - P
1	0	0	Almost Full	512 - P ♦ 511	1024 - P ♦ 1023	2048 - P ♦ 2047
0	0	0	Full	512	1024	2048

Notes:

45. CKW will write D₀ - 9 into the programming register. CKR will read D₀ - 9 during a programming register read.
46. The synchronous architecture guarantees the flags valid for approximately one cycle of the clock they are synchronized to.
47. P is the decimal value of the binary number represented by D₀ - 7 for the CY7C455, D₀ - 8 for the CY7C456, and D₀ - 9 for the CY7C457. P = 0 signifies that the Almost Empty state = Empty state.



Flag Operation (continued)

(CKW). For example, if the CY7C457 contains 2,047 words (2,048 words indicate Full for the CY7C457), the next write (rising edge of CKW while ENW=LOW) causes the flag pins to output a state that is decoded as Full.

Since the flags denoting emptiness (Empty, Almost Empty) are only updated by CKR and the flags signifying fullness (Half Full, Almost Full, Full) are exclusively updated by CKW, careful attention must be given to the flag operation. The user must be aware that if a boundary (Empty, Almost Empty, Half Full, Almost Full, or Full) is crossed due to an operation from a clock that the flag is not synchronized to (i.e., CKW does not affect Empty or Almost Empty), a flag update cycle is necessary to represent the FIFO's new state. The signal to which a flag is not synchronized will be referred to as the opposite clock (CKW is opposite clock for Empty and Almost Empty flags; CKR is the opposite clock for Half Full, Almost Full, and Full flags). Until a proper flag update cycle is executed, the synchronous flags will not show the new state of the FIFO.

When updating flags, the FIFO must make a decision as to whether or not the opposite clock was recognized when a clock updates the flag. For example (when updating the Empty flag), if a write occurs at least t_{SKEW1} after a read, the write is guaranteed not to be included when CKR updates the flag. If a write occurs at least t_{SKEW2} before a read, the write is guaranteed to be included when CKR updates flag. If a write occurs within t_{SKEW1} after or t_{SKEW2} before CKR, then the decision of whether or not to include the write when the flag is updated by CKR is arbitrary.

The update cycle for non-boundary flags (Almost Empty, Half Full, Almost Full) is different from that used to update the boundary flags (Empty, Full). Both operations are described below.

Boundary and Non-Boundary Flags

Boundary Flags (Empty)

The Empty flag is synchronized to the CKR signal (i.e., the Empty flag can only be updated by a clock pulse on the CKR pin). An empty FIFO that is written to will be described with an Empty flag state until a rising edge is presented to the CKR pin. When making the transition from Empty to Almost Empty (or Empty to Less than or Equal to Half Full), a clock cycle on CKR is necessary to update the flags to the current state. In such a state (flags showing Empty even though data has been written to the FIFO), two read clock cycles are required to read data out of the FIFO. The first read serves only to update the flags to the Almost Empty or Less than or Equal to Half Full state, while the second read outputs the data. This first read cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in FIFO). It simply deasserts the Empty flag. The flag is updated regardless of the ENR state. Therefore, the update occurs even when ENR is deasserted (HIGH), so that a valid read is not necessary to update the flags to correctly describe the FIFO. In this example, the write must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the write will be included in the count when CKR updates the flags. When a free-running clock is connected to CKR, the flag is updated each cycle. Table 2 shows an example of a sequence of operations that update the Empty flag.

Boundary Flags (Full)

The Full flag is synchronized to the CKW signal (i.e., the Full flag can only be updated by a clock pulse on the CKW pin). A full FIFO that is read will be described with a Full flag until a rising edge is presented to the CKW pin. When making the transition from Full

to Almost Full (or Full to Greater Than Half Full), a clock cycle on CKW is necessary to update the flags to the current state. In such a state (flags showing Full even though data has been read from the FIFO), two write cycles are required to write data into the FIFO. The first write serves only to update the flags to the Almost Full or Greater Than Half Full state, while the second write inputs the data. This first write cycle is known as the latent or flag update cycle because it does not affect the data in the FIFO or the count (number of words in the FIFO). It simply deasserts the Full flag. The flag is updated regardless of the ENW state. Therefore, the update occurs even when ENW is deasserted (HIGH), so that a valid write is not necessary to update the flags to correctly describe the FIFO. In this example, the read must occur at least t_{SKEW2} before the flag update cycle in order for the FIFO to guarantee that the read will be included in the count when CKW updates the flags. When a free-running clock is connected to CKW, the flag updates each cycle. Full flag operation is similar to the Empty flag operation described in Table 2.

Non-Boundary Flags (Almost Empty, Half Full, Almost Full)

The CY7C45X features programmable Almost Empty and Almost Full flags. Each flag can be programmed a specific distance from the corresponding boundary flags (Empty or Full). The flags can be programmed to be activated at the Empty or Full boundary, or at any distance from the Empty/Full boundary. When the FIFO contains the number of words or fewer for which the flags have been programmed, the PAFE flag will be asserted signifying that the FIFO is Almost Empty. When the FIFO is within that same number of empty locations from being Full, the PAFE will also be asserted signifying that the FIFO is Almost Full. The HF flag is decoded to distinguish the states.

The default distance from where PAFE becomes active to the boundary (Empty, Full) is 16 words/locations. The Almost Full and Almost Empty flags can be programmed so that they are only active at Full and Empty boundaries. However, the operation will remain consistent with the non-boundary flag operation that is discussed below.

Almost Empty is only updated by CKR while Half Full and Almost Full are updated by CKW. Non-boundary flags employ flag update cycles similar to the boundary flag latent cycles in order to update the FIFO status. For example, if the FIFO just reaches the Greater than Half Full state, and then two words are read from the FIFO, a write clock (CKW) will be required to update the flags to the Less than Half Full state. However, unlike the boundary flag latent cycle, the state of the enable pin (ENW in this case) affects the operation. Therefore, set-up and hold times for the enable pins must be met (t_{SEN} and t_{HEN}). If the enable pin is active during the flag update cycle, the count and data are updated in addition to PAFE and HF. If the enable pin is not asserted during the flag update cycle, only the flags are updated. Tables 3 show an example of a sequence of operations that update the Almost Empty and Almost Full flags.

The CY7C45X also features even or odd parity checking and generation. D₁₅ - D₁₇ are used during a program write to describe the parity option desired. Table 4 summarizes programmable parity options. If the user elects not to program the device, then parity is disabled. Parity information is provided on two multi-mode output pins (Q₉/PG1/PE1 and Q₁₇/PG2/PE2). The three possible modes are described in the following paragraphs.



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Table 2. Empty Flag (Boundary Flag) Operation Example

Status Before Operation					Operation	Status After Operation					Comments
Current State of FIFO	E/F	AFE	HF	Number of Words in FIFO		Next State of FIFO	E/F	AFE	HF	Number of words in FIFO	
Empty	0	0	1	0	Write (ENW = 0)	Empty	0	0	1	1	Write
Empty	0	0	1	1	Write (ENW = 0)	Empty	0	0	1	2	Write
Empty	0	0	1	2	Read (ENR = X)	AE	1	0	1	2	Flag Update
AE	1	0	1	2	Read (ENR = 0)	AE	1	0	1	1	Read
AE	1	0	1	1	Read (ENR = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)
Empty	0	0	1	0	Write (ENR = 0)	Empty	0	0	1	1	Write
Empty	1	0	1	1	Read (ENR = X)	AE	1	0	1	1	Flag Update
AE	1	0	1	1	Read (ENR = 0)	Empty	0	0	1	0	Read (transition from Almost Empty to Empty)

Programmable Parity

Parity Disabled (Q₈/Q₁₇ mode)

When parity is disabled (or the user does not program parity option) the FIFO stores all 18 bits present on D₀ - 17 inputs internally and will output all 18 bits on Q₀ - 17.

Parity Generate (PG mode)

This mode is used to generate either even or odd parity (as programmed) from D₀ - 7 and D₉ - 16. D₈ and D₁₇ inputs are ignored. The parity bits are stored internally as D₈ and D₁₇, and during a subsequent read will be available on the PG1 and PG2 pins along with the data words from which the parity was generated (Q₀ - 7 and Q₉ - 16). For example, if parity generate is set to ODD and the D₀ - 7 inputs have an EVEN number of 1s, PG1 will be HIGH.

Parity Check (PE mode)

If the FIFO is programmed for parity checking, it will compare the parity of D₀ - 8 and D₉ - 17 with the program register. For example, D₈ and D₁₇ will be set according to the result of the parity check on each word. When these words are later read, PE₁ and PE₂ will reflect the result of the parity check. If a parity error occurs in D₀ - 8, D₈ will be set LOW internally. When this word is later read, PE₁ will be LOW.

Width Expansion Modes

During width expansion all flags (programmable and nonprogrammable) are available. These FIFOs can be expanded in width to provide word width greater than 18 in increments of 18. During width expansion mode all control line inputs are common. When the FIFO is being read near the Empty (Full) boundary, it is important to note that both sets of flags should be checked to see if they have been updated to the Not Empty (Not Full) condition to insure that the next read (write) will perform the same operation on all devices.

Checking all sets of flags is critical so that data is not read from the FIFOs "staggered" by one clock cycle. This situation could occur when the first write to an empty FIFO and a read are very close together. If the read occurs less than t_{SKW2} after the first write to two width-expanded devices, A and B, device A may go Almost

Empty (read recognized as flag update) while device B stays Empty (read ignored). This occurs because a read can be either recognized or ignored if it occurs within t_{SKW2} of a write. The next read cycle outputs the first half of the first word on device A while device B updates its flags to Almost Empty. Subsequent reads will continue to output "staggered" data assuming more data has been written to FIFOs.

Depth Expansion Mode

The CY7C45X can operate up to 50 MHz when cascaded. Depth expansion is accomplished by connecting expansion out (XO) of the first device to expansion in (XI) of the next device, with XO of the last device connected to XI of the first device. The first device has its first load pin (FL) tied to V_{SS} while all other devices must have this pin tied to V_{CC}. The first device will be the first to be write and read enabled after a master reset.

Proper operation also requires that all cascaded devices have common CKW, CKR, ENW, ENR, D₀ - 17, Q₀ - 17, and MR pins. When cascaded, one device at a time will be read enabled so as to avoid bus contention. By asserting XO when appropriate, the currently enabled FIFO alerts the next FIFO that it should be enabled. The next rising edge on CKR puts Q₀ - 17 outputs of the first device into a high-impedance state. This occurs regardless of the state of ENR or the next FIFO's Empty flag. Therefore, if the next FIFO is empty or undergoing a latent cycle, the Q₀ - 17 bus will be in a high-impedance state until the next device receives its first read, which brings its data to the Q₀ - 17 bus.

Program Write/Read of Cascaded Devices

Programming of cascaded FIFOs is the same as for a single device. Because the controls of the FIFOs are in parallel when cascaded, they all get programmed the same. During program mode, only parity is programmed since Almost Full and Almost Empty flags are not available when CY7C45X is cascaded. Only the "first device" (FIFO with FL=LOW) will output its program register contents on Q₀ - 17 during a program read. Q₀ - 17 of all other devices will remain in a high-impedance state to avoid bus contention.



PRELIMINARY

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C455-14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455-14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455-14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455-14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C455-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455-20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455-20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C455-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C455-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C455-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C455-30LMB	L69	52-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C456-14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456-14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456-14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456-14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C456-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456-20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456-20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C456-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C456-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C456-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C456-30LMB	L69	52-Square Leadless Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
14	CY7C457-14JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457-14NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457-14LC	L69	52-Square Leadless Chip Carrier	
	CY7C457-14JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457-14LMB	L69	52-Square Leadless Chip Carrier	Military
20	CY7C457-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457-20NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457-20LMB	L69	52-Square Leadless Chip Carrier	Military
30	CY7C457-30JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C457-30NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C457-30JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C457-30LMB	L69	52-Square Leadless Chip Carrier	Military



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{CC}	1, 2, 3
I _{OS}	1, 2, 3
I _{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t _{CKW}	9, 10, 11
t _{CKR}	9, 10, 11
t _{CKH}	9, 10, 11
t _{CKL}	9, 10, 11
t _A	9, 10, 11
t _{OH}	9, 10, 11
t _{FH}	9, 10, 11
t _{SD}	9, 10, 11
t _{HD}	9, 10, 11
t _{SEN}	9, 10, 11
t _{HEN}	9, 10, 11
t _{OE}	9, 10, 11
t _{PG}	9, 10, 11
t _{PE}	9, 10, 11
t _{FD}	9, 10, 11
t _{SKEW1}	9, 10, 11
t _{SKEW2}	9, 10, 11
t _{PMR}	9, 10, 11
t _{SCMR}	9, 10, 11
t _{OHMR}	9, 10, 11
t _{MRR}	9, 10, 11
t _{MRF}	9, 10, 11
t _{AMR}	9, 10, 11
t _{SMRP}	9, 10, 11
t _{HMRP}	9, 10, 11
t _{FTP}	9, 10, 11
t _{AP}	9, 10, 11
t _{OHP}	9, 10, 11

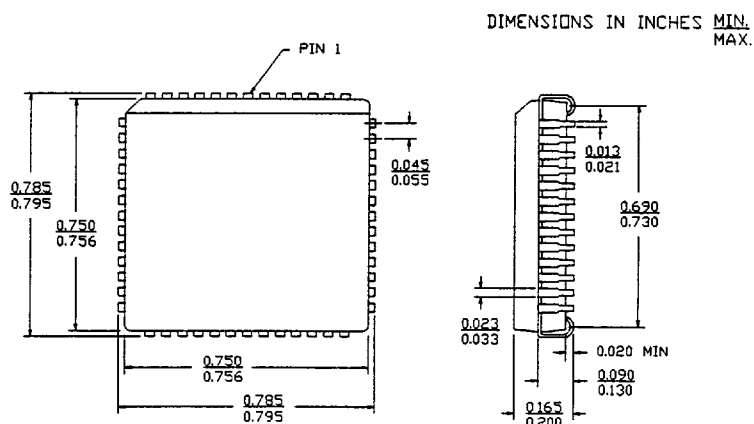
Document #: 38-00211-B



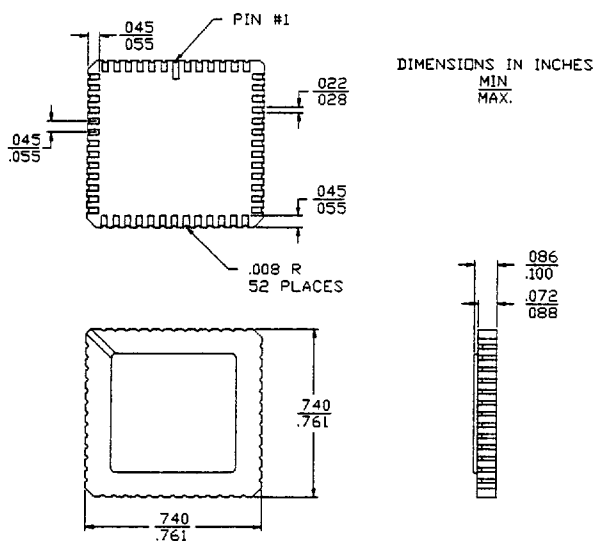
PRELIMINARY

Package Diagrams

52-Lead Plastic Leaded Chip Carrier J69



52-Square Leadless Chip Carrier L69



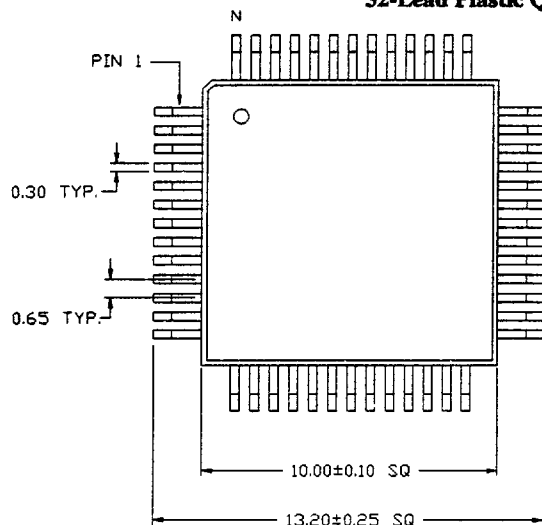


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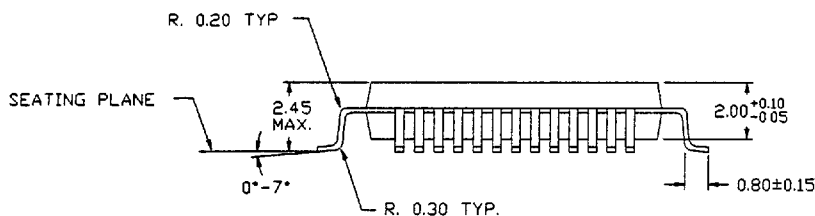
CY7C455
CY7C456
CY7C457

Package Diagrams (continued)

52-Lead Plastic Quad Flatpack N52



DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



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