SANYO No.2723A

LC9100, 92000 Series

CMOS LSI

Gate Array

Overview

The LC9100, 92000 series are semicustom LSIs especially suited to develop the user-requested LSI in a short period of time and at a low cost. The LC9100, 92000 series provide 17 types of master chip having 400 gates to 10,000 gates. The LC9100, 92000 series contain not only logic cells such as gate, flip-flop and input/output cells such as input/output buffer in a large number but also approximately 220 types of macro cells for the TTL74 series, CMOS4000, 4500 series. Therefore, standard logic IC-applied circuits can be input, almost as they are, as our format.

Features of <LC9100, 92000> Series

· Many function cells

Logic cell	Approximately 130 types	Gate, flip-flop, etc.
Input/output cell	Approximately 30 types	TTL/CMOS compatible, capable of containing RC OSC amp, comparator, monostable multivibrator, high-current buffer, LCD driver
Macro cell	Approximately 220 types	For the TTL74 series, CMOS4000, 4500 series

LC9100 Series Lineup

○:Available, *:Under development, ★:In planning

LC9100 Series										
Item	Type No.		LC 9111A	LC 9116A	LC 9123A	LC 9130A	LC 9140A	LC 9153A	LC 9103B	LC 9105B	LC 9108B
Number of basic cells (Gates)			1190	1692	2394	3013	4082	5365	340	588	858
Number of basic I/O cells			70	84	96	112	128	152	32	44	52
Package	DIP	16	–	–	–	–	–	–	○	○	–
		18	–	–	–	–	–	–	○	○	–
		20	–	–	–	–	–	–	○	○	–
		24	○	*	*	*	*	*	○	○	○
		28	○	○	○	○	○	*	○	○	○
		40	○	○	○	○	○	*	–	○	○
		42	○	○	○	○	*	*	–	*	○
	Shrink DIP	30	○	○	–	–	–	–	○	○	○
		42	○	○	○	○	*	*	–	○	○
		64	–	–	○	○	○	○	–	–	–
	QIP	48	○	○	○	*	○	*	○	○	○
		64	○	○	○	○	○	○	–	–	○
		80	–	○	○	○	○	○	–	–	–
		100	–	–	○	○	○	○	–	–	–
		128	–	–	–	–	○	○	–	–	–
		160	–	–	–	–	★	○	–	–	–
	MFP	20	–	–	–	–	–	–	○	–	–
		24	*	*	*	*	–	–	○	*	*
		28	○	○	○	–	–	–	○	○	○
	PLCC	68	–	○	○	○	○	*	–	–	–
Internal gate delay time			1.7ns (2-input NAND F/O=2, L=2mm type								
Power supply			3 to 5.5V								
I/O level			TTL/CMOS compatible								

Specifications and information herein are subject to change without notice.

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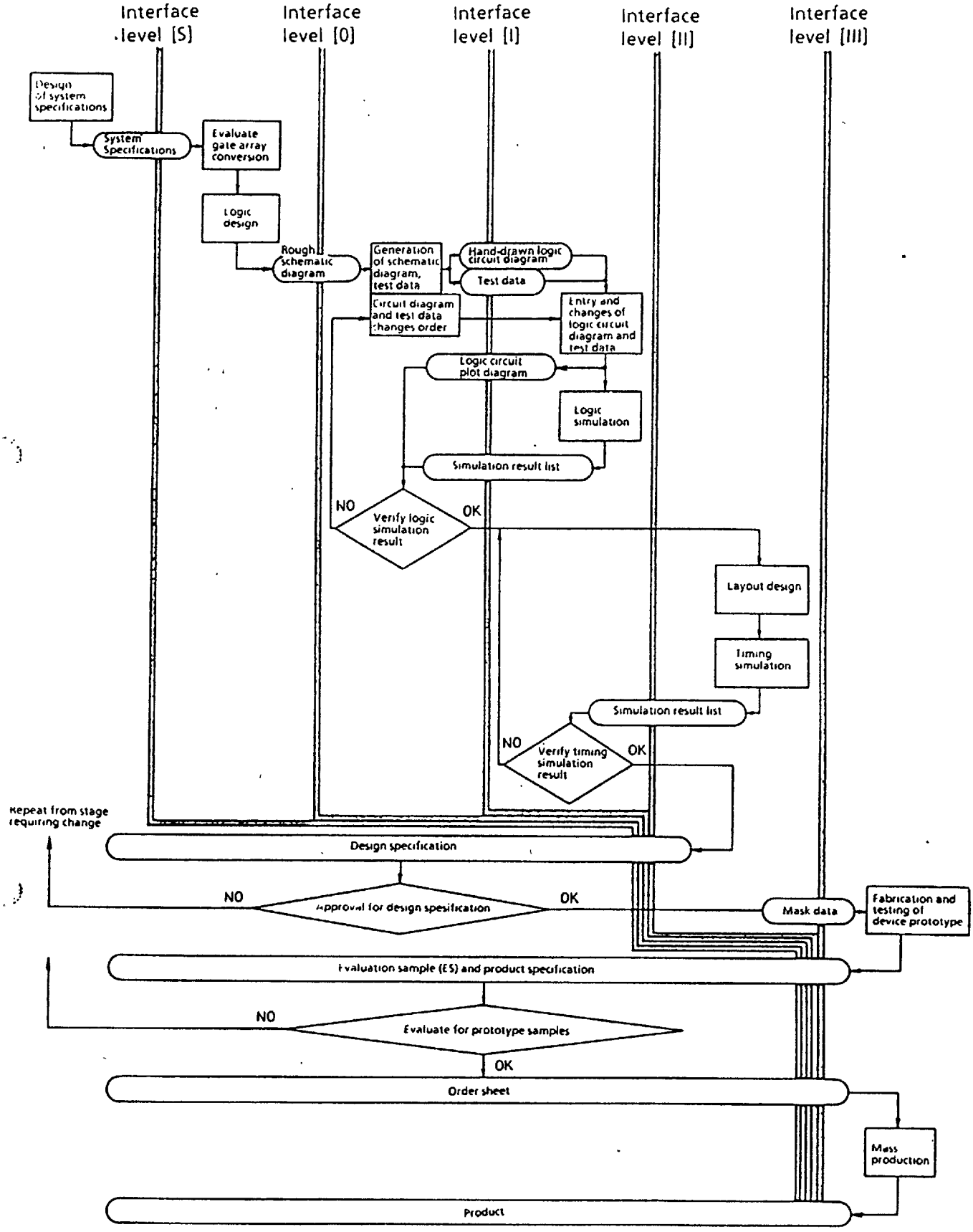
LC92000 Series Lineup

○:Available, *:Under development, ★:In planning

LC92000 Series									
Item		Type No.	LC 92032A	LC 92041A	LC 92060A	LC 92080A	LC 92100A	LC 92007B	LC 92011B	LC 92018B
Number of basic cells (Gates)			3216	4185	6016	8028	10023	708	1110	1881
Number of basic I/O cells			96	108	130	152	176	62	82	108
Package	DIP	24	*	*	*	*	*	○	*	*
		28	○	○	○	*	*	○	○	○
		40	○	○	○	*	*	○	○	○
		42	○	○	*	*	*	○	○	○
	Shrink DIP	30	–	–	–	–	–	○	○	–
		42	○	○	*	*	*	○	○	○
		64	○	○	○	○	*	–	–	○
	QIP	48	○	*	○	*	–	○	○	○
		64	○	○	○	○	–	○	○	○
		80	○	○	○	○	○	–	○	○
		100	○	○	○	○	○	–	–	○
		128	–	–	○	○	*	–	–	–
		160	–	–	★	○	○	–	–	–
	MFP	24	*	*	–	–	–	*	*	*
		28	○	–	–	–	–	○	○	○
	PLCC	68	○	○	○	*	*	–	○	○
Internal gate delay time			1.2ns (2-input NAND F/O=2, L=2mm type							
Power supply			3 to 5.5V							
I/O level			TTL/CMOS compatible							

Development Procedure and User Interface



In accordance with customer requirements, gate arrays can be developed from circuit data in any format. The above flowchart shows five levels of customer interface. The right of each interface shown as the vertical double lines are Sanyo's job and the left is user's job. Blocks shown with rounded ends ⬭ indicate materials to be provided by the customer or Sanyo. Blocks shown with squared ends ▭ indicates jobs to be done.

Pre-defined Macrocells

The following table shows the pre-defined macrocells for TTL74 series and 4000 and 4500 CMOS series logic devices.

Macros for the TTL74 Series								Macros for the CMOS 4000, 4500 Series			
Macro cell name	No. of cells	Macro cell name	No. of cells	Macro cell name	No. of cells	Macro cell name	No. of cells	Macro cell name	No. of cells	Macro cell name	No. of cells
1/4 LS00	1	LS93	31	1/4 LS175	7	1/2 LS390	34	1/4 C4001	1	C4099	86
1/4 LS02	1	N94	41	N176	52	1/2 LS393	30	1/2 C4002	2	C40101	28
1/6 LS04	1	LS95	31	N177	47	LS396	49	C4006	96	C40102	173
1/4 LS08	2	LS96	57	N178	37	LS398	37	C4008	47	C40103	165
1/3 LS10	2	N97	99	N179	43	LS399	29	1/4 C4011	1	C40147	45
1/3 LS11	2	1/2 N100	12	N180	26			1/2 C4012	2	C40160	65
1/2 LS20	2	1/2 LS107	11	LS181	83			1/2 C4013	8	C40161	60
1/2 LS21	3	1/2 LS109	12	N182	21			C4014	57	C40162	62
1/2 N25	3	1/2 LS112	12	1/2 LS183	12			1/2 C4015	25	C40163	57
1/3 LS27	2	1/2 LS113	11	N184	96			C4017	50	C40174	37
1/4 LS28	1	1/2 LS114	12	N185	80			C4018	58	C40175	29
LS30	6	1/2 N116	22	LS190	81			C4019	12	C40181	83
1/4 LS32	2	1/2 N120	15	LS191	78			C4020	98	C40182	21
1/4 LS37	1	1/4 LS125	3	LS192	78			C4021	73	C40192	77
1/2 LS40	2	1/4 LS126	2	LS193	68			C4022	41	C40193	66
LS42	24	LS133	11	LS194	43			1/3 C4023	2	C40194	51
N43	24	1/4 S135	6	LS195	40			C4024	51	C4510	92
N44	24	LS137	31	LS196	52			1/3 C4025	2	C4514	45
1/2 LS51Y	3	LS138	23	LS197	47			1/2 C4027	11	C4515	44
1/2 LS51Z	2	1/2 LS139	8	N198	79			C4028	21	C4516	82
N54	4	LS147	27	N199	73			C4029	100	1/2 C4518	39
LS54	6	LS148	29	LS259	71			1/4 C4030	3	C4519	28
LS55	4	N150	56	1/2 LS260	5			C4032	61	1/2 C4520	37
S64	8	LS151	27	LS261	51			C4035	51	C4522	78
1/2 LS68Y	34	LS152	22	1/8 LS273	6			C4038	61	C4526	74
1/2 LS68Z	34	LS153	16	N278	27			C4040	86	C4527	61
1/2 LS69Y	31	LS154	34	1/4 LS279Y	2			C4042	19	1/2 C4530	14
1/2 LS69Z	30	LS155	17	1/4 LS279Z	3			C4063	43	C4531	36
N70	17	LS157	15	LS280	42			C4068	6	C4532	29
1/2 LS73	11	LS158	11	LS283	47			1/6 C4069	1	C4549	167
1/2 LS74	10	LS160	65	LS290	41			1/4 C4070	3	C4554	44
1/4 LS75	4	LS161	60	LS293	31			1/4 C4071	2	1/2 C4555	10
1/2 LS76	14	LS162	62	LS298	30			1/2 C4072	3	1/2 C4556	11
1/4 LS77	3	LS163	57	LS352	18			1/3 C4073	2	C4559	165
1/2 LS78	14	LS164	51	1/4 LS375	4			1/3 C4075	2	C4560	54
N82	23	LS165	76	1/8 LS377	7			1/4 C4077	3	C4561	20
LS83	47	LS166	68	1/6 LS378	7			C4078	6	C4581	83
LS85	41	N167	66	1/4 LS379	8			1/4 C4081	2	C4582	21
1/4 LS86	3	LS168	76	LS381	117			1/2 C4082	3	C4585	31
LS90	41	LS169	72	LS382	110			1/2 C4085	3		
LS91	43	1/4 LS171	7	1/4 LS385	30			C4095	17		
LS92	33	1/6 LS174	6	1/4 LS386	3			C4096	19		

*1 Those macro names that contain a fraction, such as 1/2 or 1/4, are those in which a number of identical function circuits are incorporated in the standard logic IC. For example, the 74LS00 is an IC that incorporates four, 2-input NAND gates. In Sanyo's nomenclature, however, a macro with a single, 2-input NAND gate is defined with the macro name LS00 and designated as 1/4LS00.

Names that are identical except for a final Y or Z indicate devices that incorporate a number of independent circuits of differing functions in the corresponding standard logic device. Sanyo defines these circuits separately as macros.

<LC9100> Series

Absolute Maximum Ratings at $V_{SS}=0V$, Ta = 25°C

Parameter	Symbol	Ratings	unit
Maximum Supply Voltage	V_{DD} max	−0.3 to +7.0	V
Input/Output Voltage	V_I, V_O	−0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	−30 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C

Allowable Operating Conditions at Ta = −30 to +70°C, $V_{SS}=0V$

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage Range	V_{IH}	0		V_{DD}	V

DC Characteristics

Input/Output Level at $V_{SS}=0V$, $V_{DD}=4.5$ to 5.5V, Ta = −30 to +70°C (B Series only)

Item	Symbol	Condition	min	typ	max	Condition	min	typ	max	Condition	min	typ	max	unit
'H'-Level Input Voltage	V_{IH}	TTL compatible	2.2			TTL compatible	2.2			TTL compatible	2.2			V
		CMOS compatible	0.7 V_{DD}			CMOS compatible	0.7 V_{DD}			CMOS compatible	0.7 V_{DD}			V
'L'-Level Input Voltage	V_{IL}	TTL compatible			0.8	TTL compatible			0.8	TTL compatible			0.8	V
		CMOS compatible			0.3 V_{DD}	CMOS compatible			0.3 V_{DD}	CMOS compatible			0.3 V_{DD}	V
'H'-Level Output Voltage	V_{OH}	I_{OH} = −3mA	2.4			I_{OH} = −8mA	2.4			I_{OH} = −12mA	2.4			V
		I_{OH} = −1μA	V_{DD} −0.05			I_{OH} = −4μA	V_{DD} −0.05			I_{OH} = −6μA	V_{DD} −0.05			V
'L'-Level Output Voltage	V_{OL}	I_{OL} = 3mA			0.4	I_{OL} = 8mA			0.4	I_{OL} = 12mA			0.4	V
		I_{OL} = 1μA			V_{DD} +0.05	I_{OL} = 4μA			V_{DD} +0.05	I_{OL} = 6μA			V_{DD} +0.05	V
Input Leakage Current	I_L	$V_I=V_{SS}$, V_{DD}	−1		+1	$V_I=V_{SS}$, V_{DD}	−1		+1	$V_I=V_{SS}$, V_{DD}	−1		+1	μA

Note : The buffer with a large-current output is also available.

<LC92000> Series

Absolute Maximum Ratings at $V_{SS}=0V$, $Ta=25°C$

Parameter	Symbol	Ratings	unit
Maximum Supply Voltage	V_{DD} max	−0.3 to +7.0	V
Input/Output Voltage	V_I, V_O	−0.3 to V_{DD}+0.3	V
Operating Temperature	Topg	−30 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C

Allowable Operating Conditions at $Ta=-30$ to $+70°C$, $V_{SS}=0V$

Parameter	Symbol	min	typ	max	unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage Range	V_{IH}	0		V_{DD}	V

DC Characteristics

Input/Output Level at $V_{SS}=0V$, $V_{DD}=4.5$ to $5.5V$, $Ta=-30$ to $+70°C$ (B Series only)

Item	Symbol	Condition	min	typ	max	Condition	min	typ	max	Condition	min	typ	max	unit
'H'-Level Input Voltage	V_{IH}	TTL compatible	2.2			TTL compatible	2.2			TTL compatible	2.2			V
		CMOS compatible	0.7 V_{DD}			CMOS compatible	0.7 V_{DD}			CMOS compatible	0.7 V_{DD}			V
'L'-Level Input Voltage	V_{IL}	TTL compatible			0.8	TTL compatible			0.8	TTL compatible			0.8	V
		CMOS compatible			0.3 V_{DD}	CMOS compatible			0.3 V_{DD}	CMOS compatible			0.3 V_{DD}	V
'H'-Level Output Voltage	V_{OH}	$I_{OH}=-3mA$	2.4			$I_{OH}=-6mA$	2.4			$I_{OH}=-12mA$	2.4			V
		$I_{OH}=-1\mu A$	$V_{DD}-0.05$			$I_{OH}=-2\mu A$	$V_{DD}-0.05$			$I_{OH}=-4\mu A$	$V_{DD}-0.05$			V
'L'-Level Output Voltage	V_{OL}	$I_{OL}=3mA$			0.4	$I_{OL}=6mA$			0.4	$I_{OL}=12mA$			0.4	V
		$I_{OL}=1\mu A$			$V_{DD}+0.05$	$I_{OL}=2\mu A$			$V_{DD}+0.05$	$I_{OL}=4\mu A$			$V_{DD}+0.05$	V
Input Leakage Current	I_L	$V_I=V_{SS}$, V_{DD}	−1		+1	$V_I=V_{SS}$, V_{DD}	−1		+1	$V_I=V_{SS}$, V_{DD}	−1		+1	μA

Note : The cell series with $I_{OL}=4mA$ is also available as standard. The buffer with a large-current output is also available.