



CYPRESS
SEMICONDUCTOR

CY7C9115
CY7C9116/CY7C9117

CMOS 16-Bit Microprogrammed ALU

Features

- **Fast**
 - 35-ns worst-case propagation delay, I to Y
- **Low power CMOS**
 - I_{CC} (max. at 10 MHz) = 145 mA (commercial)
 - I_{CC} (max. static) = 68 mA (commercial)
- **V_{CC} margin 5V $\pm$ 10%**
 - All parameters guaranteed over commercial and military operating temperature range
- **Instruction set and architecture optimized for high-speed controller applications**

- **CY7C9117 separate I/O**
 - One and two operand arithmetic and logical operations
 - Bit manipulation, field insertion/extraction instructions
 - Eleven types of instructions
- **Immediate instruction capability**
- **16-bit barrel shifter capability**
- **32-word x 16-bit register file**
- **8-bit status register**
 - Four ALU status bits
 - Link bit and three user-definable status bits
- **Capable of withstanding greater than 2001V static discharge voltage**

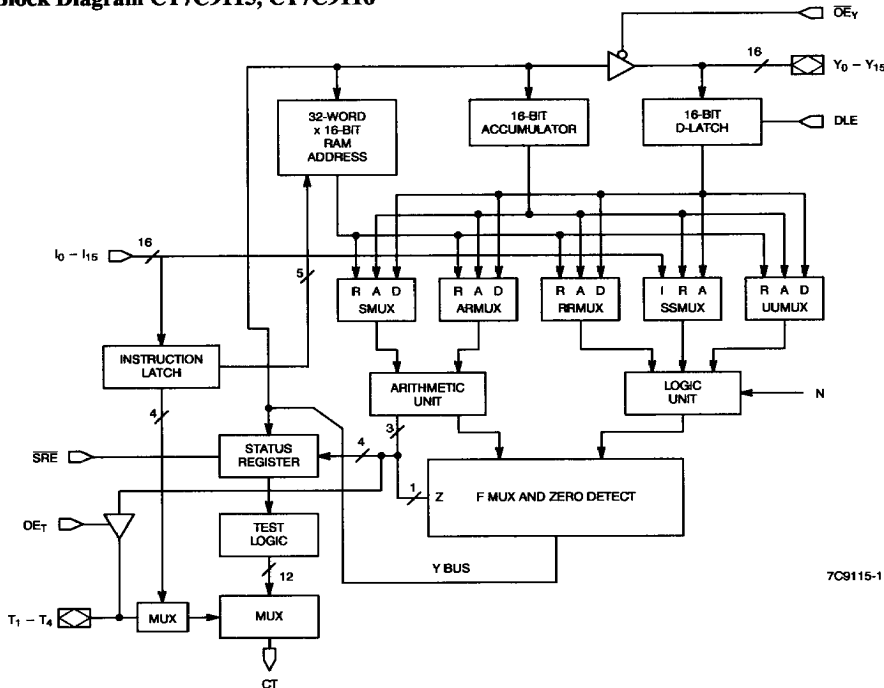
- **Pin compatible and functionally equivalent to 29116, 29116A, 29C116, 29117, 29117A, 29C117**

Functional Description

The CY7C9115, CY7C9116, and CY7C9117 are high-speed 16-bit microprogrammed Arithmetic and Logic Units (ALUs).

The architecture and instruction set of the devices are optimized for peripheral controller applications such as disk controllers, graphics controllers, communications controllers, and modems. When used with the CY7C517 multiplier, the CY7C9115, CY7C9116, and CY7C9117 also support microprogrammed processor applications.

Logic Block Diagram CY7C9115, CY7C9116



7C9115-1

Functional Description (continued)

The CY7C9115, CY7C9116, and CY7C9117 (shown in the block diagrams) consist of a 32-word by 16-bit single-port RAM register file, a 16-bit arithmetic unit and logic unit, an instruction latch and decoder, a data latch, an accumulator register, a 16-bit barrel shifter, a priority encoder, a status register, a condition code generator and multiplexer, and three-state output buffers.

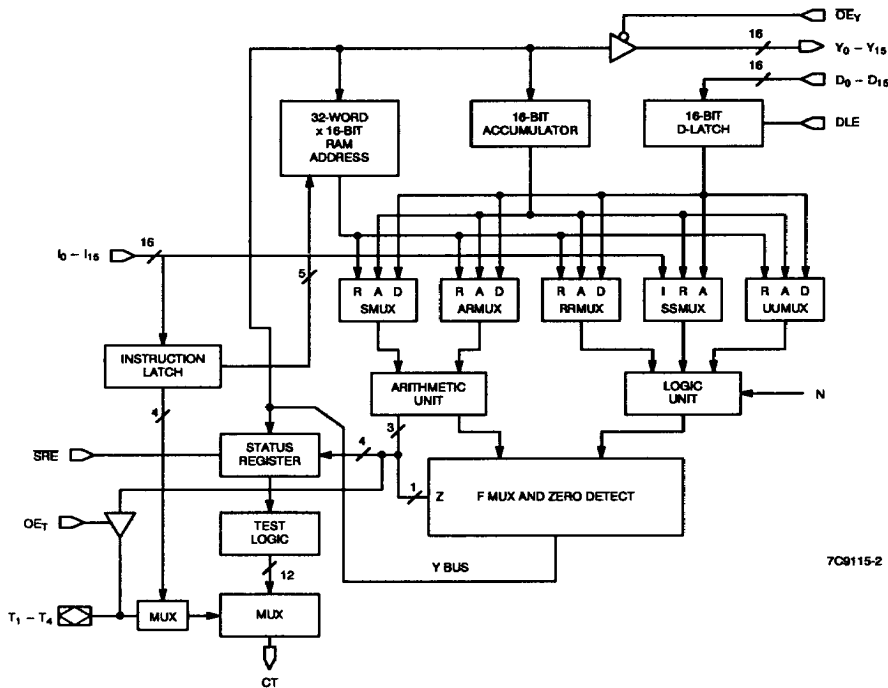
The instruction set of the CY7C9115, CY7C9116, and CY7C9117 can be divided into eleven instruction types: single-operand, two-operand, single-bit shifts, rotate and merge, rotate and compare, rotate by n-bits, bit-oriented instructions, priori-

tize, Cyclic Redundancy Check (CRC), status, and NO-OP. Instruction execution occurs in a single clock cycle except for Immediate Instructions, which require two clock cycles to execute.

The CY7C9116 and CY7C9117 are pin-compatible, functional equivalents of the industry-standard 29116, 29116A, 29C116, 29117, 29117A, and 29C117 with improved performance.

Fabricated in an advanced 1.2-micron, two-level metal CMOS process, the CY7C9115, CY7C9116, and CY7C9117 eliminate latch-up, have ESD protection greater than 2001V, and achieve superior performance with low power dissipation.

Logic Block Diagram CY7C9117

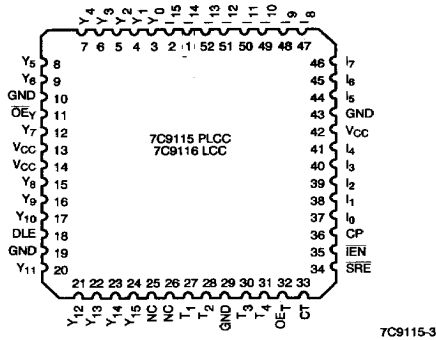


Selection Guide

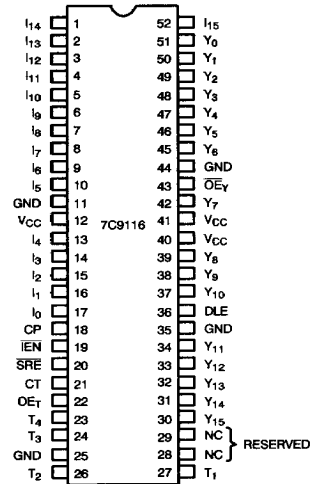
		7C9115-35 7C9116-35 7C9117-35	7C9115-40, 45 7C9116-40, 45 7C9117-40, 45	7C9115-65 7C9116-65 7C9117-65	7C9115-79 7C9116-79 7C9117-79
Worst-Case I - Y Propagation Delay (ns)	Commercial	35	45	65	
	Military		40	65	79
Maximum Operating Current @ 10 MHz (mA)	Commercial	145	145	145	
	Military		166	166	166

Pin Configurations

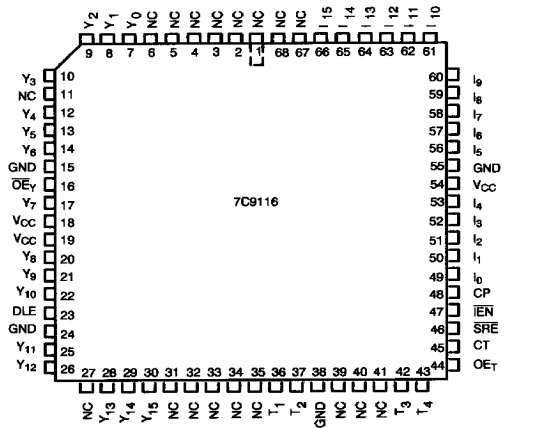
PLCC, LCC
Top View



DIP
Top View

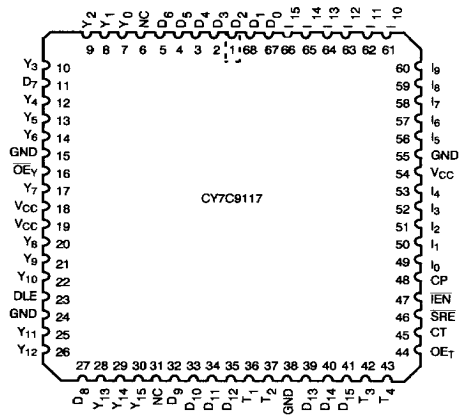


PLCC
Top View



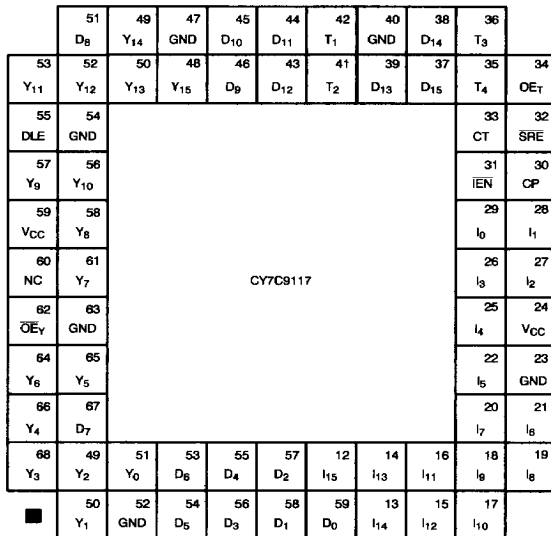
Pin Configurations (continued)

LCC/PLCC
Top View



7C9115-7

68 PGA
Top View



7C9115-6

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential	- 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 3.0V to +7.0V
Output Current into Outputs (LOW)	30 mA

Description of Architecture

The CY7C9115, CY7C9116, and CY7C9117 are 16-bit micro-programmed arithmetic and logic units comprised of the following sections (see block diagram):

- 32-Word x 16-Bit Register File
- Data Latch
- Instruction Latch and Decoder
- Accumulator
- Logic Unit with a 16-Bit Barrel Shift Capability
- Arithmetic Unit
- Priority Encoder
- Condition Code Generator and Multiplexer
- Status Register
- Output Buffers

32-Word x 16-Bit Register File

The 32-word x 16-bit register file is a single-port RAM with a 16-bit latch at the output. The latch is transparent while CP is HIGH and latched when CP is LOW. If IEN is LOW and the current instruction specifies the RAM at its destination, data is written into the RAM while CP is LOW. Word instructions write into all 16 bits of the RAM word addressed; byte instructions write into only the lower eight bits.

Use of an external multiplexer on five of the instruction inputs makes it possible to select separate read and write addresses for the same Non-immediate Instruction. Immediate Instructions do not allow this two-address operation for the 7C9115 and 7C9116. The 7C9117 does support two-address Immediate Instructions.

Data Latch

The data latch holds the 16-bit input to the CY7C9115, CY7C9116, and CY7C9117 from the Y (bidirectional) bus for the 7C9115 and 7C9116 and the data bus for the 7C9117. When DLE is HIGH, the latch is transparent, and it is latched when DLE is LOW.

Instruction Latch and Decoder

The 16-bit instruction latch is always transparent, except when Immediate Instructions are executed. The Instruction Decoder decodes the instruction inputs into the internal signals which control the CY7C9115, CY7C9116, and CY7C9117. All instructions other than Immediate Instructions execute in a single clock cycle.

Execution of Immediate Instructions takes two clock cycles. During the first clock cycle, the Instruction Decoder identifies the instruction as an Immediate Instruction and the Instruction Latch

Static Discharge Voltage >2001V
(Per MIL-STD-883 Method 3015)

Latch-Up Current (Outputs) >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Military ^[1]	- 55°C to +125°C	5V ±10%

Notes:

1. T_A is the "instant on" case temperature.

captures the instruction at the instruction inputs. For Immediate Instructions, the data at the instruction inputs during the second clock cycle is used as one of the operands for the Immediate Instruction specified during the first clock cycle. Upon completion of the Immediate Instruction (the end of the second clock cycle), the Instruction Latch again becomes transparent.

Accumulator

The accumulator is a 16-bit edge-triggered register. If the IEN is LOW and the current instruction specifies the accumulator as its destination, the accumulator accepts Y-input data at the clock LOW-to-HIGH transition. Word instructions write into all 16 bits of the accumulator, byte instructions write into the lower eight bits.

16-Bit Barrel Shifter

The barrel shifter can rotate data input to it from either the register file, the accumulator, or the data latch from 0 to 15 bit positions. In word mode, the barrel shifter rotates a 16-bit word; in byte mode, it only affects the lower eight bits. The barrel shifter is used as one of the ALU inputs.

Arithmetic and Logic Unit

The CY7C9115, CY7C9116, and the CY7C9117 have an arithmetic unit and a logic unit. The arithmetic unit is capable of operating on one or two operands while the logic unit is capable of operating on one, two, or three operands. The two units in parallel are able to execute the one and two operand instructions such as pass, complement, two's complement, add, subtract, AND, OR, EXOR, NAND, NOR, and EXNOR. Three operand instructions include rotate/merge and rotate/masked compare. There are three data types supported by the CY7C9115, CY7C9116, and CY7C9117; bit, byte, and 16-bit word.

All arithmetic and logic unit operations can be performed in either word or byte mode, with byte instructions performed only on the lower eight bits.

Three status outputs are generated by the arithmetic unit: carry (C), negative (N), and overflow (OVR). A zero flag (Z) detects a zero condition, though this flag is not generated by the arithmetic unit or the logic unit. These flags are generated in either word or byte mode, as appropriate.

The arithmetic unit uses full carry look-ahead across all 16 bits during arithmetic operations. The carry input to the arithmetic unit comes from the carry multiplexer, which can select either zero, one, or a stored carry bit (QC) from the status register. Multiprecision arithmetic uses QC as the carry input.

Description of Architecture (continued)

Priority Encoder

The priority encoder generates a binary-weighted code based on the location of the highest order ONE in its input word or byte. The operand to be prioritized may be ANDed with a mask to eliminate certain bits from the priority encoding. This masking is performed by the logic unit.

In word mode, the output is a binary one if bit 15 is the first (unmasked) HIGH encountered, a binary two if bit 14 is the first HIGH and so on. If bit 0 is the only HIGH, the output of the priority encoder is binary 16. If no bits are HIGH, a binary zero is output.

In byte mode, only bits 7 through 0 are examined. Bit 7 HIGH produces a binary one, bit 6 a binary two, and so on. If bit 0 is the only HIGH, a binary eight is output; if no bits are HIGH, a binary zero is output.

Condition Code Generator and Multiplexer

The twelve condition code test signals are generated in this section. The multiplexer selects one of these twelve and places it at the CT output. The multiplexer is addressed by either using the Test Instruction or by using the bidirectional T bus as an input. The test instruction specifies the test condition to be placed at the CT output, but it does not allow an ALU operation at the same time. Using the T bus as input, the CY7C9115, CY7C9116, and CY7C9117 may simultaneously test and execute an instruction. The test instruction lines ($I_4 - I_0$) take precedence over $T_4 - T_1$ for testing status.

Status Register

The 8-bit status word is held by the status register. The status register is updated at the end of all instructions except NO-OP, Save Status, and Test Status, provided the status register enable (SRE) and instruction enable (IEN) are both LOW. The status register is inhibited from changing if either SRE or IEN are HIGH.

The lower four status bits are the ALU status: OVR (overflow), N (negative), C (carry), and Z (zero). The upper four bits are a link bit and three user-defined status bits (Flag1, Flag2, Flag3).

As stated above, when IEN and SRE are LOW, the status register is updated at the end of all instructions other than NO-OP, Save Status, and Test Status. The lower four status bits are updated under the above conditions, with the additional exception of when IEN and SRE are LOW and the Status Set/Reset instruction is performed on the upper four bits. When IEN and SRE are LOW, the upper four status bits are only changed during their corresponding Status Set/Reset instructions and during Status Load instructions in word mode. The Link-Status bit is also updated after every shift instruction.

The status register can be loaded via the internal Y bus; it can also be selected as a source for the internal Y bus. Loading the status register in word mode updates all eight bits of the status register. In byte mode, only the lower four bits are updated.

Using the status register as a source in the word mode loads all eight bits into the lower byte of the destination; the upper byte is zero-filled. In byte mode, the status register loads the lower byte of the destination; however the upper byte is unchanged. Interrupt and subroutine processing is facilitated by this store/load combination, which allows saving and restoring the status register. The lower four bits of the status register can be read directly by outputting them to the $T_4 - T_1$ outputs. These outputs are enabled when OE_T is HIGH.

Output Buffers

Two sets of bidirectional buses exist on the CY7C9115 and CY7C9116. The bidirectional Y bus (16 bits) is controlled by OE_Y . The three state outputs are enabled when OE_Y is LOW, they are at high impedance when OE_Y is HIGH. This will allow data to be input to the data latch from the external world. The second bidirectional bus is the four-bit T bus. These three-state buffers are enabled by a HIGH on OE_T , which will output the internal ALU status bits (OVR, N, C, Z). If OE_T is LOW, the T outputs are at high impedance, and a test condition can be input on the T bus to determine the CT output.

The 7C9117 has separate Y bus output and Data Input buses. All other pins are functionally equivalent to the 7C9115 and 7C9116.

Pin Definitions

Signal Name	I/O	Description	Signal Name	I/O	Description
$Y_{15} - Y_0$	I/O	Data Input/Output. These bidirectional lines are used to directly load the 16-bit data latch when $\overline{OE}_Y$ is HIGH. When $\overline{OE}_Y$ is LOW, the arithmetic unit or the logic unit output data is output on $Y_{15} - Y_0$.	SRE	I	Status Register Enable. The Status Register is updated at the end of all instructions except NO-OP, Save Status, and Test Status when SRE and IEN are both LOW. The Status Register is inhibited from changing when either SRE or IEN are HIGH.
$I_{15} - I_0$	I	Instruction Word. This 16-bit word selects the function performed by the 7C911X. These lines are also used to input data when executing Immediate Instructions.	$\overline{OE}_Y$	I	Y Output Enable. This controls the 16-bit $Y_{15} - Y_0$ I/O port. When $\overline{OE}_Y$ is LOW, the Y outputs are enabled, when $\overline{OE}_Y$ is HIGH, the Y outputs are disabled (high impedance).
$T_4 - T_1$	I/O	Status Input/Output. These bidirectional pins are used to output the lower four status bits (OVR, N, C, and Z) when OE_T is HIGH. When OE_T is LOW, these lines are used as inputs to generate the conditional test (CT) output.	OE_T	I	T Output Enable. The four-bit T outputs are enabled when OE_T is HIGH; they are disabled (high impedance) when OE_T is LOW.
CT	O	Conditional Test. One of twelve condition code signals is selected by the condition code multiplexer to be placed on the CT output. CT = HIGH for a pass condition; CT = LOW for a fail condition.	CP	I	Clock Pulse. The RAM output latch is transparent when CP is HIGH; the RAM output is latched when CP goes LOW. If IEN is LOW and the current instruction specifies the RAM as the destination, then data is written into the RAM while CP is LOW. If IEN is LOW, the Accumulator and Status Register will accept data at the clock LOW to HIGH transition. The instruction latch becomes transparent upon exiting an Immediate Instruction during a LOW to HIGH clock transition.
DLE	I	Data Latch Enable. The 16-bit data latch is transparent when DLE is HIGH and latched when DLE is LOW.	$D_{15} - D_0$	I	These input lines are used to directly load the data latch.
IEN	I	Instruction Enable. The following occurs with IEN LOW: Data may be written into the RAM when the clock is LOW, the accumulator can accept data during the clock LOW to HIGH transition, and the Status Register can be updated when SRE is LOW. If IEN is HIGH, CT is disabled as a function of the instruction inputs. IEN should be LOW during the first half of the first cycle of Immediate Instructions.	$Y_{15} - Y_0$	I/O	These output lines are used to present the arithmetic unit or the logic unit output when $\overline{OE}_Y$ is LOW. (CY7C9117 $Y_{15} - Y_0$ and output only.)

Instruction Set

The instruction set of the CY7C9115, CY7C9116, and CY7C9117 is optimized for peripheral controller applications. It features: Bit Set, Bit Reset, Bit Test, Rotate and Merge, Rotate and Compare, and Cyclic-Redundancy-Check (CRC) generation, in addition to standard Single- or Two-Operand logical and arithmetic instructions. A single clock cycle will execute all but the Immediate Instructions which take 2 clock cycles.

The CY7C9115, CY7C9116, and CY7C9117 can operate in three different data modes: bit, byte, and word (16 bits). The LSB of the word is used for Byte Mode. Also in Byte Mode when the status register is specified as the destination, only the LSH (OVR, N, C, Z) of the register is updated. Save Status and Test Status instructions do not change the status register. During Test Status instructions the Y bus (or D bus for the CY7C9117) is undefined; the result is in the CT output.

The eleven instruction types outlined below are described in detail on the following pages.

Single-Operand	Rotate and Compare
Two-Operand	Prioritize
Single Bit Shift	CRC
Bit-Oriented	Status
Rotate by n Bits	No-Op
Rotate and Merge	

$\overline{OE}_Y$ is assumed LOW for all cases, allowing ALU outputs on the Y or D bus.

Instructions are individually distinguished by using OP-CODES and two assigned quadrant bits. Four quadrants, 0 to 3, have been assigned to each instruction type in order to ease groupings of instructions and addressing modes.

Table 1. Operand Source-Destination Combinations

Instruction Type	Operand Combinations ^[2]		
	Source (R/S)	Destination	
Single Operand SOR SONR	RAM ^[3] ACC D D(OE) S(SE) I O	RAM ACC Y Bus Status ACC and Status	
Two Operand TOR1 TOR2 TONR	Source (R)	Source (S)	Destination
	RAM RAM D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus Status ACC and Status
Single Bit Shift SHFTR SHFTNR	Source (U)		Destination
	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
Bit Oriented BOR1 BOR2 BONR	Source (R/S)		Destination
	RAM ACC D		RAM ACC Y Bus
Rotate n Bits ROTR1 ROTR2 ROTNR	Source (U)		Destination
	RAM ACC D		RAM ACC Y Bus
Rotate and Merge ROTM ROTC	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC

Instruction Type	Operand Combinations ^[2]		
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Compare CDAI CDRI CDRA CRAI	D D D RAM	I I ACC I	ACC RAM RAM ACC
Prioritize ^[4] PRT1 PRT2 PRTNR	Source (R)	Mask (S)	Destination
	RAM ACC D	RAM ACC I O	RAM ACC Y Bus
Cyclic Redun- dancy Check CRCF CRCR	Data In	Destination	Polynomial
	QLINK	RAM	ACC
Set Reset Status SETST RSTST SVSTR SVSTNR TEST	Bits Affected		
	OVR, N, C, Z LINK Flag1 Flag2 Flag3		
Store Status	Source		Destination
	Status		RAM ACC Y Bus
Status Load	Source (R)	Source (S)	Destination
	D ACC D	ACC I I	Status Status and ACC
Test Status	Test Condition (CT)		
	(N ∇ OVR) + Z N ∇ OVR Z OVR Low C		Z + $\bar{C}$ N LINK Flag1 Flag2 Flag3
No Operation NOOP	—		

Notes:

- If there is no division between the R/S operand or SOURCE and DESTINATION, the two are a given pair. If a division exists, any combination is possible.
- RAM cannot be used as source when both ACC and STATUS are designated as a DESTINATION.
- OPERAND and MASK must be different sources.

Instruction Set (continued)

Single-Operand Instructions

Each Single-Operand instruction contains four designators:

4. Mode (Byte or Word)
5. Opcode
6. Source
7. Address or Destination

These designators are divided into two basic categories, those that use RAM addresses and those that do not.

The instruction formats shown below are unique for each category. In both cases the desired operation, controlled by the instruction inputs, is performed on the source with the result either placed on the Y bus or stored in the destination or both. The functions of Extending Sign Bit (D(SE)) and Binary Zero (D(OE)) over 16 bits in Word mode are available for cases where 8-bit to 16-bit conversion is necessary. The functions performed using Single-Operand instructions update the LSB of the status register (OVR, N, C, Z) but do not effect the MSB (FLAG1, FLAG2, FLAG3, LINK). Single-operand instructions are limited such that when both the ACC and the status register are the destination, the source cannot be RAM.

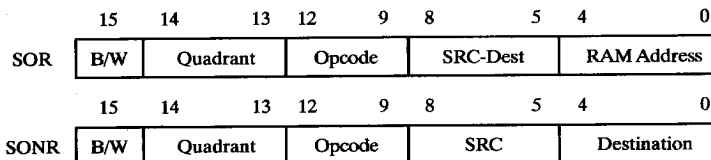


Figure 1. Single-Operand Field Definitions

Table 2. Single-Operand Instruction Set

	15	14	13	12	9	8	5	4	0
Instruction ^[5]	B/W ^[6]	Quad ^[7]	Opcode			R/S ^[8]		Dest ^[8]	RAM Address/Destination
SOR	0 = B 1 = W	10	1100	MOVE	SRC ∇ Dest	0000	SORA	RAM ACC	00000 R00 RAM Reg 00
			1101	COMP	SRC ∇ Dest	0010	SORY	RAM Y Bus	
			1110	INC	SRC + 1 ∇ Dest	0011	SORS	RAM Status	11111 R31 RAM Reg 31
			1111	NEG	SRC + 1 ∇ Dest	0100	SOAR	ACC RAM	
						0110	SODR	D RAM	
						0111	SOIR	I RAM	
						1000	SOZR	O RAM	
						1001	SOZER	D(OE) RAM	
						1010	SOSER	D(SE) RAM	
						1011	SORR	RAM RAM	
Instruction	B/W	Quad	Opcode			R/S ^[8]			Destination
SONR	0 = B 1 = W	11	1100	MOVE	SRC ∇ Dest	0100	SOA	ACC	00000 NRY Y Bus
			1101	COMP	SRC ∇ Dest	0110	SOD	D	00001 NRA ACC
			1110	INC	SRC + 1 ∇ Dest	0111	SOI	1	00100 NRS Status ^[9]
			1111	NEG	SRC + 1 ∇ Dest	1000	SOZ	O	00101 NRAS ACC, Status ^[9]
						1001	SOZE	D(OE)	
						1010	SOSE	D(SE)	

Table 3. Y Bus and Status^[10]

Instruction	Opcode	Description	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR SONR	COMP	SRC ∇ Dest	1 = W 0 = B	Y ∇ SRC	NC	NC	NC	NC	0	U	0	U
	INC	SRC + 1 ∇ Dest		Y ∇ SRC + 1	NC	NC	NC	NC	U	U	U	U
	MOVE	SRC ∇ Dest		Y ∇ SRC	NC	NC	NC	NC	0	U	0	U
	NEG	SRC + 1 ∇ Dest		Y ∇ SRC + 1	NC	NC	NC	NC	U	U	U	U

Notes:

5. Instruction mnemonic.
6. B = Byte Mode, W = Word Mode.
7. Quadrant subdivides instructions into categories.
8. R = Source; S = Source; Dest = Destination.
9. Status is destination,
Status ∇ Yi i = 0 to 3 (byte mode)
i = 0 to 7 (word mode)
10. SRC = Source; NC = No Change; 1 = Set; U = Update; 0 = Reset;
i = 0 to 15 when not specified

Instruction Set (continued)

Two-Operand Instructions

Each Two-Operand instruction is constructed of 5 fields:

1. Mode (Byte or Word)
2. Opcode
3. R Source
4. S Source
5. Address or Destination

These instructions are further divided into those using RAM addresses and those that do not. The first type uses two formats which differ only by quadrant designator.

Functions are performed on the specified R and S sources and results are stored in the specified destination and/or placed on the Y bus. Arithmetic functions update the least significant nibble of the status register (OVR, N, C, Z), while logical functions affect only the N and Z bits. Executions of logical functions clear the OVR and C bits of the status register.

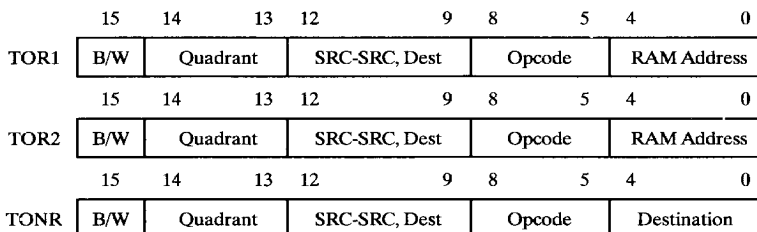


Figure 2. Two-Operand Field Definitions

Table 4. Two-Operand Instruction Set

Instruction	B/W	Quad	R ^[8] S ^[8] Dest ^[8]				Opcode			RAM Address				
TOR1	0 = B 1 = W	00	0000	TORAA	RAM	ACC	ACC	0000	SUBR	S minus R	00000	R00	RAM Reg00	
			0010	TORIA	RAM	I	ACC	0001	SUBRC ^[11]	S minus R with carry	11111	R31	RAM Reg31	
			0011	TODRA	D	RAM	ACC							
			1000	TORAY	RAM	ACC	Y Bus	0010	SUBS	R minus S				
			1010	TORIY	RAM	I	Y Bus	0011	SUBSC ^[11]	R minus S with carry				
			1011	TODRY	D	RAM	Y Bus							
			1100	TORAR	RAM	ACC	RAM	0100	ADD	R plus S				
			1110	TORIR	RAM	I	RAM	0101	ADDC	R plus S with carry				
			1111	TODRR	D	RAM	RAM							
									0110	AND	R $\wedge$ S			
									0111	NAND	R $\wedge$ S			
									1000	EXOR	R $\vee$ S			
						1001	NOR	R $\vee$ S						
						1010	OR	R $\vee$ S						
						1011	EXNOR	R $\vee$ S						
Instruction	B/W	Quad	R ^[8] S ^[8] Dest ^[8]				Opcode			RAM Address				
TOR2	0 = B 1 = W	10	0001	TODAR	D	ACC	RAM	0000	SUBR	S minus R	00000	R00	RAM Reg00	
			0010	TOAIR	ACC	I	RAM	0001	SUBRC ^[11]	S minus R with carry	11111	R31	RAM Reg31	
			0101	TODIR	D	I	RAM							
								0010	SUBS	R minus S				
								0011	SUBSC ^[11]	R minus S with carry				
								0100	ADD	R plus S				
								0101	ADDC	R plus S with carry				
								0110	AND	R $\wedge$ S				
								0111	NAND	R $\wedge$ S				
								1000	EXOR	R $\vee$ S				
								1001	NOR	R $\vee$ S				
								1010	OR	R $\vee$ S				
					1011	EXNOR	R $\vee$ S							

Notes:

11. For subtraction the carry is interpreted as borrow.

Instruction Set (continued)

Table 4. Two-Operand Instruction Set (continued)

Instruction	B/W	Quad	R ^[8]		S ^[8]		Opcode			Destination		
TONR	0 = B 1 = W	11	0001	TODA	D	ACC	0000	SUBR	S minus R	00000	NRY	Y Bus
			0010	TOAI	ACC	I	0001	SUBRC ^[11]	S minus R with carry	00001	NRA	ACC
			0101	TODI	D	I	0010	SUBS	R minus S	00100	NRS	Status ^[9]
							0011	SUBSC ^[11]	R minus S with carry	00101	NRAS	ACC, Status ^[9]
							0100	ADD	R plus S			
							0101	ADDC	R plus S with carry			
							0110	AND	R $\wedge$ S			
							0111	NAND	R $\wedge$ S			
							1000	EXOR	R $\vee$ S			
							1001	NOR	R $\vee$ S			
							1010	OR	R $\vee$ S			
							1011	EXNOR	R $\vee$ S			

Table 5. Y Bus and Status^[12]

Instruction	Opcode	Description	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	ADD	R plus S	0 = B 1 = W	Y $\diamond$ R + S	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		Y $\diamond$ R + S + QC	NC	NC	NC	NC	U	U	U	U
	AND	R $\wedge$ S		Y $\diamond$ R _i AND S _i	NC	NC	NC	NC	0	U	0	U
	EXOR	R $\vee$ S		Y _i $\diamond$ R _i EXOR S _i	NC	NC	NC	NC	0	U	0	U
	EXNOR	R ∇ S		Y _i $\diamond$ R _i EXNOR S _i	NC	NC	NC	NC	0	0	0	U
	NAND	R $\wedge$ S		Y _i $\diamond$ R _i NAND S _i	NC	NC	NC	NC	0	U	0	U
	NOR	R $\vee$ S		Y _i $\diamond$ R _i NOR S _i	NC	NC	NC	NC	0	U	0	U
	OR	R $\vee$ S		Y _i $\diamond$ R _i OR S _i	NC	NC	NC	NC	0	U	0	U
	SUBR	S minus R		Y $\diamond$ S + R + 1	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry		Y $\diamond$ S + R + QC	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		Y $\diamond$ R + S + 1	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		Y $\diamond$ R + S + QC	NC	NC	NC	NC	U	U	U	U

Note:

12. U = Update; NC = No Change; 0 = Reset; 1 = Set; i = 0 to 15 when not specified

Single-Bit Shift Instructions

Single-Bit Shift instructions are constructed of four fields:

1. Mode (Byte or Word)
2. Direction (up or down) and shift linkage
3. Source
4. Destination

These instructions are further divided into those using RAM addresses and those that do not. The shift linkage indicator indicates what is to be loaded into the vacant bit.

During a shift up the LSB may be loaded with a zero, one, or with the link status bit (QLINK), while the MSB is shifted into the QLINK bit. During a shift down, the MSB is loaded with a zero, one, the status carry bit (QC), the exclusive-or of the negative-status bit and the overflow-status bit (QN $\vee$ QOVR), or the link-status bit. The status register's N and Z bits are updated, while the OVR and C bits are reset. Shift down with QN $\vee$ QOVR can be used in two's complement multiplication.

Instruction Set (continued)

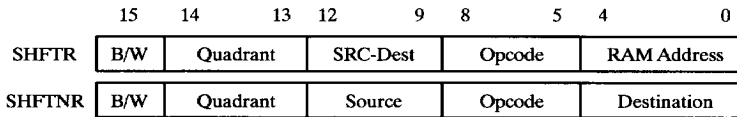


Figure 3. Single Bit Shift Field Definitions

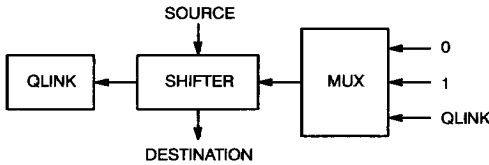


Figure 4. Shift Up Function

7C9115-8

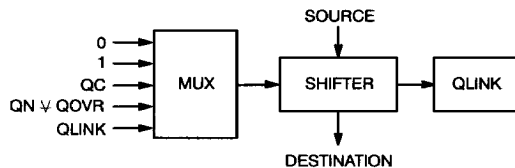


Figure 5. Shift Down Function

7C9115-9

Table 6. Single Bit Shift Instruction Set

Instruction	B/W	Quad	U ^[13]	Dest ^[13]	Opcode	RAM Address/Destination
SHFTR	0 = B 1 = W	10	0110	SHRR RAM	0000 SHUPZ Up 0	00000 R00 RAM Reg 00
			0111	SHDR D RAM	0001 SHUP1 Up 1	
					0010 SHUPL Up QLINK	11111 R31 RAM Reg 31
					0100 SHDNZ Down 0	
					0101 SHDN1 Down 1	
					0110 SHDNL Down QLINK	
					0111 SHDNC Down QC	
					1000 SHDNOV Down QN ∨ QOVR	
Instruction	B/W	Quad	U ^[13]		Opcode	Destination
SHFTNR	0 = B 1 = W	11	0110	SHA ACC	0000 SHUPZ Up 0	00000 NRY Y Bus
			0111	SHD D	0001 SHUP1 Up 1	00001 NRA ACC
					0010 SHUPL Up QLINK	
					0100 SHDNZ Down 0	
					0101 SHDN1 Down 1	
					0110 SHDNL Down QLINK	
					0111 SHDNC Down QC	
					1000 SHDNOV Down QN ∨ QOVR	

Table 7. Y Bus and Status^[10]

Instruction	Opcode	Description	B/W	Y Bus	Flag3	Flag2	Flag1	LINK ^[14]	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	Y _i ∓ SRC _{i-1} , i = 1 to 15; Y ₀ ∓ Shift Input	NC	NC	NC	SRC ₁₅	0	SRC ₁₄	0	U
			0 = B	Y _i ∓ SRC _{i-1} , i = 1 to 7; Y ₀ ∓ Shift Input; Y ₈ ∓ SRC ₇ ; Y _i ∓ SRC _{i-9} for i = 9 to 15	NC	NC	NC	SRC ₇	0	SRC ₆	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN ∨ QOVR	1 = W	Y _i ∓ SRC _{i+1} , i = 0 to 14; Y ₁₅ ∓ Shift Input	NC	NC	NC	SRC ₀	0	Shift Input	0	U
			0 = B	Y _i ∓ SRC _{i+1} , i = 0 to 6; Y _i ∓ SRC _{i-7} , i = 8 to 14; Y _{7, 15} ∓ Shift Input	NC	NC	NC	SRC ₀	0	Shift Input	0	U

Notes:

13. U = Source; Dest = Destination

14. Shifted output is loaded into the QLINK.

Instruction Set (continued)

Bit-Oriented Instructions

Bit-Oriented instructions are constructed from four fields:

1. Mode (Byte or Word)
2. Operation
3. Source or Destination
4. Bit position operated on (0 = LSB)

These instructions are further divided into those using RAM addresses and those that do not. The specified function operates on the given source and the result is stored in the specified destination and/or on the Y bus.

Set Bit n: Forces the n th bit to ONE without affecting other bit positions.

Reset Bit n: Forces the n th bit to ZERO without affecting other bit positions.

Test Bit n: Sets the Z status bit to the state of bit n .

Load 2ⁿ: Loads ZERO in bit position n and sets all other bits.

Load 2ⁿ: Loads ONE in bit position n and clears all other bits.

Increment 2ⁿ: Adds 2ⁿ to the operand.

Decrement 2ⁿ: Subtracts 2ⁿ from the operand.

Load, Set, Reset, and Test instructions update N and Z status bits while forcing OVR and C bits to ZERO. Arithmetic operations affect the entire lower nibble of the status register (OVR, C, N, and Z).

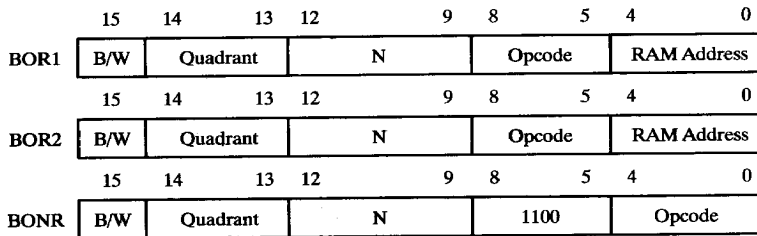


Figure 6. Bit-Oriented Field Definitions

Table 8. Bit-Oriented Instruction Set

Instruction	B/W	Quadrant	n	Opcode		RAM Address				
BOR1	0 = B 1 = W	11	0 to 15	1101	SETNR	Set RAM, bit n	00000	R00	RAM Reg 00	
				1110	RSTNR	Reset RAM, bit n				
				1111	TSTNR	Test RAM, bit n	11111	R31	RAM Reg 31	
Instruction	B/W	Quadrant	n	Opcode		RAM Address				
BOR2	0 = B 1 = W	10	0 to 15	1100	LD2NR	2 ⁿ ♦ RAM	00000	R00	RAM Reg 00	
				1101	LDC2NR	2 ⁿ ♦ RAM				
				1110	A2NR	RAM plus 2 ⁿ ♦ RAM	11111	R31	RAM Reg 31	
				1111	S2NR	RAM minus 2 ⁿ ♦ RAM				
Instruction	B/W	Quadrant	n	Opcode		Opcode				
BONR	0 = B 1 = W	11	0 to 15	1100	00000	TSTNA	Test ACC, bit n			
					00001	RSTNA	Reset ACC, bit n			
					00010	SETNA	Set ACC, bit n			
					00100	A2NA	ACC plus 2 ⁿ ♦ ACC			
					00101	S2NA	ACC minus 2 ⁿ ♦ ACC			
					00110	LD2NA	2 ⁿ ♦ ACC			
					00111	LDC2NA	2 ⁿ ♦ ACC			
					10000	TSTND	Test D, bit n			
					10001	RSTND	Reset D, bit n			
					10010	SETND	Set D, bit n			
					10100	A2NDY	D plus 2 ⁿ ♦ Y Bus			
					10101	S2NDY	D minus 2 ⁿ ♦ Y Bus			
					10110	LS2NY	2 ⁿ ♦ Y Bus			
					10111	LDC2NY	2 ⁿ ♦ Y Bus			

Instruction Set (continued)

Rotate by n Bits Instructions

The Rotate by n Bits instructions contain four indicators: byte or word mode, source, destination, and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in Table 9. Under the control of instruction inputs, the n indicator specifies

the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y bus or both. An example of this instruction is given in Figure 8. In the Word mode, all 16 bits are rotated up; while in the Byte mode, only the lower 8 bits (0 – 7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by $(16 - n)$ bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by $(8 - n)$ bits. The N and Z bits of the status register are affected and OVR and C bits are forced to zero.

	15	14	13	12	9	8	5	4	0
ROTR1	B/W	Quadrant	n		SRC-Dest				RAM Address
ROTR2	B/W	Quadrant	n		SRC-Dest				RAM Address
ROTRN	B/W	Quadrant	n		1100				SRC-Dest

Figure 7. Rotate by n Bits Shift Field Definitions

EXAMPLE: $n = 4$, Word Mode

Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: $n = 4$, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 8. Rotate by n Example

Table 9. Rotate by n Bits Instruction Set

Instruction	B/W	Quadrant	n	U ^[13]	Dest ^[13]	RAM Address
ROTR1	0 = B 1 = W	00	0 to 15	1100	RTRA	RAM ACC
				1110	RTRY	RAM Y Bus
				1111	RTRR	RAM RAM
ROTR2	0 = B 1 = W	01	0 to 15	0000	RTAR	ACC RAM
				0001	RTDR	D RAM
				1111		
ROTRN	0 = B 1 = W	11	0 to 15	1100		U ^[13] Dest ^[13]
					11000	RTDY D Y Bus
					11001	RTDA D ACC
					11100	RTAY ACC Y Bus
					11101	RTAA ACC ACC

Table 10. Y Bus and Status^[10]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTRN		1 = W	$Y_i \leftarrow SRC_{(i-n) \bmod 16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_i + 8 = SRC_{(i-n) \bmod 8}$ for $i = 0$ to 7	NC	NC	NC	NC	0	SRC_{6-n}	0	U

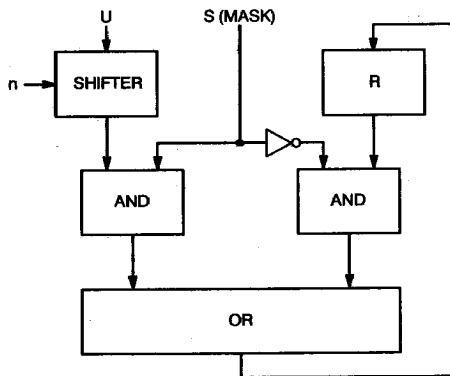
Instruction Set (continued)

Rotate and Merge Instructions

Each Rotate and Merge instruction consists of five fields:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask Location (S)
5. Number of bits Rotated (n)

This shift register rotates source U up n places. ANDing with the mask causes any bit i to be passed from the rotated source that corresponds to a set bit in mask position i . The R input is not shifted, but is masked by the compliment of mask S, so that a ZERO in mask bit i will pass bit i of R. The ORed result is stored in register R. Rotate and Merge operations update the N and Z status bits, while clearing the OVR and C bits.



7C9115-10

Figure 9. Rotate and Merge Function

	15	14	13	12	9	8	5	4	0
ROTM	B/W	Quadrant	n			U, R, S			RAM Address

EXAMPLE: $n = 4$, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 10. Rotate and Merge Field Definitions

Table 11. Rotate and Merge Instruction Set

Instruction	B/W	Quadrant	n	U ^[15] R/Dest ^[15] S ^[15]			RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111	MDAI	D	ACC	I	00000 R00 RAM Reg 00
				1000	MDAR	D	ACC	RAM	...
				1001	MDRI	D	RAM	I	11111 R31 RAM Reg 31
				1010	MDRA	D	RAM	ACC	
				1100	MARI	ACC	RAM	I	
				1110	MRAI	RAM	ACC	I	

Notes:

15. U = Rotated Source; R/Dest = Non-Rotated Source/Destination;

S = Mask

Table 12. Y Bus and Status^[12]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1 = W	$Y_i \oplus (\text{Non Rot Op})_i \cdot (\text{mask})_i + (\text{Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \oplus (\text{Non Rot Op})_i \cdot (\text{mask})_i + (\text{Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

Instruction Set (continued)

Rotate and Compare Instructions

The five fields of the Rotate and Compare instructions are:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask (S)
5. Number of bits Rotated (n)

Input U is rotated n bits, ANDed with the inversion of S and compared with the input R ANDed with the inversion of S. Thus, a zero in the mask S will allow that bit of both inputs to be compared. The Z bit of the status register is set if the comparison passes, and reset if it does not. OVR and C bits are reset in the status register.

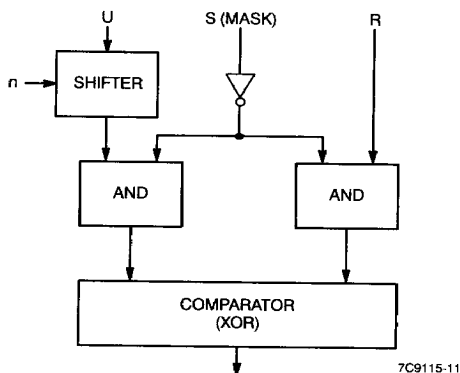


Figure 11. Rotate and Compare Function

	15	14	13	12	9	8	5	4	0
ROTC	B/W	Quadrant		n	U, R, S		RAM Address		

EXAMPLE: $n = 4$, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0001	0101	1111	1111
Z (Status)	= 1			

Figure 12. Rotate and Compare Field Definitions

Table 13. Rotate and Compare Instruction Set

Instruction	B/W	Quadrant	n	U ^[16]		R ^[16]		S ^[16]		RAM Address	
ROTC	0 = B 1 = W	01	0 to 15	0010	CDAI	D	ACC	I		00000	R00 RAM Reg 00
				0011	CDRI	D	RAM	I			
				0100	CDRA	D	RAM	ACC			
				0101	CRAI	RAM	ACC	I		11111	R31 RAM Reg 31

Notes:

16. U = Rotated Source; R = Non-Rotated Source; S = Mask

Table 14. Y Bus and Status^[12]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \downarrow (\text{Non Rot Op})_i \bullet (\text{mask})_i \vee (\text{Rot Op})_{(i-n) \bmod 16} \bullet (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \downarrow (\text{Non Rot Op})_i \bullet (\text{mask})_i \vee (\text{Rot Op})_{(i-n) \bmod 8} \bullet (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

Instruction Set (continued)

Prioritize Instructions

The four fields of the Prioritize instructions are:

1. Mode (Byte or Word)
2. Mask Source (S)
3. Operand Source (R)
4. Destination

The inverter mask, S is ANDed with R. A "one" in S prohibits that bit from participating in the priority encoding. From the 16-bit input, the priority encoder outputs a 5-bit binary weighted code indicating the bit-position of the highest priority active bit. If there are no active bits, the output is zero. See *Figure 14* for operation in both word and byte mode. Using Prioritize updates the N and Z bits of the status register, and forces C and OVR to zero. This instruction is limited in that the operand and the mask must be different sources.

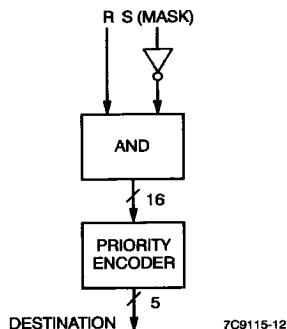


Figure 13. Prioritize Function

15	14	13	12	9	8	5	4	0
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (S)				
B/W	Quad	Mask (S)	Destination	RAM Address/ Source (R)				
B/W	Quad	Mask (S)	Source (R)	RAM Address/ Destination				
B/W	Quad	Mask (S)	Source (R)	Destination				

Word Mode		Byte Mode ^[17]	
Highest Priority Bit Active	Encoder Output	Highest Priority Bit Active	Encoder Output
None	0	None	0
15	1	7	1
14	2	6	2
:	:	:	:
1	15	1	7
0	16	0	8

Figure 14. Prioritize Instruction Field Definitions

Note:

17. Bits 8 through 15 not available.

Instruction Set (continued)

Table 15. Prioritize Instruction Set

Instruction	B/W	Quad	Destination			Source (R)			RAM Address/Mask (S)		
PRT1	0 = B 1 = W	10	1000	PRT1A	ACC	0111	PRT1A	ACC	00000	R00	RAM Reg 00
			1010	PR1Y	Y Bus	1001	PR1D	D	11111	R31	RAM Reg 31
			1011	PR1R	RAM						
Instruction	B/W	Quad	Mask (S)			Destination			RAM Address/Source (R)		
PRT2	0 = B 1 = W	10	1000	PRA	ACC	0000	PR2A	ACC	00000	R00	RAM Reg 00
			1010	PRZ	O	0010	PR2Y	Y Bus	11111	R31	RAM Reg 31
			1011	PRI	I						
Instruction	B/W	Quad	Mask (S)			Source (R)			RAM Address/Destination		
PRT3	0 = B 1 = W	10	1000	PRA	ACC	0011	PR3R	RAM	00000	R00	RAM Reg 00
			1010	PRZ	O	0100	PR3A	ACC	11111	R31	RAM Reg 31
			1011	PRI	I	0110	PR3D	D			
Instruction	B/W	Quad	Mask (S)			Source (R)			Destination		
PRTNR	0 = B 1 = W	11	1000	PRA	ACC	0100	PRTA	ACC	00000	NR0	Y Bus
			1010	PRZ	O	0110	PRTD	D	00001	NRA	ACC
			1011	PRI	I						

Table 16. Y Bus and Status—Prioritize Instruction^[10]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2		1 = W	$Y_i \leftarrow \text{CODE}(\text{SCR}_n \cdot \text{mask}_n);$ $Y_m \leftarrow 0; i = 0 \text{ to } 4 \text{ and } n = 0 \text{ to } 15$ $m = 5 \text{ to } 15$	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	$Y_i \leftarrow \text{CODE}(\text{SCR}_n \cdot \text{mask}_n);$ $Y_m \leftarrow 0; i = 0 \text{ to } 3 \text{ and } n = 0 \text{ to } 7$ $m = 4 \text{ to } 15$	NC	NC	NC	NC	0	U	0	U

CRC Instructions

The single designator for this instruction is the address of the RAM location that is used as the checksum register. Two CRC instructions, CRC Forward and CRC Reverse, are available. These instructions give the procedure for determining the check bits in a CRC calculation. Since the CRC standards do not specify which data bit is transmitted first, the MSB or the LSB, both Forward and

Reverse options are available to the user. The process for generating the check bits for the CRC Forward and Reverse operations are illustrated in Figures 16 and 17. The ACC is used as a polynomial mask while the RAM contains the partial sum and eventually the final check sum. The serial input comes from the QLINK bit of the status register. Status register bits OVR and C are forced to zero while LINK, N, and Z bits are updated.

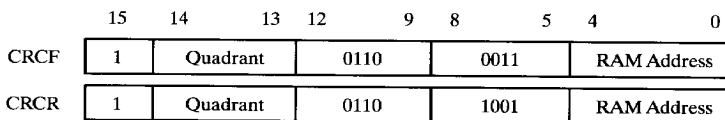
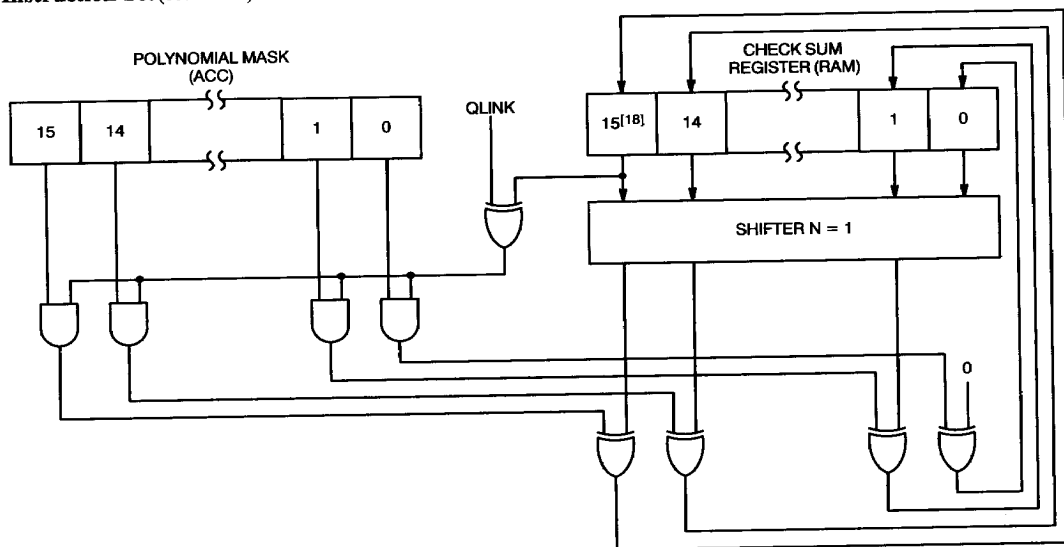


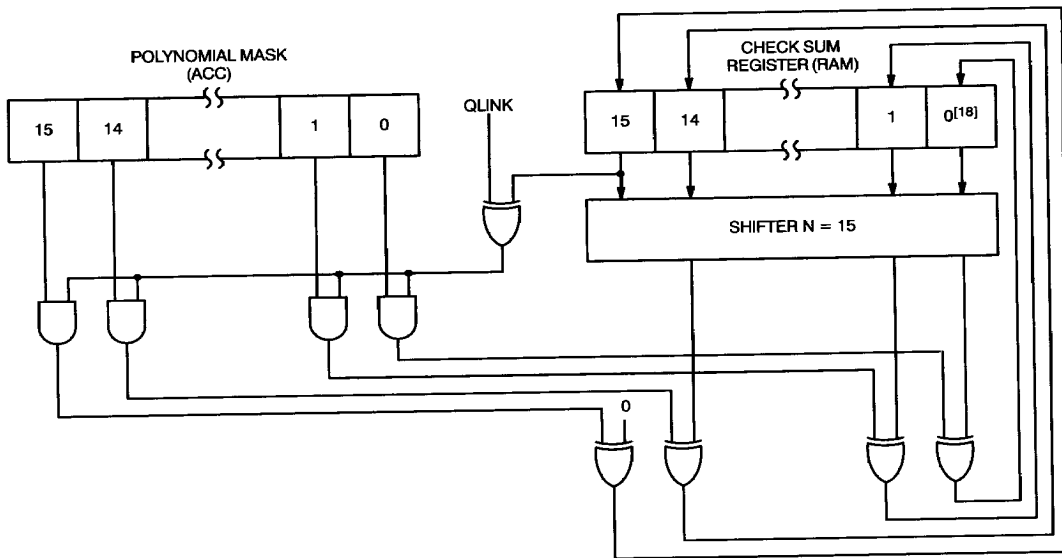
Figure 15. Cyclic-Redundancy-Check Definitions

Instruction Set (continued)



7C9115-13

Figure 16. CRC Forward Function



7C9115-14

Figure 17. CRC Reverse Function

Note:
18. This bit must be transmitted first.

Instruction Set (continued)

Table 17. Cyclic Redundancy Check Instruction Set

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000	R00	RAM Reg 00
					11111	R31	RAM Reg 31
Instruction	B/W	Quad			RAM Address		
CRCR	1	10	0110	1001	00000	R00	RAM Reg 00
					11111	R31	RAM Reg 31

Table 18. Y Bus and Status^[12]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_1 \nabla [(QLINK \nabla RAM_{15}) \cdot ACC_1]$ ∇RAM_{i-1} for $i = 15$ to 1 $Y_0 \nabla [(QLINK \nabla RAM_{15}) \cdot ACC_0] \nabla 0$	NC	NC	NC	$RAM_{15}^{[19]}$	0	U	0	U
CRCR		1 = W	$Y_1 \nabla [(QLINK \nabla RAM_0) \cdot ACC_1]$ ∇RAM_{i+1} for $i = 14$ to 0 $Y_{15} \nabla [(QLINK \nabla RAM_0) \cdot ACC_{15}] \nabla 0$	NC	NC	NC	$RAM_0^{[19]}$	0	U	0	U

Notes:

19. QLINK is loaded with the shifted out bit from the checksum register.

20. $\overline{IEN}^*$ test status instruction has priority over $T_1 - T_4$ instruction.

Status Instructions

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	Link	OVR	N	C	Z

Set Status: Specifies which bits in the status register are to be set.

Reset Status: Specifies which bits in the status register are to be cleared.

Store Status: Indicates byte or word and the destination into which the processor status is saved. The register is always stored in the low byte of the destination. The high byte is unchanged for RAM storage and is loaded with zeroes for ACC storage.

Load Status: Imbedded in the Single- and Two-Operand instructions.

Test Status: Instructions specify which of the twelve possible test conditions are to be placed on the conditional test output. In addition to the eight status bits, four logical may be selected: $N \nabla OVR$, $(N \nabla OVR) + Z$, $Z + C$, and LOW. These functions are useful in testing two's complement and unsigned number arithmetic operations.

The status register may also be tested via the T bus as shown in Table 19. The instruction lines I_4 through I_1 have bus priority for testing the status register on the CT output.^[20]

Table 19. Condition Code Output Selection

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	$(N \nabla OVR) + Z$
0	0	0	1	$N \nabla OVR$
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW
0	1	0	1	C
0	1	1	0	$Z + C$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

	15	14	13	12	9	8	5	4	0
SETST	0	Quad	1011	1010	Opcode				
RSTST	0	Quad	1010	1010	Opcode				
SVSTR	B/W	Quad	0111	1010	RAM Address/ Dest				
SVSTNR	B/W	Quad	0111	1010	Destination				

Figure 18. Status

Instruction Set (continued)

Table 20. Status Instruction Set

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011	SONCZ	Set OVR, N, C, Z
					00101	SL	Set LINK
					00110	SF1	Set Flag1
					01001	SF2	Set Flag2
					01010	SF3	Set Flag3
Instruction	B/W	Quad			Opcode		
RSTST	0	11	1010	1010	00011	RONCZ	Reset OVR, N, C, Z
					00101	RL	Reset LINK
					00110	RF1	Reset Flag1
					01001	RF2	Reset Flag2
					01010	RF3	Reset Flag3
Instruction	B/W	Quad			RAM Address/Destination		
SVSTR	0 = B 1 = W	10	0111	1010	00000	R00	RAM Reg 00
					11111	R31	RAM Reg 31
Instruction	B/W	Quad			Destination		
SVSTNR	0 = B 1 = W	11	0111	1010	00000	NRY	Y Bus
					00001	NRA	ACC
Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000	TNOZ	Test (N $\neq$ OVR) + Z
					00010	TNO	Test N $\neq$ OVR
					00100	TZ	Test Z
					00110	TOVR	Test OVR
					01000	TLOW	Test LOW
					01010	TC	Test C
					01100	TZC	Test Z + $\bar{C}$
					01110	TN	Test N
					10000	TL	Test LINK
					10010	TF1	Test Flag1
					10100	TF2	Test Flag2
					10110	TF3	Test Flag3

Instruction Set (continued)

Table 21. Y Bus and Status^[12]

Instruction	Opcode	Description	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	Y _i $\neq$ 0 for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SETST	SONCZ	Set OVR, N, C, Z	0 = B	Y _i $\neq$ 1 for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
SVSTR		Save Status ^[21]	0 = B	Y _i $\neq$ Status for i $\neq$ 0 to 7;	NC	NC	NC	NC	NC	NC	NC	NC
SVSTNR			1 = W	Y _i $\neq$ 0 for i = 8 to 15								
Test	TNOZ	Test(N ∇ OVR) + Z	0 = B	Note 22	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test (N ∇ OVR)			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test Z + C			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

Notes:

21. In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16 bits from the Y bus are loaded into the RAM or ACC.
22. Y Bus is Undefined.

No-Op Instruction

The No-Op Instruction does not affect any internal registers; the Status Register, RAM register and AC register are left unchanged. The 16-bit opcode is fixed.

	15	14	13	12	9	8	5	4	0
NO-OP	0	11		1000		1010		00000	

Figure 19. No-Op Field Definition

Table 22. Status Instruction Set

Instruction	B/W	Quad			
No-Op	0	11	1000	1010	0000

Table 23. Y Bus and Status^[10]

Instruction	Opcode	B/W	Y Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
No-Op		0 = B	Note 22	NC	NC	NC	NC	NC	NC	NC	NC

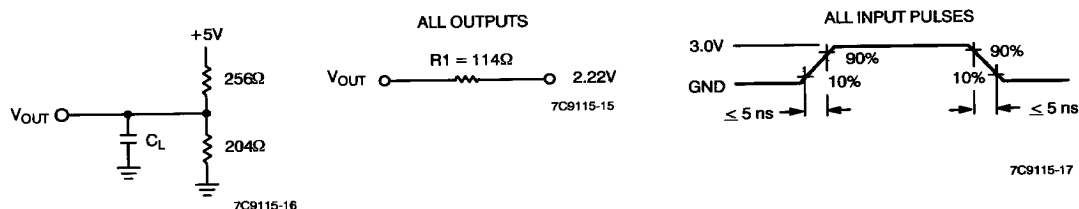
Electrical Characteristics Over Commercial and Military Operating Range^[23]

Parameters	Description	Test Conditions	Min.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.6 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC}	V
V _{IL}	Input LOW Voltage			0.8	V
I _{IX}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC} , V _{CC} = Max.	-10	+10	μA
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _{OUT} = V _{SS} to V _{CC}	-10	+10	μA
I _{SC}	Output Short Circuit Current ^[24]	V _{CC} = Max., V _{OUT} = 0V		-85	mA
I _{CC} (Q ₁) ^[25]	Supply Current (Quiescent)	V _{SS} ≤ V _{IN} ≤ V _{IL} or V _{IH} ≤ V _{IN} ≤ V _{CC} ; $\overline{OE}_Y$ = HIGH	Commercial	126	mA
			Military	145	
I _{CC} (Q ₂)	Supply Current (Static)	V _{IN} = V _{CC} or GND, V _{CC} = Max., I _{OPER} = 0 μA	Commercial	68	mA
			Military	78	
I _{CC} (Max.) ^[25]	Supply Current	V _{CC} = Max., f _{CLK} = 10 MHz; $\overline{OE}_Y$ = HIGH	Commercial	145	mA
			Military	166	

Capacitance^[26]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		7	pF

Output Loads Used for AC Performance Characteristics^[27, 28]



Notes:

23. V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V.
24. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
25. To calculate I_{CC} at any given frequency, use I_{CC}(Q₁) + I_{CC}(AC) where I_{CC}(Q₁) is shown above and I_{CC}(AC) = (1.9 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC}(AC) = (2.1 mA/MHz) × Clock Frequency for Military temperature range.
26. Tested on a sample basis.
27. C_L = 50 pF includes scope probe, wiring and stray capacitance.
28. C_L = 5 pF for output disable tests.

Commercial Switching Characteristics^[29]

Combinatorial Propagation Delays (ns)

To Output	Y ₀ – Y ₁₅			T ₁ – T ₄			CT		
From Input	Y ₀ – Y ₁₅			T ₁ – T ₄			CT		
Speed(ns)	35	45	65	35	45	65	35	45	65
I ₀ – I ₄ (ADDR)	35	45	65	35	52	73			
I ₀ – I ₁₅ (DATA)	35	45	65	35	52	73			
I ₀ – I ₁₅ (INST)	35	45	65	35	52	73	20	29	30
DLE ^[30]	20	32	55	30	32	55			
T ₁ – T ₄							15	25	27
CP	30	32	60	30	32	66	25	25	37
Y ₀ – Y ₁₅	20	32	53	30	32	53			
IEN							15	25	25

Enable/Disable Times^[31] (ns)

From Input	To Output	Enable						Disable					
		T _{PZH}			T _{PZL}			T _{PHZ}			T _{PLZ}		
Speed (ns)		35	45	65	35	45	65	35	45	65	35	45	65
OE _Y	Y ₀ – Y ₁₅	18	20	22	18	20	22	18	20	22	18	20	22
OE _T	T ₁ – T ₄	15	20	22	15	20	22	15	20	22	15	20	22

Clock and Pulse Requirements (ns)

Input	Minimum LOW Time			Minimum HIGH Time		
Speed (ns)	35	45	65	35	45	65
CP	15	15	20	15	15	15
DLE				15	15	15
IEN	15	15	20			

Notes:

29. T_A = 0°C to +70°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF.

30. DLE is guaranteed by other tests.

31. C_L = 5 pF, Disable Only.

Set-Up and Hold Times (ns)

Set-Up and Hold Times (ns)															
Note 32	Input	With Respect To	HIGH-to-LOW Transition						LOW-to-HIGH Transition						Comments
			Set-Up			Hold			Set-Up			Hold			
	Speed (ns)		35	45	65	35	45	65	35	45	65	35	45	65	
1	I ₀ – I ₄ (RAM Addr)	CP	12	13	13	0	0	0							Single Addr (Source)
2	I ₀ – I ₄ (RAM Addr)	CP & IEN	5	5	5	⚡ Do Not Change ⚡						0	0	0	Two Addr (Destination)
3	I ₀ – I ₁₅ (Data)	CP							40	43	60	0	0	0	
4	I ₀ – I ₄ (RAM Addr) ^[33]	IEN	15 ^[34]	18 ^[34]	24 ^[34]	4 ^[34]	5 ^[34]	10 ^[34]							Two Addr (Immediate)
5	I ₀ – I ₁₅ (Instr) ^[35]	CP	15 ^[34]	18 ^[34]	24 ^[34]	4 ^[34]	5 ^[34]	10 ^[34]	40	43	60	0	0	0	
6	IEN ^[33]	CP										8	8	8	Two Addr (Immediate)
7	IEN HIGH	CP	5	5	5							0	1	2	Disable
8	IEN LOW	CP							10	10	10	0	1	1	Enable
9	IEN LOW	CP	5	5	5	1	1	0							Note 34
10	SRE	CP							12	12	12	0	0	0	
11	Y ^[36]	CP							32	32	42	0	0	0	
12	Y ^[36]	DLE	6	6	6	5	5	5							
13	DLE	CP							20	25	43	0	0	0	

Military Switching Characteristics^[37]

Combinatorial Propagation Delays (ns)

To Output	Y ₀ - Y ₁₅			T ₁ - T ₄			CT		
From Input	Y ₀ - Y ₁₅			T ₁ - T ₄			CT		
Speed (ns)	40	65	79	40	45	79	40	65	79
I ₀ - I ₄ (ADDR)	40	65	79	40	65	79			
I ₀ - I ₁₅ (DATA)	40	65	79	40	65	79			
I ₀ - I ₁₅ (INST)	40	65	79	40	65	79	22	26	29
DLE ^[30]	20	52	62	30	52	62			
T ₁ - T ₄							15	26	29
CP	30	57	67	35	65	75	33	33	39
Y ₀ - Y ₁₅	20	52	60	30	52	60			
IEN							20	26	29

Notes:

32. t_{sx} and t_{hx} referenced on the waveforms are looked up on this table by x = line number on the left. Ex: t_{SL} = 13 ns for -53 ns devices.
 33. CY7C9117 only.
 34. Timing for immediate instruction for first cycle.

35. CY7C9115 and CY7C9116 only.

36. Y = D for CY7C9117.

37. T_A = -55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF.

Enable/Disable Times^[31] (ns)

From Input	To Output	Enable						Disable					
		T _{PZH}			T _{PZL}			T _{PHZ}			T _{PLZ}		
Speed (ns)		40	65	79	40	65	79	40	65	79	40	65	79
OE _Y	Y ₀ – Y ₁₅	18	22	25	18	22	25	18	18	25	18	18	25
OE _T	T ₁ – T ₄	18	18	20	18	18	20	15	15	20	15	15	20

Clock and Pulse Requirements (ns)

Input	Minimum Low Time			Minimum High Time		
Speed (ns)	40	65	79	40	65	79
CP	15	20	25	15	15	15
DLE				15	15	15
IEN	15	15	15			

Set-Up and Hold Times (ns)

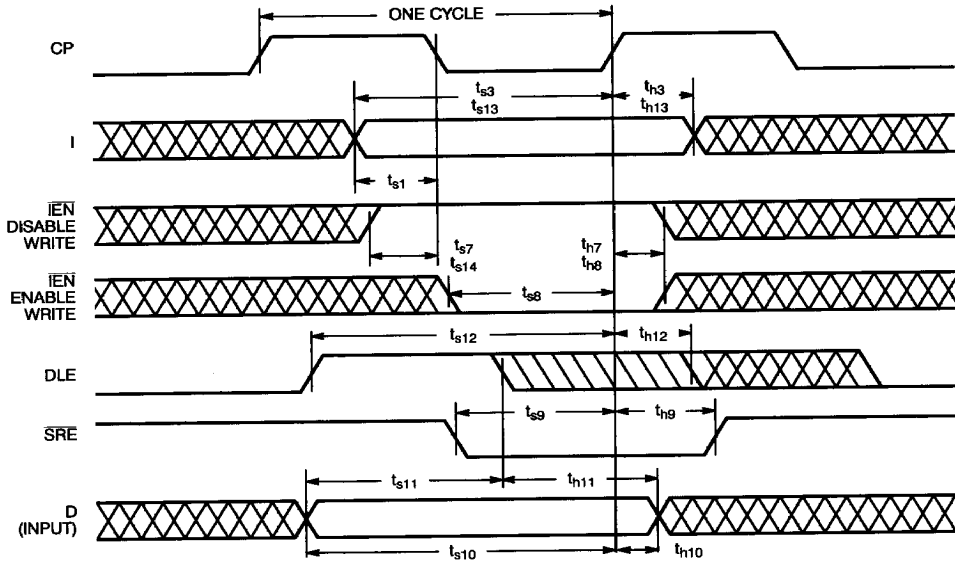
Note 38	Input	With Respect To	HIGH-to-LOW Transition						LOW-to-HIGH Transition						Comments
			Set-Up			Hold			Set-Up			Hold			
Speed (ns)			40	65	79	40	65	79	40	65	79	40	65	79	
1	I ₀ – I ₄ (RAM Addr)	CP	12	12	12	0	1	1							Single Addr (Source)
2	I ₀ – I ₄ (RAM Addr)	CP  IEN	5	7	7	◆ Do Not Change ◆						0	0	0	Two Addr (Destination)
3	I ₀ – I ₁₅ (Data)	CP							43	56	65	0	0	0	
4	I ₀ – I ₄ (RAM Addr) ^[33]	IEN	15 ^[34]	25	27 ^[34]	5 ^[34]	12	12 ^[34]							Two Addr (Immediate)
5	I ₀ – I ₁₅ (Instr) ^[35]	CP	15 ^[34]	25	27 ^[34]	5 ^[34]	12	12 ^[34]	45	56	65	0	2	2	
6	IEN ^[33]	CP										8	8	8	Two Addr (Immediate)
7	IEN HIGH	CP	5	5	5							0	2	2	Disable
8	IEN LOW	CP							10	10	12	0	3	3	Enable
9	IEN LOW	CP	7	7	7	0	3	3							Note 34
10	SRE	CP							10	10	12	0	1	1	
11	Y ^[36]	CP							39	45	53	0	0	0	
12	Y ^[36]	DLE	7	7	7	3	3	3							
13	DLE	CP							20	46	54	0	0	0	

Notes:

38. t_{SX} and t_{HX} referenced on the waveforms are looked up on this table by x = line number on the left. Ex: t_{S1} = 24 ns for – 79 ns devices.

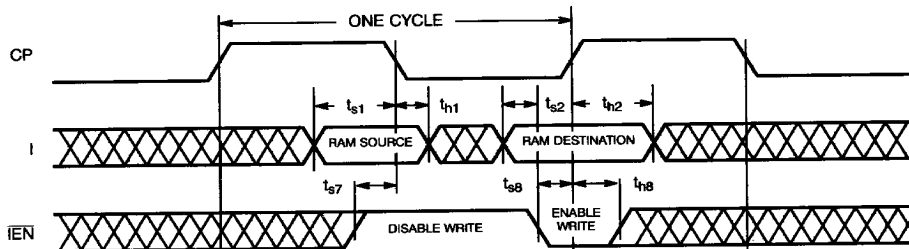
Switching Waveforms

Single Address Access Timing^[39]



7C9115-18

Double Address Access Timing



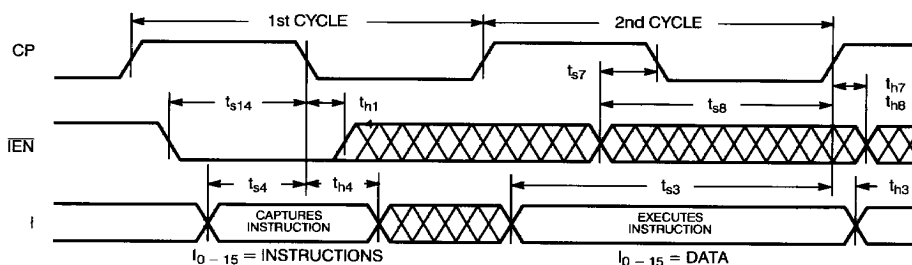
7C9115-19

Note:

39. If t_{h11} is satisfied, t_{h10} need not be satisfied.

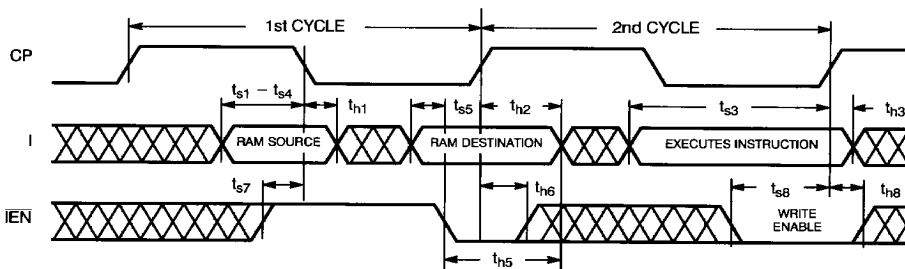
Switching Waveforms (continued)

One-Address Immediate Instruction Cycle Timing



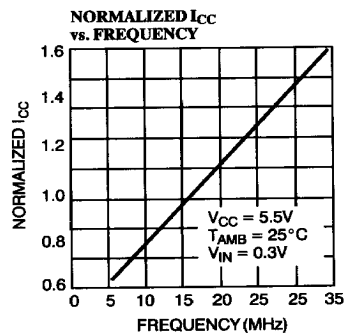
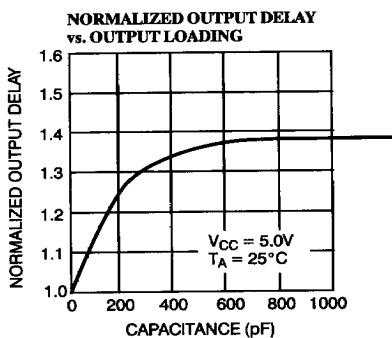
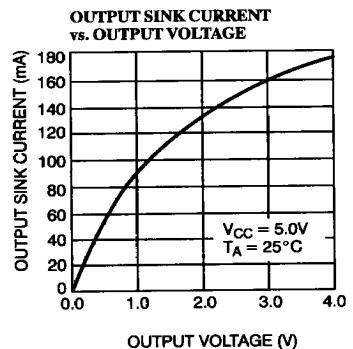
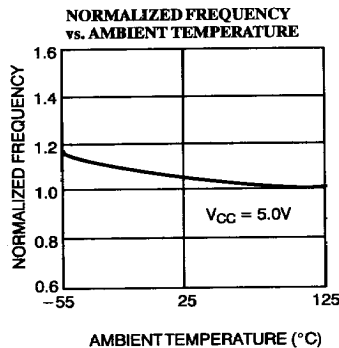
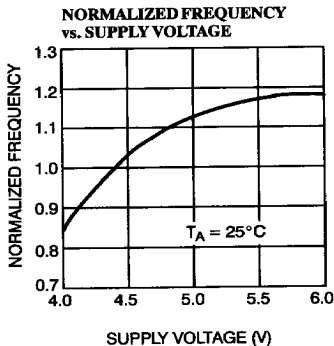
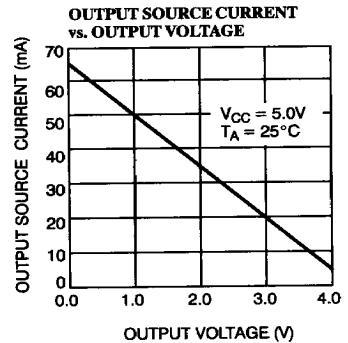
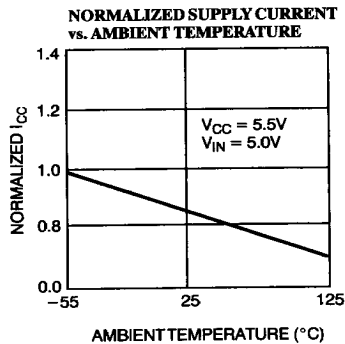
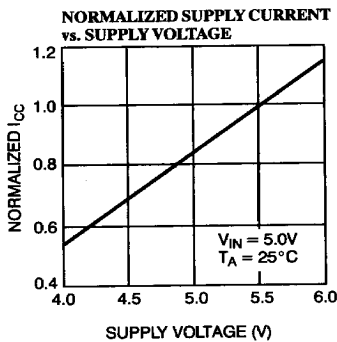
7C9115-20

Two-Address Immediate Instruction Timing (7C9117 Only)



7C9115-21

Typical DC and AC Characteristics



7C9115-22

Cross References for Set-Up and Hold Times

Note 40	HIGH-to-LOW Transition		LOW-to-HIGH Transition	
	Set-Up	Hold	Set-Up	Hold
1	t _{S1}	t _{h1}		
2	t _{S2}			t _{h2}
3			t _{S3}	t _{h3}
4	t _{S5}	t _{h5}		
5	t _{S4}	t _{h4}	t _{S13}	t _{h13}
6				t _{h6}
7	t _{S7}			t _{h7}
8			t _{S8}	t _{h8}
9	t _{S14}	t _{h14}		
10			t _{S9}	t _{h9}
11			t _{S10}	t _{h10}
12	t _{S11}	t _{h11}		
13			t _{S12}	t _{h12}

Notes:

40. Refer to Set-Up and Hold times shown on pages 25 and 26.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9115-35JC	J69	Commercial
45	CY7C9115-45JC	J69	
65	CY7C9115-65JC	J69	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9116-35DC	D28	Commercial
	CY7C9116-35JC	J81	
	CY7C9116-35LC	L69	
40	CY7C9116-40DMB	D28	Military
	CY7C9116-40LMB	L69	
45	CY7C9116-45DC	D28	Commercial
	CY7C9116-45JC	J81	
	CY7C9116-45LC	L69	
65	CY7C9116-65DC	D28	Military
	CY7C9116-65JC	J81	
	CY7C9116-65LC	L69	
	CY7C9116-65DMB	D28	
	CY7C9116-65LMB	L69	
79	CY7C9116-79DMB	D28	Military
	CY7C9116-79LMB	L69	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9117-35GC	G68	Commercial
	CY7C9117-35JC	J81	
	CY7C9117-35LC	L81	
40	CY7C9117-40GMB	G68	Military
	CY7C9117-40LMB	L81	
45	CY7C9117-45GC	G68	Commercial
	CY7C9117-45JC	J81	
	CY7C9117-45LC	L81	
65	CY7C9117-65GC	G68	Commercial
	CY7C9117-65JC	J81	
	CY7C9117-65LC	L81	
	CY7C9117-65GMB	G68	Military
	CY7C9117-65LMB	L81	
79	CY7C9117-79GMB	G68	Military
	CY7C9117-79LMB	L81	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{SC}	1, 2, 3
I _{CC} (Q ₁)	1, 2, 3
I _{CC} (Max.)	1, 2, 3

Switching Characteristics

Parameters	Subgroups
I ₀ – I ₄ (Addr)	7, 8, 9, 10, 11
I ₀ – I ₁₅ (Data)	7, 8, 9, 10, 11
I ₀ – I ₁₅ (Instr)	7, 8, 9, 10, 11
DLE	7, 8, 9, 10, 11
T ₁ – T ₄	7, 8, 9, 10, 11
CP	7, 8, 9, 10, 11
Y ₀ – Y ₂₅	7, 8, 9, 10, 11
$\overline{\text{IEN}}$	7, 8, 9, 10, 11
$\overline{\text{OE}}_{\text{Y}}$	7, 8, 9, 10, 11
OE _T	7, 8, 9, 10, 11
CP	7, 8, 9, 10, 11

Document #: 38-00057-C