ADVANCED INFORMATION

CY7C9335

SMPTE-259M/DVB-ASI Descrambler/Framer-Controller

Features

- **Fully compatible with SMPTE-259M**
  - **SMPTE-125M compliant for 4:2:2 component video**
  - **SMPTE-244M compliant for 4fsc composite video**
- **Fully compatible with DVB-ASI**
- **Operates from a single +5V or –5V supply**
- **84-pin PLCC or 100-pin TQFP packages**
- **Decodes 10-bit parallel digital streams for any rate from 16–40 Mcharacters/sec (160–400 Mbits/sec serial)**
- **Operates with CY7B933 HOTLink deserializer/receiver**
- **$X^9 + X^4 + 1$ descrambler and NRZI-to-NRZ decoder may be bypassed for raw data output**

Functional Description

SMPTE-259M Operation

The CY7C9335 is a CMOS integrated circuit designed to decode SMPTE-125M and SMPTE-244M bit-parallel digital characters (or other data formats) using the SMPTE-259M decoding rules. Following decoding, the characters are framed by locating the 30-bit TRS pattern in the parallel character stream. The framed characters are then output.

The inputs of the CY7C9335 are designed to be directly mated to a CY7B933 HOTLink receiver, which converts the SMPTE-259M compatible high-speed serial data stream into 10-bit parallel characters.

This device performs both TRS (sync) detection and framing, data descrambling with the SMPTE-259M $X^9 + X^4 + 1$ algorithm, and NRZI-to-NRZ decoding. These functions operate at any character rate from 16– to 40 MHz. For those systems operating with non-SMPTE-259M compliant video streams (or for diagnostic purposes), the scrambler and NRZI decoding functions can be disabled.

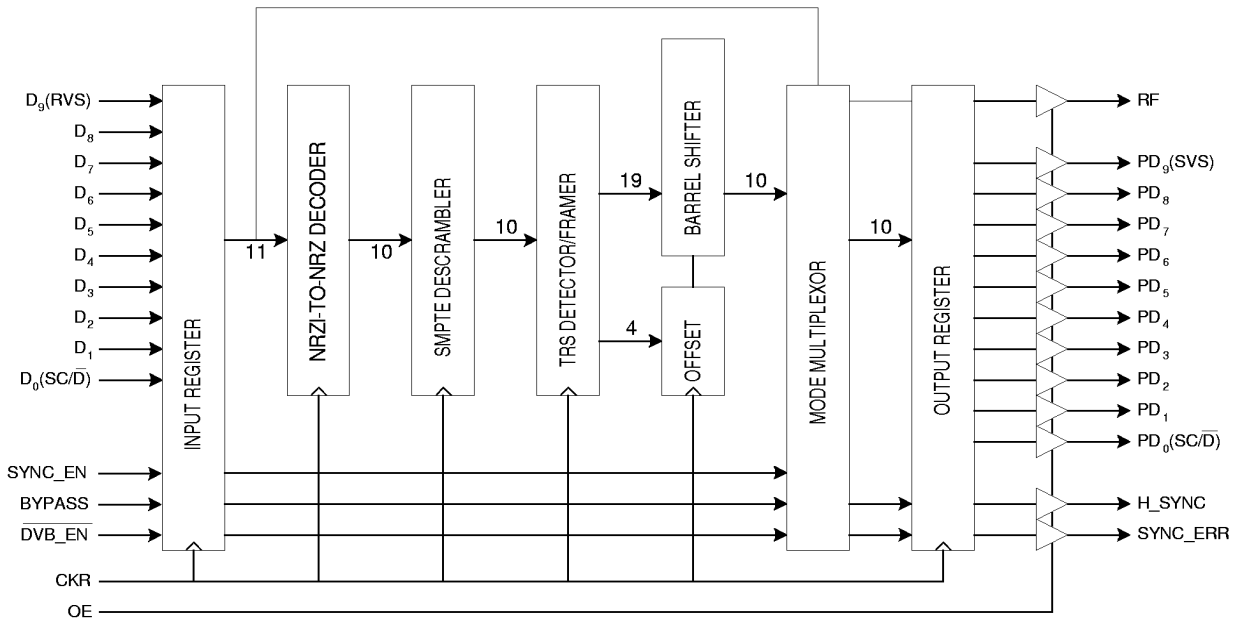
DVB-ASI Operation

The CY7C9335 also contains the necessary multiplexers, control inputs and outputs, to control a DVB-ASI compliant video stream. DVB-ASI operation is enabled through activation of a single input signal. This allows a single serial-to-parallel input port to support both SMPTE and DVB data streams under software or hardware control.

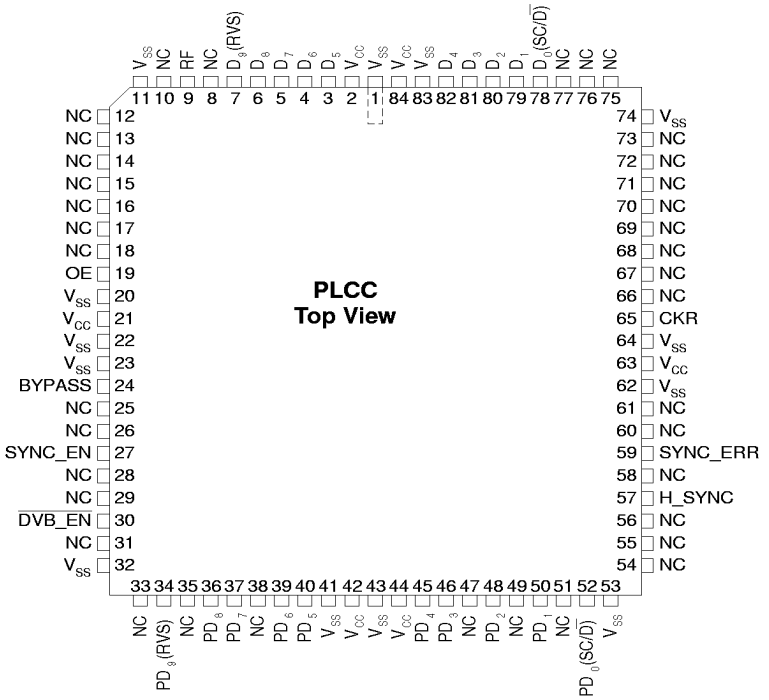
In DVB-ASI mode the CY7C9335 automatically enables both the 8B/10B decoder and multi-byte framer present in the CY7B933 receiver/deserializer. All error detection, fill, and command codes are detected and output by the CY7C9335.

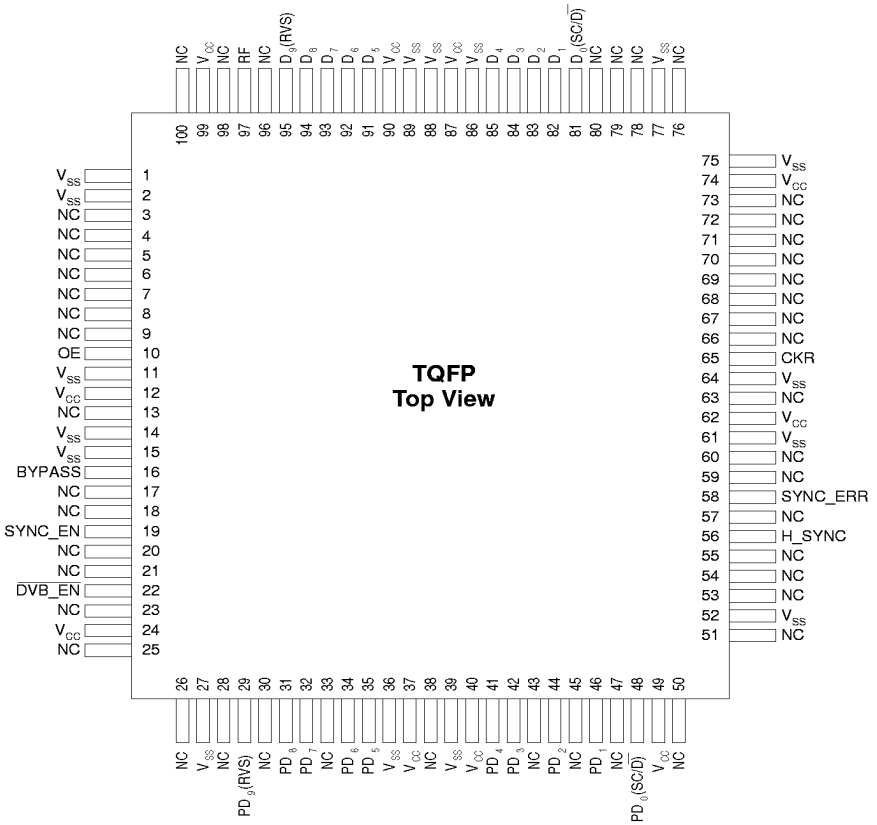
The CY7C9335 operates from a single +5V or –5V supply. It is available in either an 84-pin PLCC or 100-pin TQFP space saving packages.

Logic Block Diagram



Pin Configurations





Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–40°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State.....–0.5V to +7.0V

Output Current Into Outputs .....16 mA

DC Input Voltage .....–0.5V to +7.0V

Static Discharge Voltage.....>2001 V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%

Pin Descriptions

CY7C9335 SMPTE-259M Decoder

Name	I/O	Description
BYPASS	Input	Bypass SMPTE decoding. BYPASS is ignored if $\overline{DVB\_EN}$ is active (LOW). If BYPASS is HIGH at the rising edge of CKR (and $\overline{DVB\_EN}$ is HIGH), the data latched into the input register is routed around both the NRZI decoder and the SMPTE descrambler and presented to the output register. If BYPASS is LOW at the rising edge of the CKR clock (and $\overline{DVB\_EN}$ is HIGH), the data present in the input register is routed through the NRZI decoder and SMPTE scrambler.
RF	Output	Reframe. This output is driven HIGH one CKR clock cycle after $\overline{DVB\_EN}$ is recognized as being active (LOW), and returns LOW one CKR clock cycle after $\overline{DVB\_EN}$ is recognized as being disabled (HIGH).
H_SYNC	Output	Horizontal Sync. This output toggles once every time that the TRS field is recognized. It changes state one clock cycle prior to the first character of the TRS field (3FF in 10-bit hex) appearing at the PD_{0-9} outputs. This output also toggles to indicate detection of a TRS sequence, even when the TRS characters are at a different offset from the present offset and SYNC_EN is active (HIGH). This toggling action is disabled when $\overline{DVB\_EN}$ is active (LOW).
SYNC_EN	Input	Sync Filtering Enabled. This input controls the operation of the SMPTE framer. When this signal is active (HIGH) and a TRS sequence is detected, if the 10-bit character boundary is different from the previously received TRS, the H_SYNC output is toggled, but the character offset is not updated. If the immediately following TRS also has a different offset, the H_SYNC output is again toggled and the character offset is updated to match that of the detected TRS sequence. When this signal is inactive (LOW), the framer will update the character offset and toggle H_SYNC on every detected TRS sequence.
SYNC_ERR	Output	Sync Error. This output pulses HIGH for one CKR clock period to indicate the detection of a TRS sequence that is offset from its previous 10-bit character offset. This pulse starts at the same time as the H_SYNC signal toggles, but only occurs when SYNC_EN is active (HIGH) and the character offset is not updated.
PD_9(RVS)	Output	Parallel Data 9 or Received Violation Symbol. This is the MSB of the framed output data bus. It is latched in the output register at the rising edge of CKR. When $\overline{DVB\_EN}$ is active (LOW), this output indicates that the character present on PD_{8-0} identifies the type of error detected in the character stream. When $\overline{DVB\_EN}$ is disabled (HIGH), the character in the output register bits PD_{9-0} is a descrambled and framed character of the SMPTE data stream.
PD_{8-1}	Output	Parallel Data 8 through 1. The signals present at the PD_{8-1} outputs are latched in the output register at the rising edge of CKR. When $\overline{DVB\_EN}$ is disabled (HIGH), these signals are the middle eight bits of the descrambled and framed SMPTE 10-bit data character. When $\overline{DVB\_EN}$ is active (LOW), these signals are full DVB-ASI data bus.
PD_0(SC/$\overline{D}$)	Output	Parallel Data 0 or Special Code/Data Select. This is the LSB of the output data field. It is latched in the output register at the rising edge of CKR. When $\overline{DVB\_EN}$ is active (LOW), this output identifies that the character present in PD_{8-1} is either a command (HIGH) or data (LOW) character). When $\overline{DVB\_EN}$ is inactive (HIGH), this output data bit is LSB of the descrambled and framed SMPTE data character.
D_9(RVS)	Input	Input Bit 9. This is the MSB of the input register. It should be connected directly to the CY7B933 deserializer output signal RVS(Q_j).
D_{8-1}	Input	Input Bits 8 through 1. These signals should be connected directly to the CY7B933 deserializer output signals Q_{7-0} respectively.

Pin Descriptions (continued)

CY7C9335 SMPTE-259M Decoder

Name	I/O	Description
D_0(SC/$\overline{D}$)	Input	Input Bit 0. This is the LSB of the input register. It should be connected directly to the CY7B933 deserializer output signal SC/$\overline{D}$(Q_a).
$\overline{DVB\_EN}$	Input	DBV Mode Enable. This signal is sampled by the rising edge of the CKR clock. If $\overline{DVB\_EN}$ is active (LOW), the data present on the D_{0-9} inputs are latched and routed to the PD_{0-9} outputs.
CKR	Input	Recovered Clock Read. This clock controls all synchronous operations of the CY7C9335. It operates at the character rate which is equivalent to one tenth the deserialized bit-rate. This clock is driven directly by the CKR output of the CY7B933 deserializer.
OE	Input	Output Enable. When this signal is HIGH all outputs are driven to their normal logic levels. When LOW, all outputs are placed in a High-Z state.
V_{CC}		Power.
V_{SS}		Ground.

CY7C9335 Description

Input Register

The input register is clocked by the rising edge of CKR. This register captures the data present at the D_{0-9} inputs on every clock cycle. In addition to the data inputs, all control inputs except OE are also captured at each rising edge of CKR. This includes BYPASS, $\overline{DVB\_EN}$, and SYNC_EN.

NRZI-to-NRZ Decoder

The data in the input register is routed through an NRZI-to-NRZ decoder prior to being fed to the SMPTE descrambler. This removes the extra transitions added to the data stream by the NRZI encoder at the transmit end of the interface.

SMPTE Descrambler

Once the data has been converted back to NRZ, it is then routed through a linear feed-forward descrambler. It decodes the data present in the NRZ decode register using the $X^9 + X^4 + 1$ polynomial to remove the extra transitions added to the data stream at the transmit end of the interface.

TRS Framer

The TRS Framer is used to detect all 30-bit TRS sequences (3FF, 000, 000 in 10-bit hex) in the character stream. Anytime this sequence is detected, the H_SYNC output toggles.

This sequence is also used to frame the received characters so that the characters delivered to the output register are on their correct 10-bit boundaries. If SYNC_EN is disabled (LOW) and the TRS sequence is detected in the decoded data stream, the character offset register is set to match the offset of the TRS sequence, and both the TRS sequence and the following characters are output on their proper 10-bit boundaries.

If SYNC_EN is enabled, and a TRS sequence is detected whose character offset does not match that in the offset register, an internal flag is set but the offset register is not updated. On the next consecutive TRS sequence this flag is cleared and the offset register is updated.

DVB-ASI Operation

The CY7C9335 is designed to operate in both SMPTE-259M and DVB-ASI environments. When operated in SMPTE-only environments, the $\overline{DVB\_EN}$ inputs must be tied to V_{CC} or driven HIGH.

DVB-ASI operation is enabled by asserting $\overline{DVB\_EN}$ LOW. This signal is latched by the rising edge of the CKR clock. When the CY7C9335 is placed in DVB mode, the SMPTE and NRZI decoders are bypassed, and the data latched into the input register is routed directly to the output register.

Error Detected

Errors detected in the DVB-ASI data stream are indicated by the Q_9 bit being HIGH. The specific type of error is identified by the remaining Q_{8-0} bits in the output register.

Command Code Reception

The DVB-ASI interface does not normally transmit any command characters other than the K28.5 code that is used both for synchronization and as a fill character when data is not being transmitted. These K28.5 characters are normally received as C5.0 characters. If other command characters are also transmitted, these characters are identified by Q_0 being HIGH, and by the bits present on Q_{8-1}.

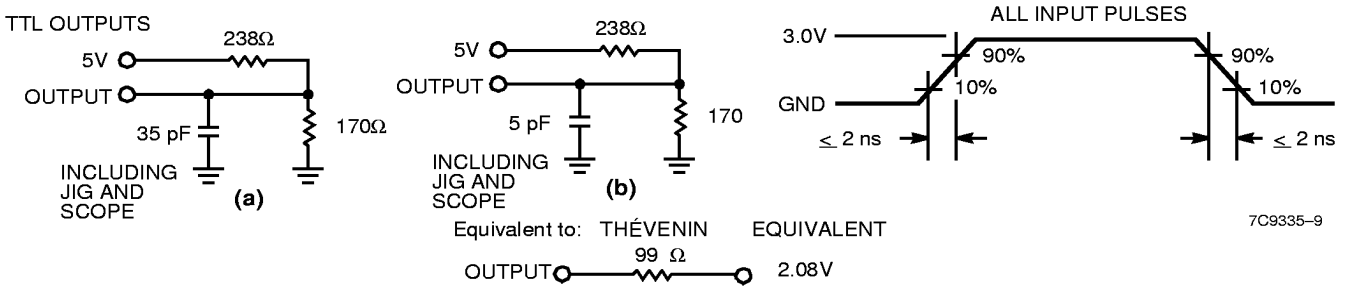
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA, V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Note 1	2.0	7.0	V
V_{IL}	Input LOW Voltage	Note 1	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–50	+50	µA
I_{OS}	Output Short Circuit Current[2, 3]	V_{CC} = Max., V_{OUT} = 0.5V	–30	–160	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance	f = 1 MHz, V_{CC} = 5.0V	12	pF

AC Test Loads and Waveforms



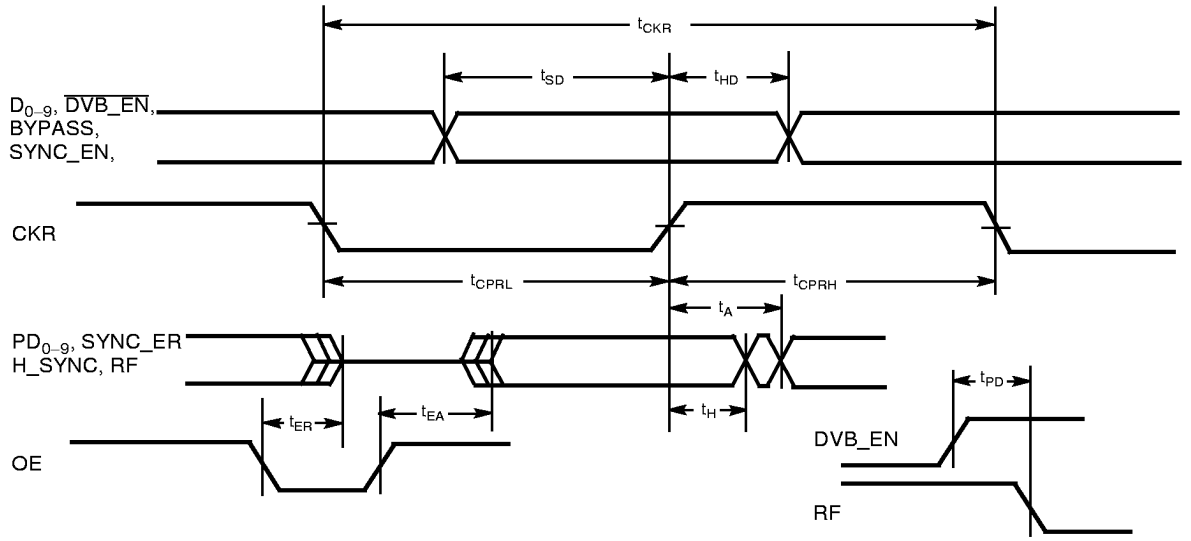
Switching Characteristics Over the Operating Range[4]

Parameter	Description	CY7C9335-27		CY7C9335-40		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output (DVB_EN to RF only)		20		15	ns
t_{SD}	Input Data Set-Up Time to CKR	10		8		ns
t_{HD}	Input Data Hold Time to CKR	0		0		ns
t_{CPRH}	CKR Pulse Width HIGH	6.5		6.5		ns
t_{CPRL}	CKR Pulse Width LOW	6.5		6.5		ns
t_{CKR}	Read Clock Cycle[5]	30	62.5	25	62.5	ns
t_A	Output Access Time from CKR		10		8	ns
t_H	Output Hold Time from CKR	4		3		ns
t_{EA}	Input to Output Enable		24		20	ns
t_{ER}	Input to Output Disable [6]		24		20	ns

Notes:

1. These are absolute values with respect to device ground. All overshoots with respect to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. VOUT = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may effect these parameters.
4. All AC parameters are with all outputs switching.
5. The clock period may be extended by up to 90% for a single clock cycle when framing occurs in DVB-ASI mode.
6. Test load (b) used for this parameter. Test load (a) used for all other AC parameters.

Switching Waveforms



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B9335-27JC	J83	84-pin Plastic Leaded Chip Carrioer	Commercial
CY7B9335-27AC	A100	100-pin Thin Quad Flat Pack	Commercial
CY7B9335-40JC	J83	84-pin Plastic Leaded Chip Carrioer	Commercial
CY7B9335-40AC	A100	100-pin Thin Quad Flat Pack	Commercial

Document #: 38-00572