PRELIMINARY

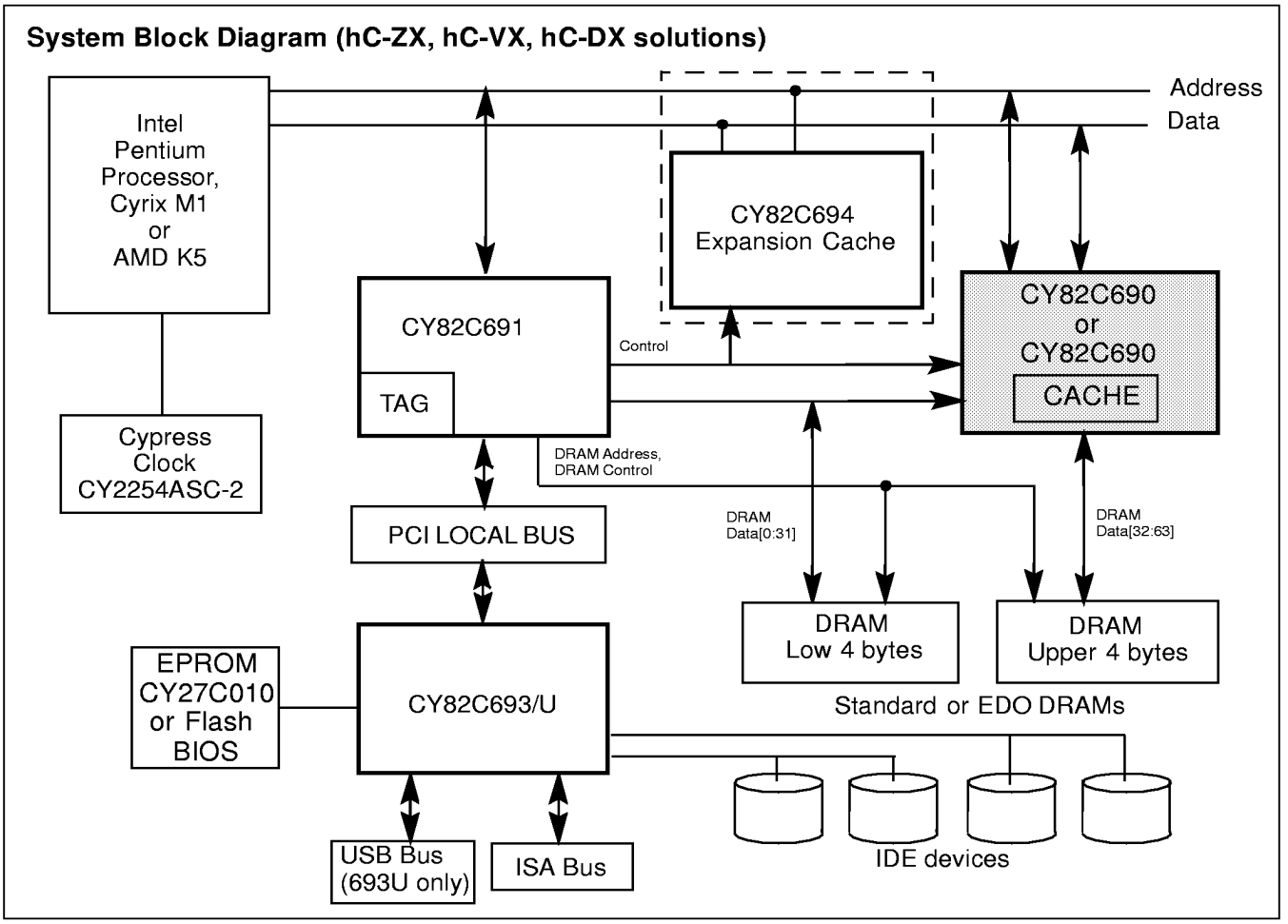
CY82C690

Pentium™ hyperCache™ Chipset Data-Path/Integrated Cache for hC-ZX Solution

Features

- Supports all 3.3V Pentium™-class processors, AMD K5, and Cyrix M1 CPUs
- Directly interfaces with CY82C691 and CY82C693 to provide high-performance three-chip Pentium Chipset system
- Provides 64-bit data path between CPU, PCI, and DRAM memory
- Direct interface with the processor and the CY82C691 PCI/Cache/Memory Controller
- 3.3V I/O CPU bus operation
- On-Chip 8-Deep FIFOs support Post-Writing/Pre-Reading PCI data
- Provides Data steering and Bus size conversion
- 4K by 64 (64-KB) Integrated Pipelined BSRAM
- Direct-mapped or two-way set associative L2 cache mapping configurations
- Two-bit wraparound counter supporting Intel Burst or Linear burst sequence
- Supports 3-1-1-1 Level 2 cache operation up to 66 MHz bus speed
- Fast Clock-to-Data (T_{CO})=8.5 ns
- Synchronous self-timed write to L2 cache BSRAM
- Direct interface with the processor and the CY82C691 PCI/Cache/Memory Controller
- Packaged in a 208-pin PQFP

System Block Diagram (hC-ZX, hC-VX, hC-DX solutions)



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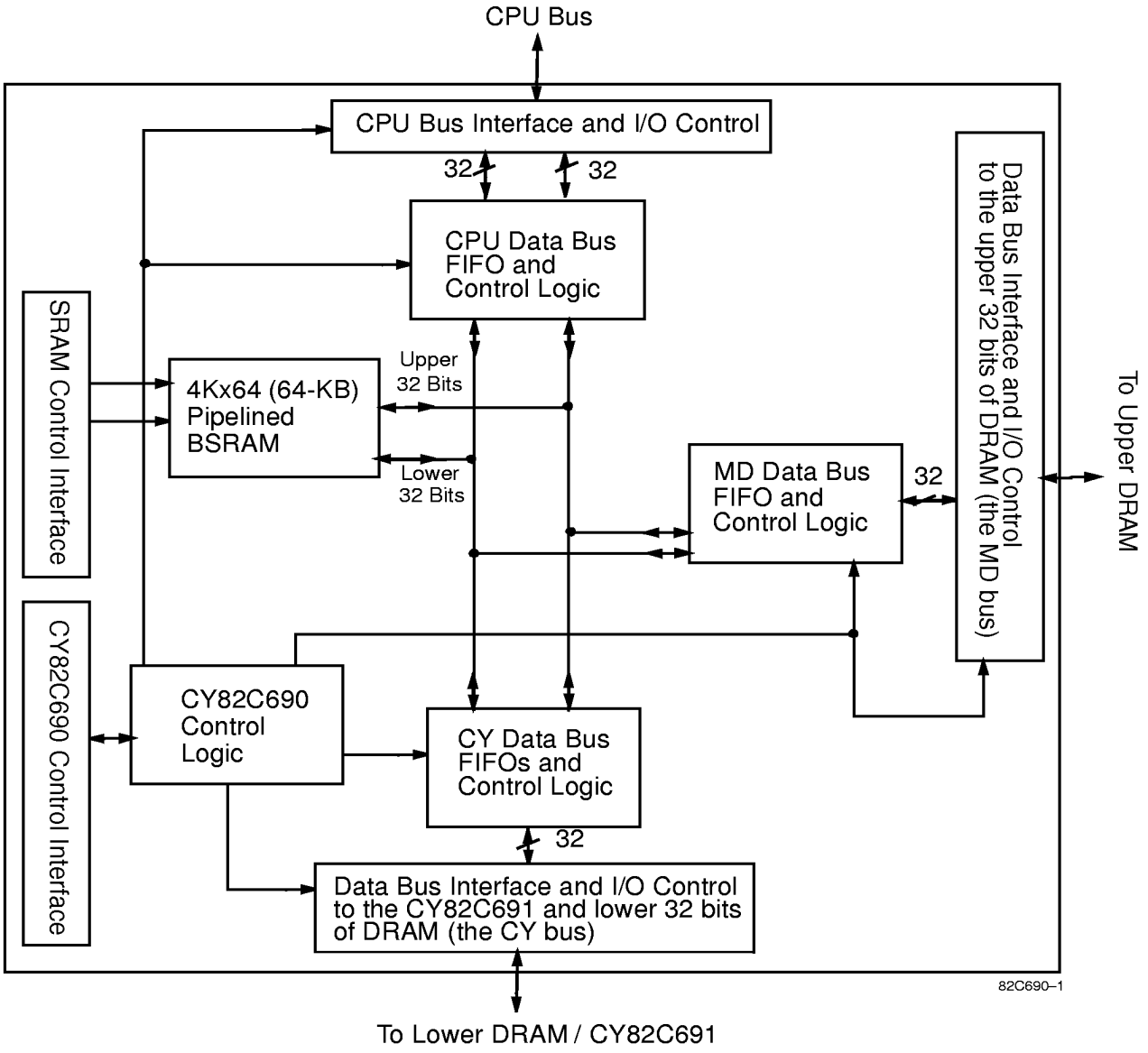
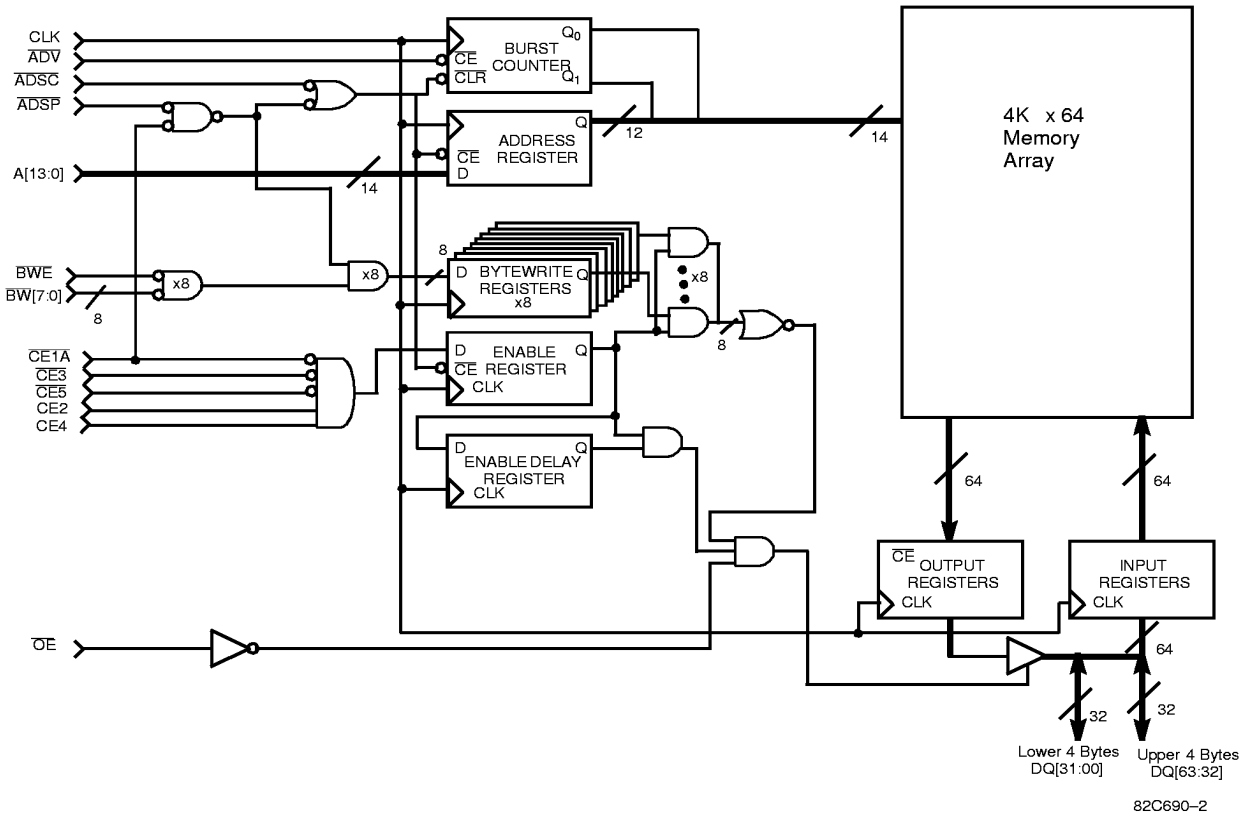
CY82C690 Block Diagram

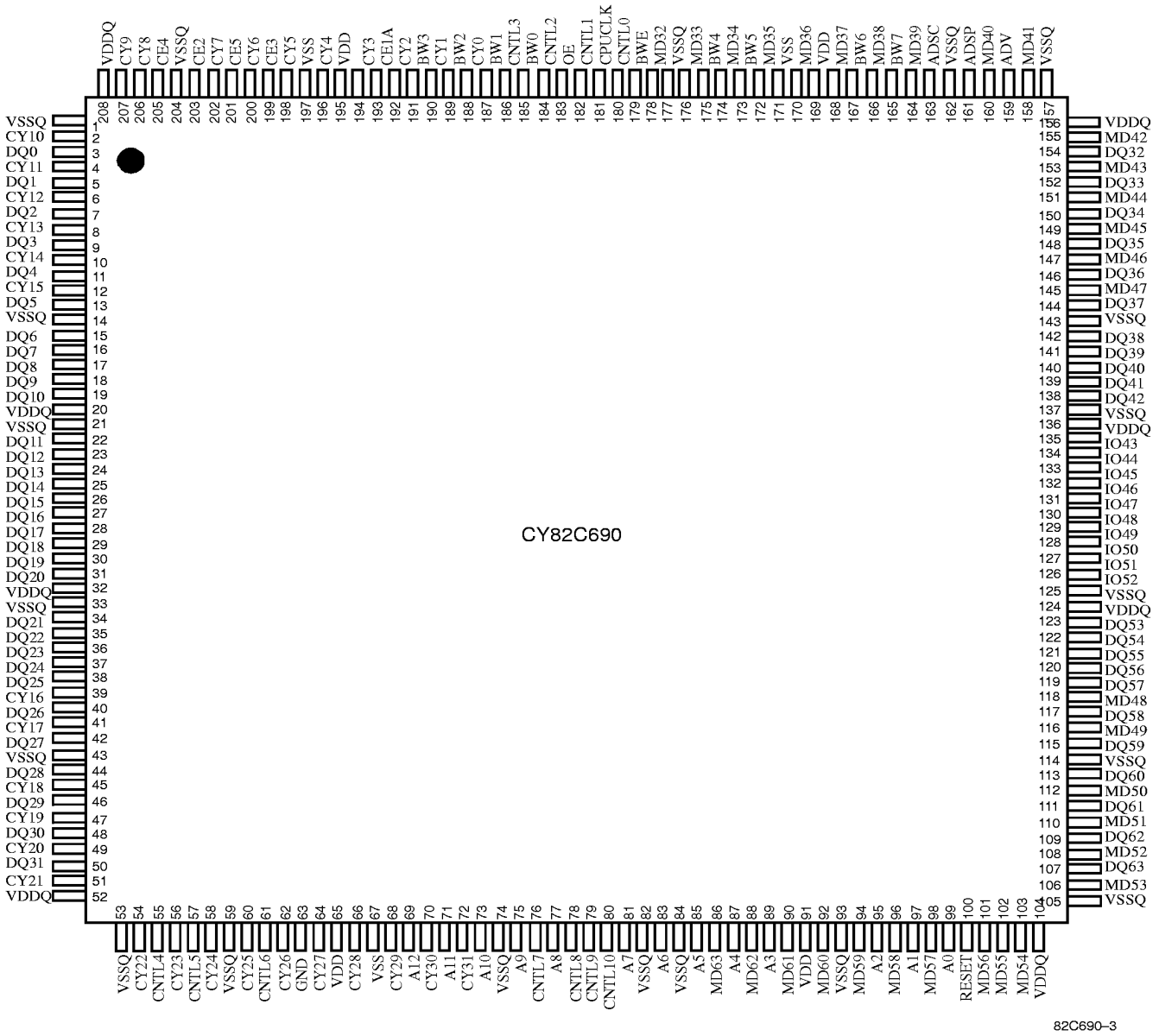


SRAM Section Logic Block Diagram



Pin Configuration

208-pin PQFP
Top View



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CY82C690 Pin Reference (In Numerical Order by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SSQ}	43	V_{SSQ}	85	A5.	127	DQ51	169	V_{DD}
2	CY10	44	DQ28	86	MD63	128	DQ50	170	MD36
3	DQ0	45	CY18	87	A4	129	DQ49	171	V_{SS}
4	CY11	46	DQ29	88	MD62	130	DQ48	172	MD35
5	DQ1	47	CY19	89	A3	131	DQ47	173	$\overline{BW5}$
6	CY12	48	DQ30	90	MD61	132	DQ46	174	MD34
7	DQ2	49	CY20	91	V_{DD}	133	DQ45	175	$\overline{BW4}$
8	CY13	50	DQ31	92	MD60	134	DQ44	176	MD33
9	DQ3	51	CY21	93	V_{SSQ}	135	DQ43	177	V_{SSQ}
10	CY14	52	V_{DDQ}	94	MD59	136	V_{DDQ}	178	MD32
11	DQ4	53	V_{SSQ}	95	A2	137	V_{SSQ}	179	$\overline{BWE}$
12	CY15	54	CY22	96	MD58	138	DQ42	180	CNTL0
13	DQ5	55	CNTL4	97	A1	139	DQ41	181	CPUCLK
14	V_{SSQ}	56	CY23	98	MD57	140	DQ40	182	CNTL1
15	DQ6	57	CNTL5	99	A0	141	DQ39	183	$\overline{OE}$
16	DQ7	58	CY24	100	$\overline{RESET}$	142	DQ38	184	CNTL2
17	DQ8	59	V_{SSQ}	101	MD56	143	V_{SSQ}	185	$\overline{BW0}$
18	DQ9	60	CY25	102	MD55	144	DQ37	186	CNTL3
19	DQ10	61	CNTL6	103	MD54	145	MD47	187	$\overline{BW1}$
20	V_{DDQ}	62	CY26	104	V_{DDQ}	146	DQ36	188	CY0
21	V_{SSQ}	63	GND	105	V_{SSQ}	147	MD46	189	$\overline{BW2}$
22	DQ11	64	CY27	106	MD53	148	DQ35	190	CY1
23	DQ12	65	V_{DD}	107	DQ63	149	MD45	191	$\overline{BW3}$
24	DQ13	66	CY28	108	MD52	150	DQ34	192	CY2
25	DQ14	67	VSS	109	DQ62	151	MD44	193	$\overline{CE1A}$
26	DQ15	68	CY29	110	MD51	152	DQ33	194	CY3
27	DQ16	69	A12	111	DQ61	153	MD43	195	V_{DD}
28	DQ17	70	CY30	112	MD50	154	DQ32	196	CY4
29	DQ18	71	A11	113	DQ60	155	MD42	197	VSS
30	DQ19	72	CY31	114	V_{SSQ}	156	V_{DDQ}	198	CY5
31	DQ20	73	A10	115	DQ59	157	V_{SSQ}	199	$\overline{CE3}$
32	V_{DDQ}	74	V_{SSQ}	116	MD49	158	MD41	200	CY6
33	V_{SSQ}	75	A9	117	DQ58	159	$\overline{ADV}$	201	$\overline{CE5}$
34	DQ21	76	CNTL7	118	MD48	160	MD40	202	CY7
35	DQ22	77	A8	119	DQ57	161	$\overline{ADSP}$	203	CE2
36	DQ23	78	CNTL8	120	DQ56	162	V_{SSQ}	204	V_{SSQ}
37	DQ24	79	CNTL9	121	DQ55	163	$\overline{ADSC}$	205	CE4
38	DQ25	80	CNTL10	122	DQ54	164	MD39	206	CY8
39	CY16	81	A7	123	DQ53	165	$\overline{BW7}$	207	CY9
40	DQ26	82	V_{SSQ}	124	V_{DDQ}	166	MD38	208	V_{DDQ}
41	CY17	83	A6	125	V_{SSQ}	167	$\overline{BW6}$		
42	DQ27	84	V_{SSQ}	126	DQ52	168	MD37		

Introduction

System Overview

The hyperCache™ family is a family of three chipsets created to provide flexible solutions for today's PC designs. The hC-ZX, hC-VX, hC-DX Chipsets provide all the functions necessary to implement a 3.3V Pentium-class processor based system with the USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), and the ISA (Industry Standard Architecture) buses. System designers can exploit the advantages of the USB and PCI buses while maintaining access to the large base of ISA cards in the marketplace.

The Cypress hyperCache family offers system designers several key advantages. With only three chips, a complete system can be implemented. Cache can be added up to 512 MB with additional CY82C694 devices in 128-KB increments All chipset solutions are pin-compatible and provide flexible upgrade paths through on-board or external cache modules. Six banks of page-mode or EDO DRAM further increase the system designer's options. The chipset also contains concurrent bus support, PCI enhanced IDE with CD-ROM support, integrated RTC, integrated peripheral control (Interrupts/ DMA), and integrated keyboard controller. This chipset is flexible enough to provide the system designer with many cost/performance/function options to provide an optimum solution for a given design.

CY82C690 Introduction

The CY82C690 is a 64-bit data path unit between the DRAM and CPU for the hC-VX an hC-DX chipset solutions. The CY82C690 serves two main functions: (1) Provides data steering to/from three different interfaces (CPU bus, the DRAM high or MD bus, and the DRAM low or CY bus), and (2) Provides 64 KB of Level 2 cache with an integrated synchronous pipelined BSRAM. With a clock-to-data valid time (TCO)=8.5 ns, 3-1-1-1 burst cycles are supported at bus frequencies up to 66 MHz.

The CY82C690 contains several sets of FIFOs that serve as Pre-Reading/Post-Writing buffers. These buffers are controlled by signals (Control[10:0]) coming from the CY82C691 System Controller. The Pre-Reading/Post-Writing feature enhances system performance by allowing concurrent transactions on the CPU, PCI, and DRAM buses.

The 3.3V CPU bus interface contains an 8-deep, 64-bit wide FIFO. This FIFO is logically broken into two 32-bit FIFOs in order to properly route data and accommodate for bus size conversions. All data coming from or going to the CPU data bus must pass through the CPU FIFO.

The DRAM interface is divided between the upper 32 bits and lower 32 bits of data. The upper 32 bits are transferred on the MD bus. The MD bus is a dedicated connection between the CY82C690 and the upper 32 bits of DRAM memory. The lower 32 bits of data are transferred on the CY bus. The CY bus also serves as the data path connecting the PCI bus (via the CY82C691) to the CPU.

The CY82C690 contains an integrated Level 2 cache configured as a 4Kx64 (64-KB) synchronous pipelined BSRAM. The BSRAM can be used as either a direct mapped or two-way set associative L2 cache. The BSRAM is controlled by dedicated control signals coming from the CY82C691 System Controller. The L2 cache can be expanded with additional CY82C694s (Cypress's 16Kx64 pipelined BSRAM) or additional discrete BSRAMs (synchronous or pipelined). Each bank must be comprised of the same type of BSRAM. L2 cache sizes of up to 512 MB are supported, using one or two banks.

Pre-Reading/Post-Writing

The CY82C690 supports Pre-Reading/Post-Writing operations through the use of on-chip 8-deep FIFOs that act as storage buffers. All Pre-Read and Post-Write operations are conducted to/from the on-chip FIFOs. Data is always stored in the FIFO closest to the target interface. By using these buffers in conjunction with on-chip control and routing logic, the CY82C690 is able to support concurrent transactions involving CPU, PCI, and DRAM memory transactions. All of the signals controlling the on-chip FIFOs are generated from the CY82C691 System Controller.

CPU Data Bus Interface

The CY82C690 interfaces to the CPU data bus through a 3.3V 64-bit interface. On-chip logic divides this interface into two 32-bit words in order to accommodate bus size conversions and concurrent transactions. Each 32-bit word passes through a 8-deep FIFO and three-state buffers.

DRAM Interface

The CY82C690 connects to DRAM memory through two separate 32-bit data interfaces, the CY and MD buses. The CY bus connects the lower 32-bits of data to both the DRAM memory and the CY82C691 System Controller. The CY bus interface contains two 32-bit-wide, 8-deep FIFOs in order to store Pre-Read/Post-Write data. The FIFO is controlled by Control[10:0] from the CY82C691 System Controller. Additionally, all CPU-to-PCI transactions are routed through the CY bus to the CY82C691 System Controller.

The upper 32 bits of DRAM data are transferred on the MD bus. The MD bus is a dedicated interface that connects the CY82C690 with the upper 32 bits of DRAM data. The MD bus interface contains 32-bit-wide 8-deep FIFOs that are used to store Pre-Read/Post-Write data destined for upper memory. FIFO control is conducted through Control[10:0].

Integrated Level 2 Cache

The CY82C690 contains an integrated Level 2 cache configured as a 4Kx64 (64-KB) synchronous pipelined Burst SRAM (BSRAM). The BSRAM operates as a separate device, independent from the other functional blocks of the CY82C690. The BSRAM can be used as either a direct mapped or two-way set associative 64-KB Level 2 cache. Level 2 cache expansion can be accomplished with either additional CY82C694s (up to a total of four for a 512-MB L2 cache), or additional dedicated BSRAMs (synchronous or pipelined). Each bank must be comprised of the same type of BSRAM. L2 cache sizes of up to 512 MB are supported, using one or two banks. If desired, the BSRAM inside the CY82C690 can also be disabled.

All synchronous inputs to the BSRAM pass through registers controlled by a positive edge triggered single clock (CLK). The synchronous inputs include all addresses, data inputs, write inputs ($\overline{BW}$[7:0], $\overline{BWE}$), $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, and chip enables ($\overline{CE1A}$, CE2, $\overline{CE3}$, CE4, $\overline{CE5}$).

All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock

rise (T_{CO}) is 8.5 ns. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY82C690 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Intel and AMD processors. The linear burst sequence is suited for processors such as the Cyrix M1. The burst order is user selectable, and is determined by writing to a specified register during power-up. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}0–7$) inputs. All writes are simplified with on-chip synchronous self-timed write circuitry.

Five synchronous chip selects ($\overline{CS1A}$, $\overline{CS3}$, $\overline{CS5}$, CS2, CS4) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CS1A}$, $\overline{CS3}$, $\overline{CS5}$, CS4, and CS2 are all asserted active, (3) either $\overline{BWE}$ is HIGH or $\overline{BW0}$-$\overline{BW7}$ are all HIGH. The address presented to the address inputs (A0–A12) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers of the SRAM section. At the rising edge of the next clock the data is driven onto the CPU data bus on D[63:00]. The requested data will be available on the CPU bus 8.5 ns after the clock rise. When the asynchronous Output Enable ($\overline{OE}$) is asserted LOW, the data outputs from the SRAM block are controlled by the Enable and Enable Delay Registers. During the first cycle of an initial read operation the outputs on the CPU bus remain in a three-state condition, regardless of the state of Output Enable ($\overline{OE}$). This feature is required in order to support pipelining without creating contention on the data bus when multiple banks of cache are used. Consecutive single read cycles are supported.

Single Write Accesses Initiated by $\overline{ADSP}$

$\overline{ADSP}$-triggered accesses are initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CS1A}$, $\overline{CS3}$, $\overline{CS5}$, CS4, and CS2 are all asserted active. The address presented to A0-A12 is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{BW0}$-$\overline{BW7}$, $\overline{BWE}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If the write inputs ($\overline{BWE}$ with one or more of the $\overline{BW}$[7:0]) are asserted LOW on the second clock rise, the data presented to the D0–D63 inputs is written into the corresponding address location in the RAM core. The CY82C690 provides byte write capability. Asserting the $\overline{BWE}$ signal together with the appropriate Byte Write signal (one or more of $\overline{BW}$[7:0]) will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has also been provided to simplify the write operations.

Since the CY82C690 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the D0–D63 inputs. Doing so will three-state the output drivers. As a safety precaution, D0-D63 are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses in Pipelined mode are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) $\overline{CS1A}$, $\overline{CS5}$, $\overline{CS3}$, CS4, and CS2 are all asserted active, and (4) the appropriate write inputs ($\overline{BWE}$, $\overline{BW0}$–$\overline{BW7}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented to A0–A12 is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. The data presented to the D0–D63 is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has also been provided to simplify the write operations.

Since the CY82C690 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the D0–D63 inputs. Doing so will three-state the output drivers. As a safety precaution, D0–D63 are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY82C690 provides a two-bit wraparound counter, fed by A0 and A1, that implement either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence, such as the Cyrix M1. The burst order is determined during boot-up by writing to a specific configuration register.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Intel Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Cycle Descriptions

Next Cycle	Add. Used	CS2	CS4	$\overline{CS3}$	$\overline{CS5}$	$\overline{CS1A}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Writes
Unselected	none	X	X	X	X	1	X	0	X	X	Hi-Z	X
Unselected	none	0	X	X	X	0	0	X	X	X	Hi-Z	X
Unselected	none	X	0	X	X	0	0	X	X	X	Hi-Z	X
Unselected	none	X	X	1	X	0	0	X	X	X	Hi-Z	X
Unselected	none	X	X	X	1	0	0	X	X	X	Hi-Z	X
Unselected	none	0	X	X	X	0	1	0	X	X	Hi-Z	X
Unselected	none	X	0	X	X	0	1	0	X	X	Hi-Z	X
Unselected	none	X	X	1	X	0	1	0	X	X	Hi-Z	X
Unselected	none	X	X	X	1	0	1	0	X	X	Hi-Z	X
Begin Read	External	1	1	0	0	0	0	X	X	X	Hi-Z	X
Begin Read	External	1	1	0	0	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	X	X	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	X	X	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	X	X	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	X	X	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	X	X	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	X	X	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	X	X	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	X	X	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	X	X	X	X	X	1	1	1	X	Hi-Z	Write[1]
Begin Write	Current	X	X	X	X	1	X	1	1	X	Hi-Z	Write[1]
Begin Write	External	1	1	0	0	0	1	0	X	X	Hi-Z	Write[1]
Continue Write	Next	X	X	X	X	X	1	1	0	X	Hi-Z	Write[1]
Continue Write	Next	X	X	X	X	1	X	1	0	X	Hi-Z	Write[1]
Suspend Write	Current	X	X	X	X	X	1	1	1	X	Hi-Z	Write[1]
Suspend Write	Current	X	X	X	X	1	X	1	1	X	Hi-Z	Write[1]

X=Don't Care, 1=Logic HIGH, 0=Logic LOW.

Note:

1. Writes defined by $\overline{BWE}$, $\overline{BW}$[7:0],see Write Cycle Description table.

Write Cycle Descriptions

Function[2]	$\overline{BWE}$	$\overline{BW7}$	$\overline{BW6}$	$\overline{BW5}$	$\overline{BW4}$	$\overline{BW3}$	$\overline{BW2}$	$\overline{BW1}$	$\overline{BW0}$
Read	1	X	X	X	X	X	X	X	X
Read	0	1	1	1	1	1	1	1	1
Write All Byte	X	X	X	X	X	X	X	X	X
Write Byte 0 - DQ[7:0]	0	1	1	1	1	1	1	1	0
Write Byte 1 - DQ[15:8]	0	1	1	1	1	1	1	0	1
Write Byte 2 - DQ[23:16]	0	1	1	1	1	1	0	1	1
Write Byte 3 - DQ[31:24]	0	1	1	1	1	0	1	1	1
Write Byte 4 - DQ[39:32]	0	1	1	1	0	1	1	1	1
Write Byte 5 - DQ[47:40]	0	1	1	0	1	1	1	1	1
Write Byte 6 - DQ[55:48]	0	1	0	1	1	1	1	1	1
Write Byte 7 - DQ[63:56]	0	0	1	1	1	1	1	1	1
Write Byte 1, 0	0	1	1	1	1	1	1	0	0
Write Byte 2, 1	0	1	1	1	1	1	0	0	1
Write Byte 2, 0	0	1	1	1	1	1	0	1	0
Write Byte 2, 1, 0	0	1	1	1	1	1	0	0	0
Write Byte 3, 0	0	1	1	1	1	0	1	1	0
Write Byte 3, 1	0	1	1	1	1	0	1	0	1
Write Byte 3, 1, 0	0	1	1	1	1	0	1	0	0
Write Byte 3, 2	0	1	1	1	1	0	0	1	1
Write Byte 3, 2, 0	0	1	1	1	1	0	0	1	0
Write Byte 3, 2	0	1	1	1	1	0	0	1	1
The remainder follows the same pattern as above.									

X=Don't Care, 1=Logic HIGH, 0=Logic LOW.

Note:

2. The SRAM always starts a Read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{BWE}$, $\overline{BW}$[7:0].

Pin Descriptions

Name	I/O	Pin Number	Description
$\overline{\text{RESET}}$	I	100	This is the RESET input signal from the CY82C693. It puts the CY82C690 into a known state and invalidates all write-buffer entries.
CPUCLK	I	181	The CPU clock input. This runs synchronous to the CPU's external clock.
D[63:00]	I/O	107, 109. 111, 113, 115, 117, 119–123, 126–135, 138–142, 144, 146, 148, 150, 152, 154, 50, 48, 46, 44, 42, 40, 38–34, 31–22, 19-15, 13, 11, 9, 7, 5, 3	The 64-bit CPU data bus interface. These are 3.3V signals.
CY[31:00]	I/O	72, 70, 68, 66,64, 62, 60, 58, 56, 54, 51, 49, 47, 45, 41, 39, 12, 10, 8, 6, 4, 2, 207, 206, 202, 200, 198, 196, 194, 192, 190, 188	The CY bus interfaces to the lower 32 DRAM data bits. It also is the data path to pass data to/from the CY82C691 for routing to the PCI bus.
MD[63:31]	I/O	86, 88, 90, 92, 94, 96, 98, 101, 102, 103, 106, 108, 110, 112, 116, 118, 145, 147, 149, 151, 153, 155, 158, 160, 164, 166, 168, 170, 172, 174, 176, 178	The MD bus interfaces to the upper 32 DRAM data bits.
A[12:0]	I	69, 71, 73, 75, 77, 81, 83, 85, 87, 89, 95, 97, 99	Address inputs to the cache BSRAM, sampled on the rising edge of the clock.
$\overline{\text{BWE}}$	I	179	Byte Write Enable input. Used in conjunction with $\overline{\text{BW}}$[7:0] to conduct byte write operations. $\overline{\text{BW}}$[7:0] are qualified with $\overline{\text{BWE}}$.
$\overline{\text{BW}}$[7:0]	I	165, 167, 173, 175, 191, 189, 187, 185	Byte write inputs to the cache BSRAM, synchronous, sampled on the rising edge of the clock.
$\overline{\text{CE1A}}$	I	193	Chip enable and $\overline{\text{ADSP}}$ mask.
CE2, $\overline{\text{CE3}}$, CE4, $\overline{\text{CE5}}$	I	203, 199, 205, 201	Expansion decode inputs for L2 cache expansion. Used to establish and decode the expansion position of each CY82C690.
$\overline{\text{OE}}$	I	183	Asynchronous Output Enable. Active LOW, used in conjunction with Control[11:00] to control the three-state buffers onto the CPU bus.
$\overline{\text{ADV}}$	I	159	Advance input signal to the BSRAM section only, active LOW, sampled on the rising edge of the clock. When detected active it will cause the on-chip burst counter to increment to the next address in the burst sequence. This signal is ignored if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is asserted.

Pin Descriptions (continued)

Name	I/O	Pin Number	Description
$\overline{ADSC}$	I	163	Address input strobe from the controller, active LOW, sampled on the rising edge of the clock. When asserted, the address inputs are captured in the address register. A0 and A1 are also loaded into the two-bit burst counter. $\overline{ADSC}$ is ignored when asserted with $\overline{ADSP}$.
$\overline{ADSP}$	I	161	Address input strobe from the processor, active LOW, sampled on the rising edge of the clock. When asserted, the address inputs are captured in the address register. A0 and A1 are also loaded into the two-bit burst counter.
CONTROL [10:00]	I	80–78, 76, 61, 57, 55, 186, 184, 182, 180	Control inputs. These are the inter-chip communication signals between the CY82C691 and CY82C690. These signals are used to control the FIFOs, logic, three-stating, and data steering inside the CY82C690. CNTL[3:0] pass state information from the 82C691 to the 82C692. CNTL4 Primary Latch signal ($\overline{PRILAT}$) CNTL5 Secondary Latch signal ($\overline{SECLAT}$) CNTL6 Advance CPU FIFO ($\overline{ADVCPUF}$) CNTL7 Advance MD FIFO ($\overline{ADVMDF}$) CNTL8 Advance CY FIFO ($\overline{ADVCYF}$) CNTL9 SELDHDL CNTL10 SELCYDL
V_{DDQ}	Supply	20, 32, 52, 104, 124, 136, 156, 208	3.3V power supply for the I/Os of the to the CY82C690.
V_{DD}	Supply	65, 91, 169, 195	5V power supply to the core of the CY82C690.
V_{SSQ}	GND	1, 14, 21, 33, 43, 53, 59, 74, 82, 84, 93, 105, 114, 125, 137, 143, 157, 162, 177, 204	Ground for the I/Os of the CY82C690.
V_{SS}	GND	67, 171, 197	Ground for the core of the CY82C690.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[3] .....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage[3].....–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[4]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	5V ± 5%	3.3V ± 0.3V

Notes:

3. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
4. T_A is the "instant on" case temperature.

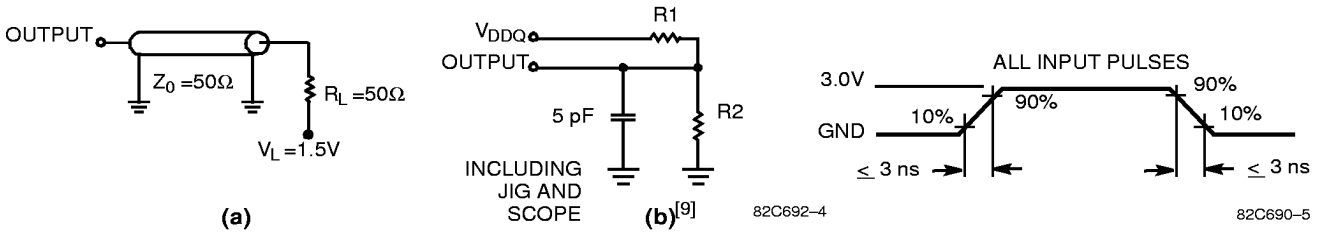
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH}=–4.0 mA		2.4	V_{DDQ}	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL}=8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD}+0.3V	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DD}		–1	1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DD}, Output Disabled		–5	5	µA
I_{OS}	Output Short Circuit Current[5]	V_{DD}=Max., V_{OUT}=GND			–300	mA
I_{CC}	V_{DD} Operating Supply Current	V_{DD}=Max., Iout=0mA, f=f_{MAX} =1/t_{CYC}	Com'l		TBD	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, $\overline{CS}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f=f_{MAX}[7]	Com'l		TBD	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, $\overline{CS}$ ≥ V_{DD} – 0.3V, V_{IN} ≥ V_{DD} – 0.3V or V_{IN} ≤ 0.3V, f=0[6,7]	Com'l		TBD	mA

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	4.5	pF
C_{IN}: Other Inputs			5	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Notes:

5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. Inputs are disabled, clock is allowed to run at speed.
7. $\overline{CS}$ LOW signifies all chip selects active during clock rise.
8. Tested initially and after any design or process changes that may affect these parameters.
9. Resistor values for V_{DDQ}=3.3V are R1=317Ω and R2=348Ω.

Switching Characteristics Over the Operating Range[10,11]

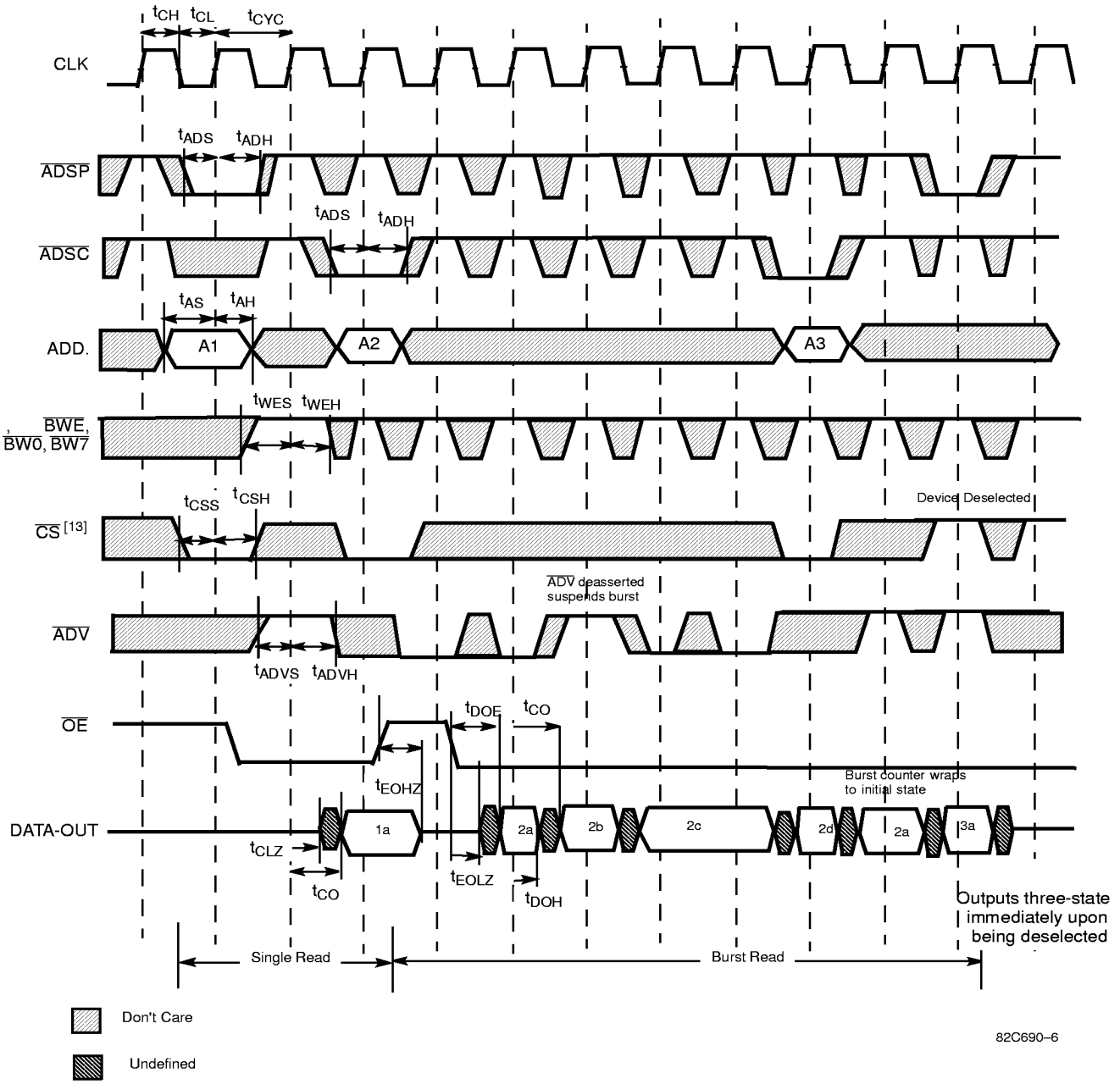
Parameter	Description	-8		Unit
		Min.	Max.	
t_{CYC}	Clock Cycle Time	15		ns
t_{CH}	Clock HIGH	6		ns
t_{CL}	Clock LOW	6		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		ns
t_{CO}	Data Output Valid After CLK Rise		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{BW}$[7:0] Set-Up Before CLK Rise	2.5		ns
t_{WEH}	$\overline{BWE}$, $\overline{BW}$[7:0] Hold After CLK Rise	0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		ns
t_{CHZ}	Clock to High-Z[11]	2	6	ns
t_{CLZ}	Clock to High-Z[11]	0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[11,12]	2	6	ns
t_{EOLZ}	$\overline{OE}$ HIGH to Output Low-Z[11]	0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[11,12]		6	ns

Notes:

10. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
11. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
12. At any given voltage and temperature, t_{EOHZ} min. is less than t_{EOV} min.

Switching Waveforms

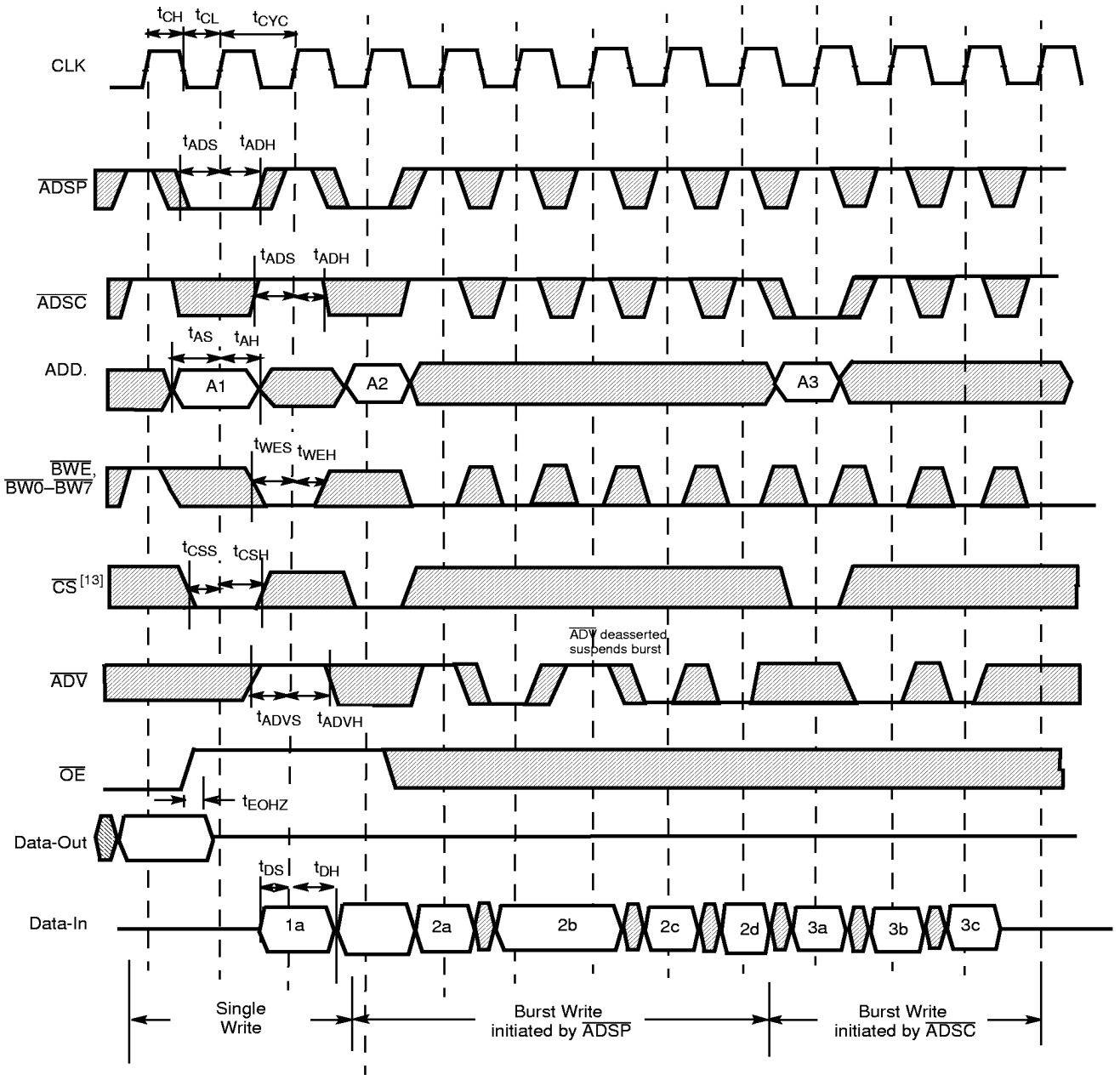
Read Timing



Note:
13. $\overline{CS}$ signifies that all chip selects ($\overline{CS1}$, $\overline{CS3}$, $\overline{CS5}$, CS2, and CS4) are all asserted active.

Switching Waveforms (continued)

Write Timing



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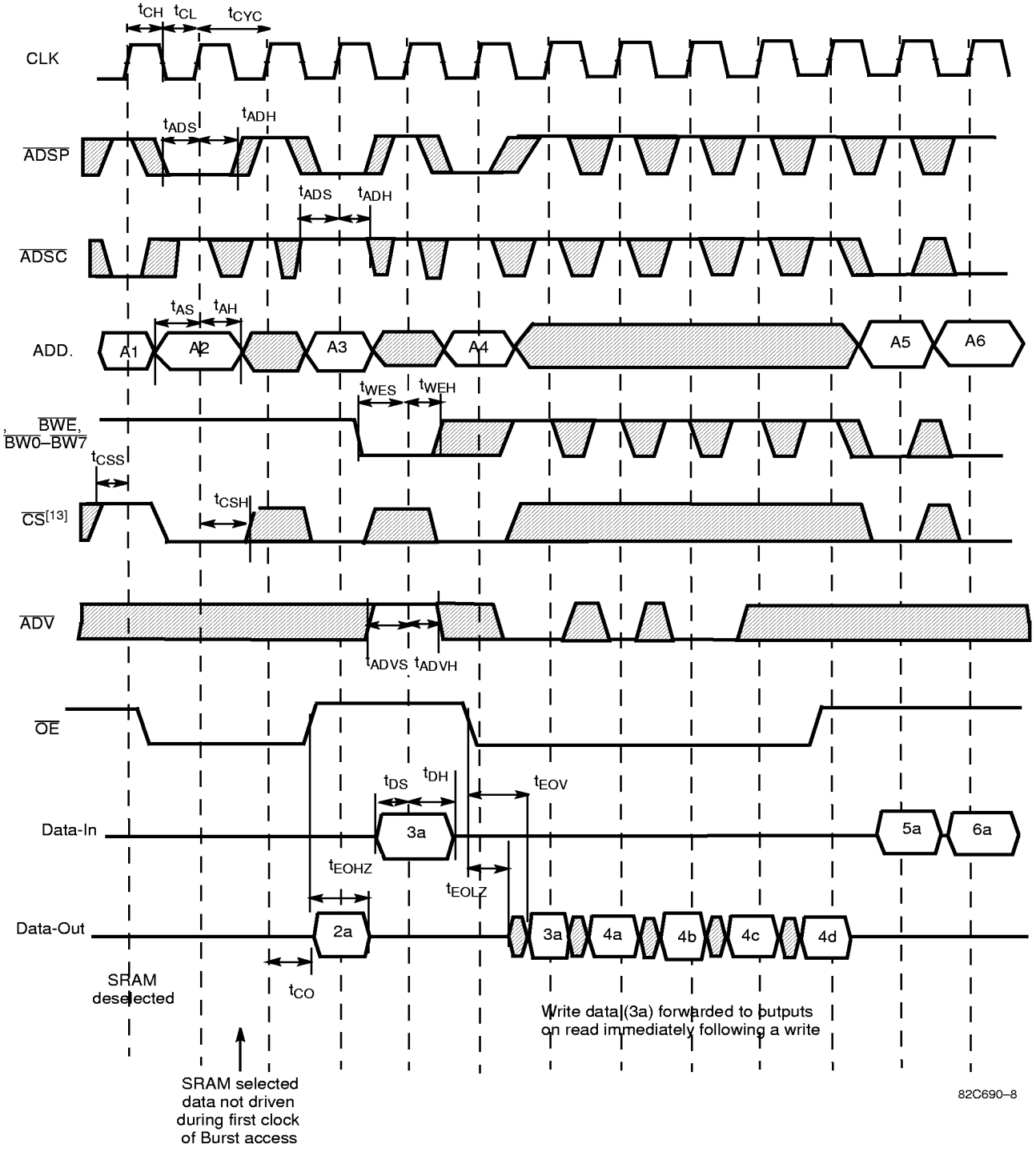
Switching Waveforms (continued)

Read/Write Timing



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY82C690-NC	N208	208-Lead Plastic Quad Flat Pack	Commercial

Document #: 38-00525-B

Package Diagram

208-Lead Plastic Quad Flatpack N208