T-42-11-09

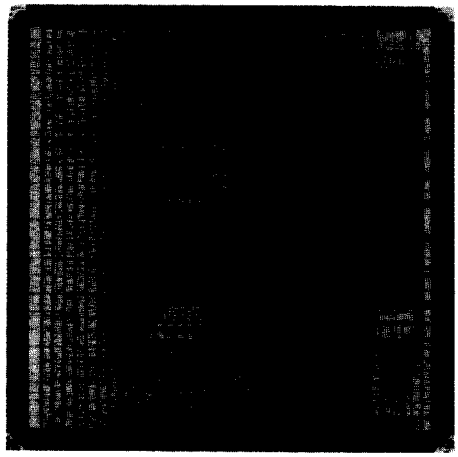
LEA100K Embedded Array™ Series

Description

The LEA100K Embedded Array™ Series is an HCMOS ASIC product which combines the benefits of cell-based and array-based ASICs. Design-specific, user-defined, semicustom, standard cell format embeddable cores offer high density and performance rivaling full custom design methodologies. Memory, microprocessors, megacells and any user-defined semicustom cores may be placed in any location on the user-defined masterslice. The remaining area is filled with potentially active transistors using LSI Logic's Channel-Free™ architecture.

The LEA100K series is manufactured using 0.7-micron channel length silicon gate HCMOS technology. This technology provides the advantages of ECL speeds with the lower power consumption and the higher noise margin characteristics of CMOS technology. With the added capability to incorporate very high density cell-based memory blocks, LEA100K Embedded Arrays offer an effective, high performance, high density design capability to implement virtually any digital logic design.

The LEA100K Embedded Array series offers the very high density and high performance of a cell-based ASIC design, with gate array turnaround time.



LEA100K Embedded Array Series Device

Features

- Silicon gate 0.7-micron channel length (1.0-micron gate length) HCMOS technology
- LCA100K Compacted Array Plus™ series turnaround time
- LCB007 Series of cell-based ASIC density and performance
- Up to 150,000 Equivalent Gate Capacity
- Up to 422 Signal I/O
- High density memory blocks:
  - High Speed Static RAM up to 144K bits
  - Up to five ports available
  - Contact Programmable ROM up to 1M bits
- Megafunctions (soft-coded LSI and MSI building blocks) including:
  - RISC Microprocessors and Floating Point Controllers
  - Motorola, Intel and AMD Peripherals
  - Communication Controllers
  - Generic Adders, Multipliers, MACs and CAMs
  - Barrel Shifters, FIFOs, LIFOs and ALUs
  - All megafunctions may be converted into megacells (hard-coded large building blocks)
- Extensive Macro Libraries
- Hierarchical functional placement
- Clock driver distribution methodology
- Full netlist compatibility with all other LSI Logic ASIC products
- Full military capability
- Fully supported by LSI Logic's Modular Design Environment™ software

October 1989 Order Number LEA100K

Architecture

Historically, gate arrays have offered the fastest turnaround times, both in the initial prototype and for any design revisions or variations. Thus, gate arrays offered the quickest time to market while minimizing delays from design modifications. Now, with the LEA100K, this flexibility and reduced risk is offered in conjunction with the performance and density associated with more customized cell-based ASIC designs.

The base wafer is customized with required RAM, ROM, microprocessor cores, megacells or any customer-defined semicustom cores. The base wafer is manufactured after the placement of embedded blocks is verified. Once the entire design is finalized, the base wafer is metalized to connect the random logic portion. Effectively, the critical turnaround time for the LEA100K design completion is the same as for the LCA100K Compacted Array Plus series.

Use of the Compacted Array Plus macrocell library for the gate array portion of the chip, and the availability of compatible cells in the LCB007 cell-based series allows for easy migration from earlier LSI Logic technologies. For example, existing multichip customer systems may be upgraded to a one-chip solution with on-chip memory.

Within the same design group or company, there may be many applications requiring heavy memory use or other cell-based embeddable cores. With proper system partitioning, the same user-defined base wafer can be used for many different applications.

For example, a customized base wafer could be used to produce a two-way set-associative cache, with four optimally placed, high performance embedded RAM cores, or, with a change in the random logic, to produce an equally high performance four-way set-associative cache. One particular design done includes a 2K x 32 high density RAM, 1K x 64 ROM, 64 x 64 3-port and 64 x 72 2-port RAMs, along with 10,000 used gates on a die of less than a centimeter on a side.

Customers may design their own microprocessor engines, with RAM and ROM on-chip. With a change in the ROM code, this same wafer can offer another state-of-the-art microprocessor engine. An example of this is embedding the 2901 bit-slice microprocessor with a sequencer. Two versions of the microcode can be combined with random logic (requiring different metalization of the same base wafer) to produce two different products.

Other potential applications include:

- DSP products may be built using hard macros and embedded memory on a masterslice
- LSI Logic's UART embedded on a core may be hooked up to many different types of peripherals with varying interfaces defined with random logic
- A RISC microprocessor core may be embedded on a masterslice, along with 144K bits of high density SRAM and over 40,000 used gates of random logic
- 1M ROM and over 45K used gates of random logic may be combined on one chip
- A SCSI controller embedded in a base wafer may be used for applications such as optical ROM disks, disk drives and mass storage devices, all using the same custom-designed base wafer.

LSI Logic's extensive library of soft- and hard-coded megacells and megafunctions, software tools including Memcomp, ChipSizer™, and Logic Block Synthesizer™, combined with developments in microprocessor, DSP and memory products provide an unlimited variety of design possibilities with state-of-the-art gate array and cell-based ASIC features.

Memory Capability

RAM and ROM blocks can be custom compiled to meet a wide variety of requirements. Many pre-built memory blocks of popular configurations are readily available. Specialized memories such as first-in, first-out (FIFOs), last-in, first-out (LIFOs), and content addressable memories (CAMs) are also available.

	RAM	ROM
LCA100K	48K	256K
LEA100K	144K	1M
LCB007	144K	1M

Software Support

LEA100K Embedded Array ASICs are fully supported by LSI Logic's Modular Design Environment software. The Silicon Integrator™ toolset creates a design environment in which complex gate array and cell-based ASICs can be designed and analyzed. Developed specifically for LSI Logic's manufacturing processes, LSI's Silicon Integrator is correlated to actual silicon performance, which facilitates the capability to create designs guaranteed to work to specifications the first time.

Software Support (Continued)

Memory Compiler

LSI Logic's Memcomp software allows ASIC system designers to automatically generate memory megacells such as single and multiport RAMs and ROMs. Use of this compiler decreases the time to produce memory megacells by several orders of magnitude. The memory megacells generated are optimized for both speed and area. Both data files for accurate timing simulation and for physical layout design are automatically generated. One-, two-, three-, and five-port RAMs and ROMs and high density single- and dual-port RAMs may also be compiled.

ASIC Systems Planning and Analysis

LSI Logic's ChipSizer software offers system designers an environment in which various alternatives may be evaluated to determine what system functions are ideal for ASIC implementation, what technology and accompanying die size will be produced, and package requirements based on both die size and pin requirements. ChipSizer allows ASIC designers to quickly perform "what if" type analysis to determine various alternatives of system partitioning. Accuracy of die-size estimation improves with design details. The user specifies system components such as logic blocks, memories, I/Os and other elements via a user-friendly, interactive graphic interface. The program displays the area allocation diagram and pad locations of various components of the system. It allows the designer to optimize die size by moving or rotating megacells and memory.

Logic Block Synthesizer

LSI Logic's Logic Block Synthesizer automates the design, verification and documentation of common logic functions. This logic design tool automatically creates user-specified logic functions which are "right by construction". Adders, counters, muxes, incrementer/decrementers, decoders, shift-registers and fallthru FIFOs specifications are entered with the easy-to-use, menu driven user interface. The circuits generated are optimized for speed or for area (gate count). LSI Logic's Logic Block Synthesizer tool greatly enhances designer productivity during the logic design phase of an ASIC design.

Packaging

LSI Logic ASIC devices can be packaged in a variety of plastic and ceramic dual in-line packages, leadless and leaded chip carriers, and pin grid arrays. Ceramic packages are available for the full military temperature range. Table 1 shows the package styles and pin counts available.

Table 1. Package Selector Guide for the LEA100K Embedded Array Series

Type	No. Pins - Ceramic	No. Pins - Plastic
Dual In-line Packages	14, 16, 18, 20, 22, 24, 28, 40, 48	14, 16, 18, 20, 22, 24, 28, 40, 48
Leaded Chip Carriers	44, 48, 52, 64, 68, 84, 100, 132, 144, 196, 224, 256, 340	28, 44, 68, 84
Leadless Chip Carriers	20, 28, 44, 68, 84	N/A
Pin Grid Array (Cavity Up)	64, 68, 84, 100, 120, 132, 144, 180, 224	68, 84, 100, 120, 144, 180, 224
Pin Grid Array (Cavity Down)	95, 132, 155, 223, 299, 391	N/A
Plastic Quad Flat pack	N/A	44, 64, 80, 100, 120, 160, 184, 208
Tape Quad Flat pack (TQFP)	N/A	164, 196, 224, 260, 300, 388, 444, 524

Overview of How to Do an ASIC Design

To implement an ASIC design, the following sequences of general steps are taken:

1. Partition the complete system into LSI Logic building blocks. An effort should be made to minimize the I/O count when partitioning the circuit. The user can describe his logic using LSI Logic's macrofunction/macrocell libraries of 7400/4000 series functions. The use of hierarchical design techniques allows netlist descriptions at these various levels. Ultimately, when the logic is compiled, it is "flattened" into macrocells. It is advisable to structure the complete schematic as a set of functional sub-systems such as a 16-bit ALU, a data receiver, a programmable timer, register file, or metal megacells and megafunctions, to allow comprehensible and easy hierarchical simulation.

In addition to the usual partitioning concerns, it may be possible to partition the complete system so that the same user-defined masterslice may be used multiple times. If this is indeed the case, the density and speed offered in the embedded cores may well produce the optimal system design.

Overview of How to Do an ASIC Design (Continued)

In general, considerations of system performance, expected number of design iterations, need for density, amount of memory, potential to use the same customized masterslice in various parts of the overall system design, time to market and need for reduced risk, plus volume of production expected for the system all play an important role in the decision of using a cell-based, gate array or embedded array approach for each part of the design. In addition, varying performance needs of different parts of the system may point to the 0.7-micron or 0.9-micron channel length HCMOS process.

The final partitioning choice of technology and family for each device will affect performance, density, turnaround time, degree of flexibility for design changes, as well as overall cost.

LSI Logic sales and support staff at design centers are trained to help you use LSI Logic ASICs most effectively for an optimal, overall system design.

2. If an Embedded Array proves optimal, the appropriate die outline, package, temperature range, performance, etc. are selected.

3. With MDE software, check the functionality of the design by running extensive simulation with user-defined test patterns. Use LSI Logic's FloorPlanner™ tools to optimize the placement of the design's functional blocks and to generate estimated block delays. The embedded blocks are treated as customized metal megacells—the embedded blocks may be viewed in FloorPlanner and placed to meet routing and timing needs at the top level of the design hierarchy. Delay estimation yielded through the FloorPlanner tool closely matches the post-layout delays.

4. Once the pre-layout simulation results are acceptable, the design is sent to layout. Layout will use the information generated by the FloorPlanner tool as guidelines for cell placement.

5. Layout determines final die outline and embedded block placement. This information is used to start fabrication of the base wafers, while placement and routing of the rest of the design continues.

6. After layout is complete, the actual segment length information is used by the designer to compare post-layout chip performance with pre-layout simulations.

7. Once the designer verifies post-layout simulation, the netlist is sent to the mask vendor.

8. At metal fabrication, the vendor-generated masks are used to metalize the pre-fabricated base wafers for the design (see step 5 above).

9. At wafer sort, processed wafers are sorted on the test floor using customer-generated functional, ac and dc test vectors.

10. Good die are assembled in the selected package(s).

11. Packaged parts are tested on the test floor using the same test patterns exercised for wafer sort.

12. Working parts are delivered to the customer.

13. The mask sets are used to run any further production orders of the design through the manufacturing line.

Design Flow

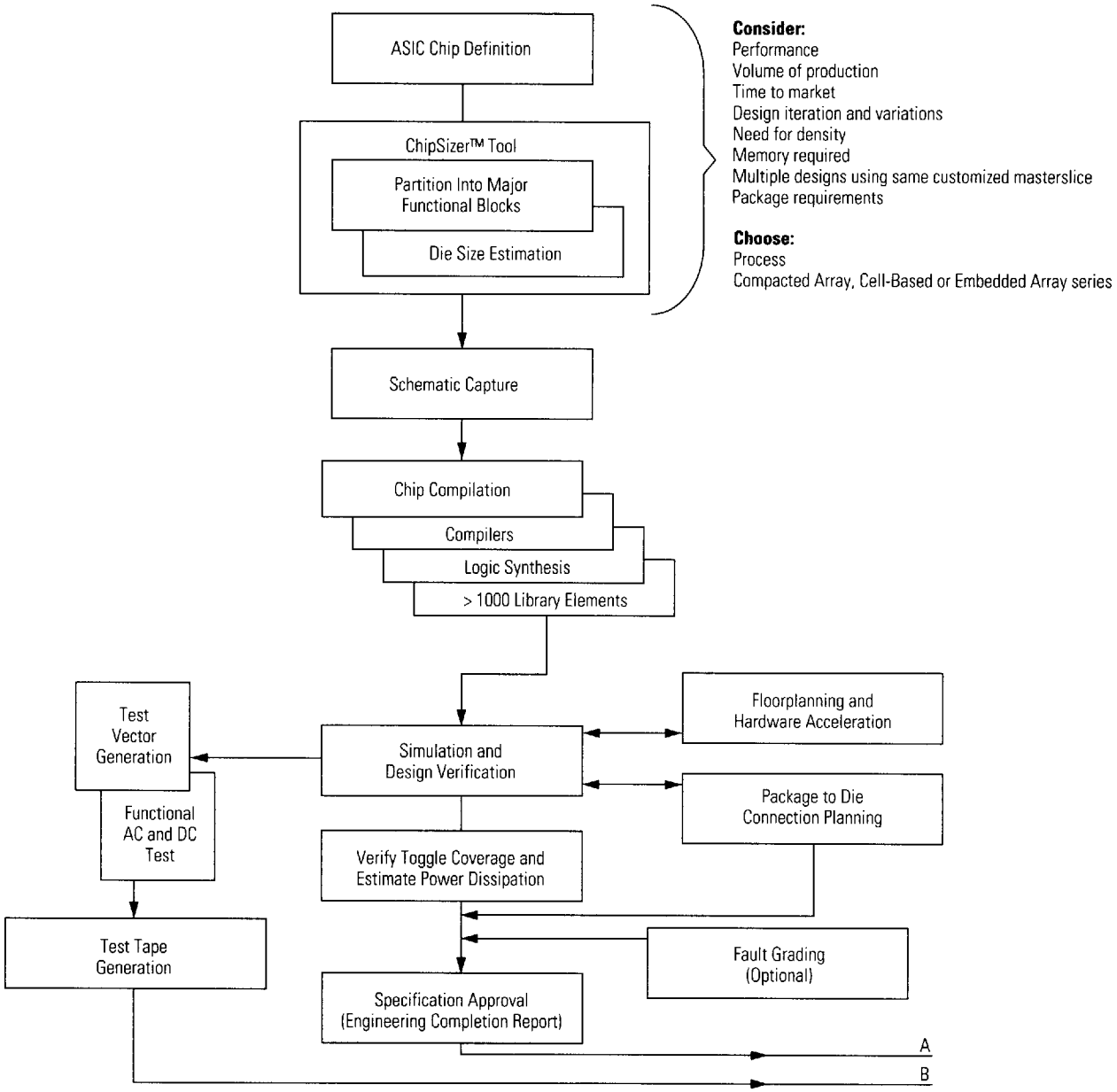


Figure 1a. LEA100K Embedded Array Series Design Flow Diagram

Design Flow
(Continued)

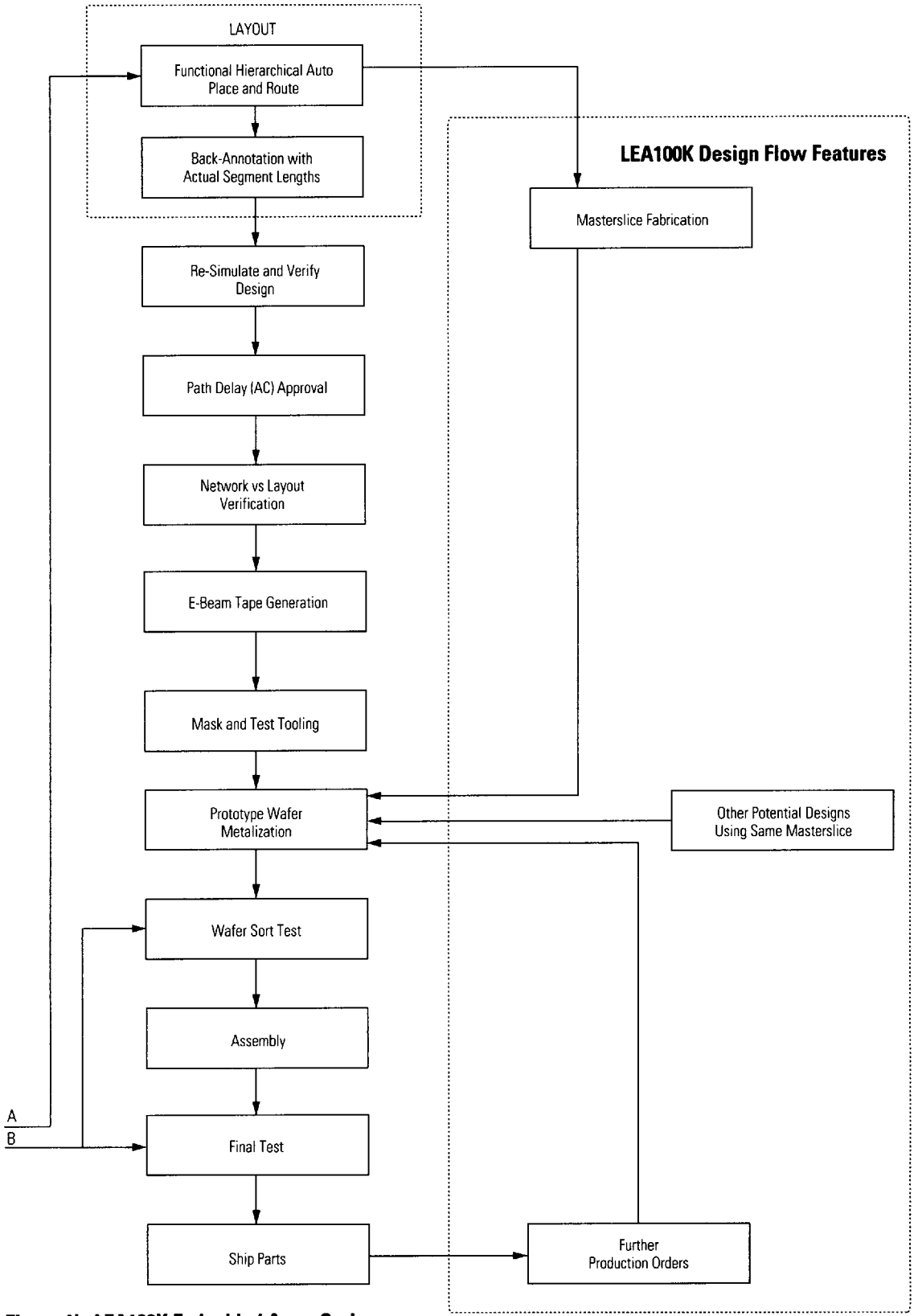


Figure 1b. LEA100K Embedded Array Series Design Flow Diagram

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