



# 2048K x 8 SRAM Module

## Features

- High-density 16-megabit SRAM modules
- High-speed CMOS SRAMs
  - Access time of 70 ns
- Low active power
  - 605 mW (max.), 2M x 8
- Double-sided SMD technology
- TTL-compatible inputs and outputs
- Small footprint SIP
  - PCB layout area of 0.72 sq. in.
- 2V data retention (L version)

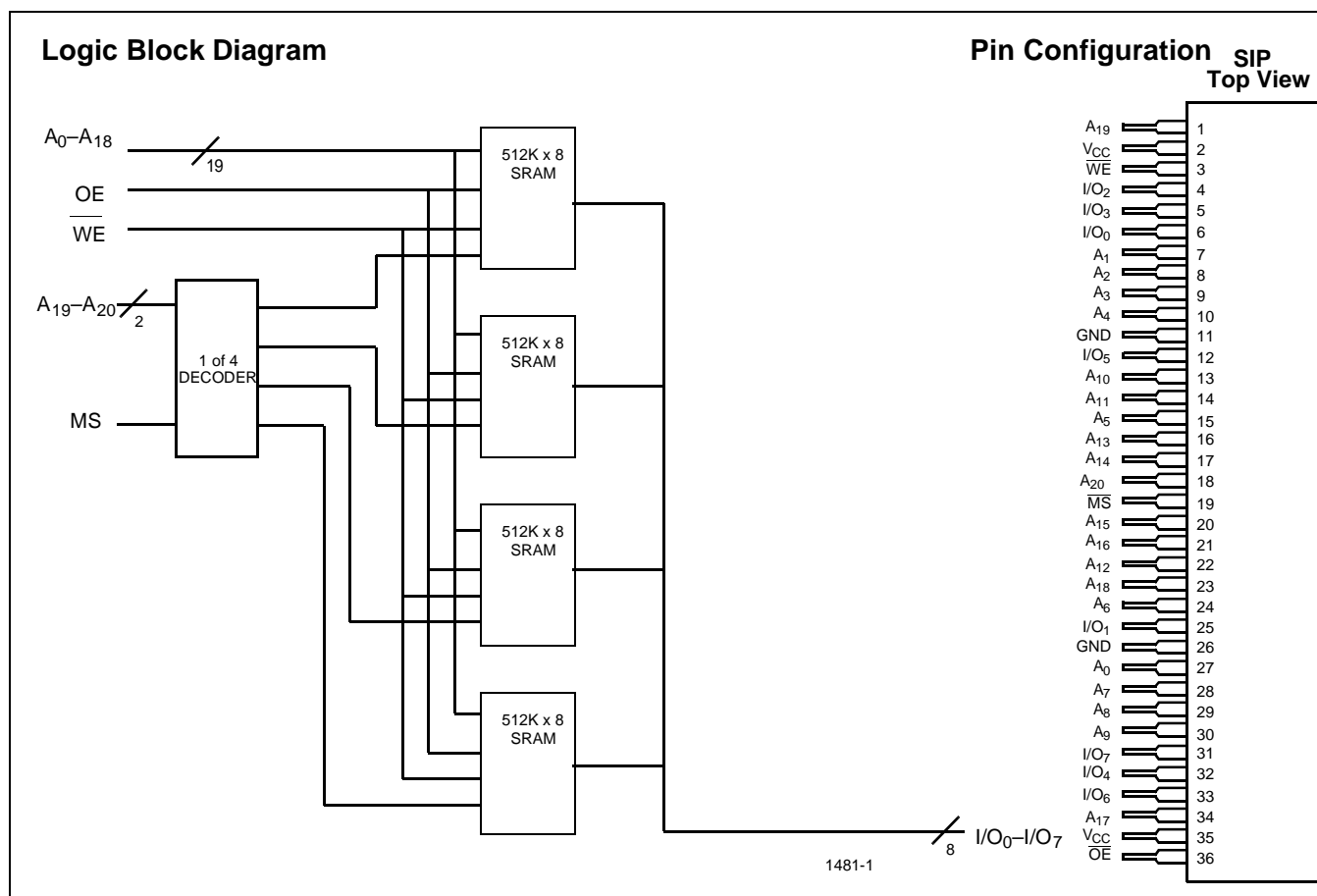
## Functional Description

The CYM1481A is a high-performance 16-megabit static RAM module organized as 2048K words by 8 bits. These modules

are constructed from four 512K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{MS}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs  $\overline{MS}$  and  $\overline{OE}$  active LOW while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.



## Selection Guide

	CYM1481A			
Maximum Access Time (ns)	70	85	100	120
Maximum Operating Current (mA)	110	110	110	110
Maximum Standby Current (mA)	64	64	64	64

## Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Ambient Temperature with  
Power Applied  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$

Supply Voltage to Ground Potential  $-0.3\text{V}$  to  $+7.0\text{V}$

DC Voltage Applied to Outputs  
in High Z State  $-0.3\text{V}$  to  $+7.0\text{V}$

DC Input Voltage  $-0.3\text{V}$  to  $+7.0\text{V}$

Output Current into Outputs (LOW)  $20\text{ mA}$

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Commercial	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		1481A		Unit
				Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = −1.0 mA		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.0 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage			−0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		−20	+20	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		−20	+20	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., $\overline{\text{MS}} \leq V_{\text{IL}}$ , I <sub>OUT</sub> = 0 mA			110	mA
I <sub>SB1</sub>	Automatic $\overline{\text{MS}}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{\text{MS}} \geq V_{\text{IH}}$ , Min. Duty Cycle = 100%			64	mA
I <sub>SB2</sub>	Automatic $\overline{\text{MS}}$ Power-Down Current	Max. V <sub>CC</sub> , $\overline{\text{MS}} \geq V_{\text{CC}} - 0.2\text{V}$ , V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.2V, or V <sub>IN</sub> ≤ 0.2V	Standard		32	mA
			L Version −100, −120		500	μA
			L Version −85		1600	μA

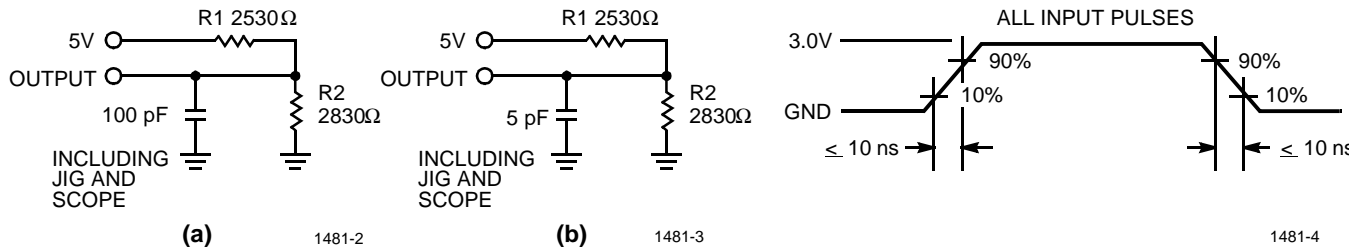
## Capacitance<sup>[1]</sup>

Parameter	Description	Test Conditions	CYM1481AM ax.	Unit
$C_{INA}$	Input Capacitance ( $A_{0-16}, \overline{OE}, \overline{WE}$ )	$T_A = 25^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	125	pF
$C_{INB}$	Input Capacitance ( $A_{17-20}, \overline{MS}$ )		25	pF
$C_{OUT}$	Output Capacitance		165	pF

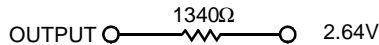
### Note:

1. Tested on a sample basis.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range<sup>[2]</sup>

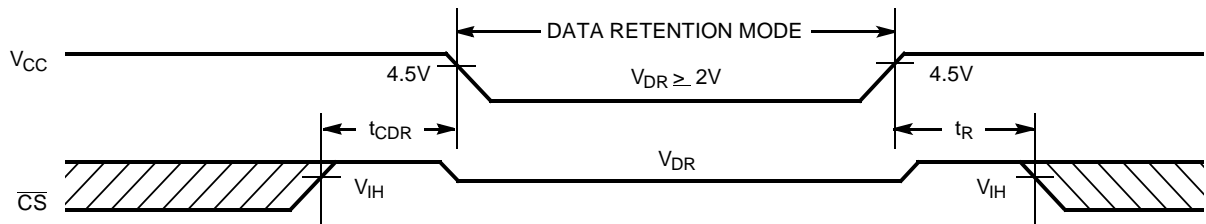
Parameter	Description	1481A-70		1481A-85		1481A-100		1481A-120		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t <sub>RC</sub>	Read Cycle Time	70		85		100		120		ns
t <sub>AA</sub>	Address to Data Valid		70		85		100		120	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		10		10		10		ns
t <sub>AMS</sub>	$\overline{MS}$ LOW to Data Valid		70		85		100		120	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		40		45		50		60	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	5		5		5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[3]</sup>		30		30		35		45	ns
t <sub>LZMS</sub>	$\overline{MS}$ LOW to Low Z <sup>[4]</sup>	5		10		10		10		ns
t <sub>HZMS</sub>	$\overline{MS}$ HIGH to High Z <sup>[3, 4]</sup>		30		30		35		45	ns
WRITE CYCLE <sup>[5]</sup>										
t <sub>WC</sub>	Write Cycle Time	70		85		100		120		ns
t <sub>SMS</sub>	$\overline{MS}$ LOW to Write End	65		75		90		100		ns
t <sub>AW</sub>	Address Set-Up to Write End	65		75		90		100		ns
t <sub>HA</sub>	Address Hold from Write End	5		7		7		7		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		5		5		5		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	65		65		75		85		ns
t <sub>SD</sub>	Data Set-Up to Write End	30		35		40		45		ns
t <sub>HD</sub>	Data Hold from Write End	0		5		5		5		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[3]</sup>		30		30		35		40	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z	5		5		5		5		ns

### Notes:

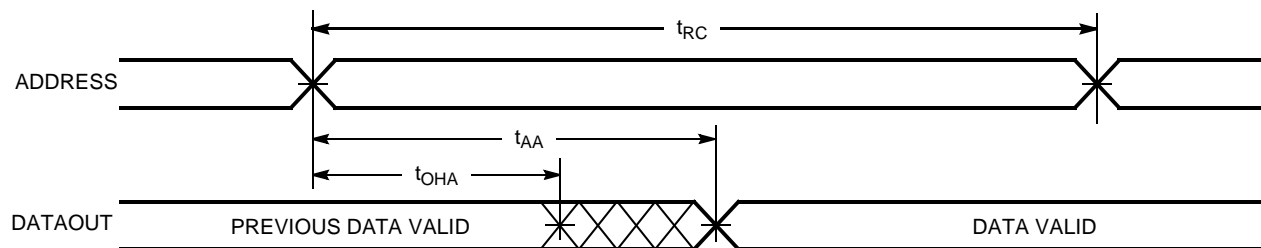
- Test conditions assume signal transition time of 10  $\mu$ s or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZMS}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZMS}$  is less than  $t_{LZMS}$  for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{MS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Data Retention Characteristics** (L Version Only)

Parameter	Description	Test Conditions	1481A-70		1481A-85		1481A-100 148A1-120		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{DR}$	$V_{CC}$ for Retention Data		2		2		2		V
$I_{CCDR}$	Data Retention Current	$V_{DR} = 3.0V$ , $\overline{MS} \geq V_{CC} - 0.2V$ ,		800		800		250	$\mu A$
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0		0		0		ns
$t_R$	Operation Recovery Time		5		5		5		ns

**Data Retention Waveform**


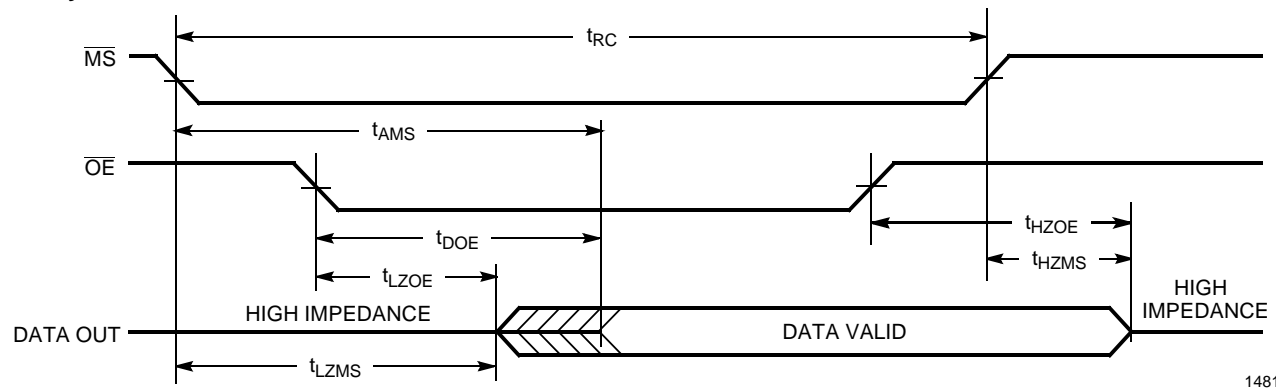
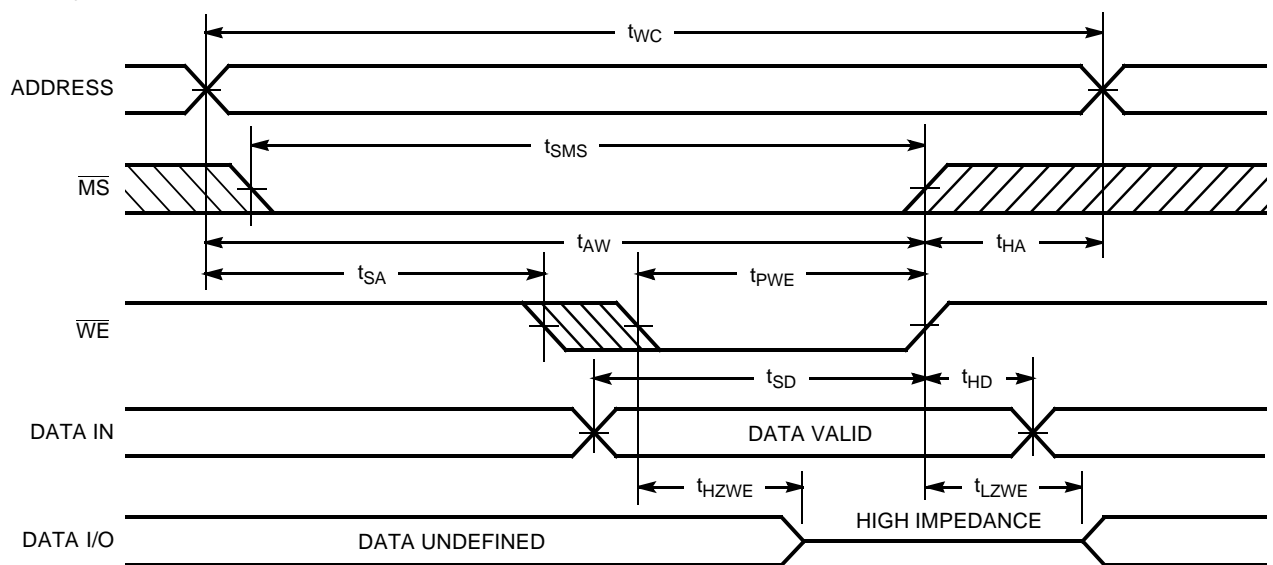
1481-6

**Switching Waveforms**
**Read Cycle No. 1**<sup>[7, 8]</sup>


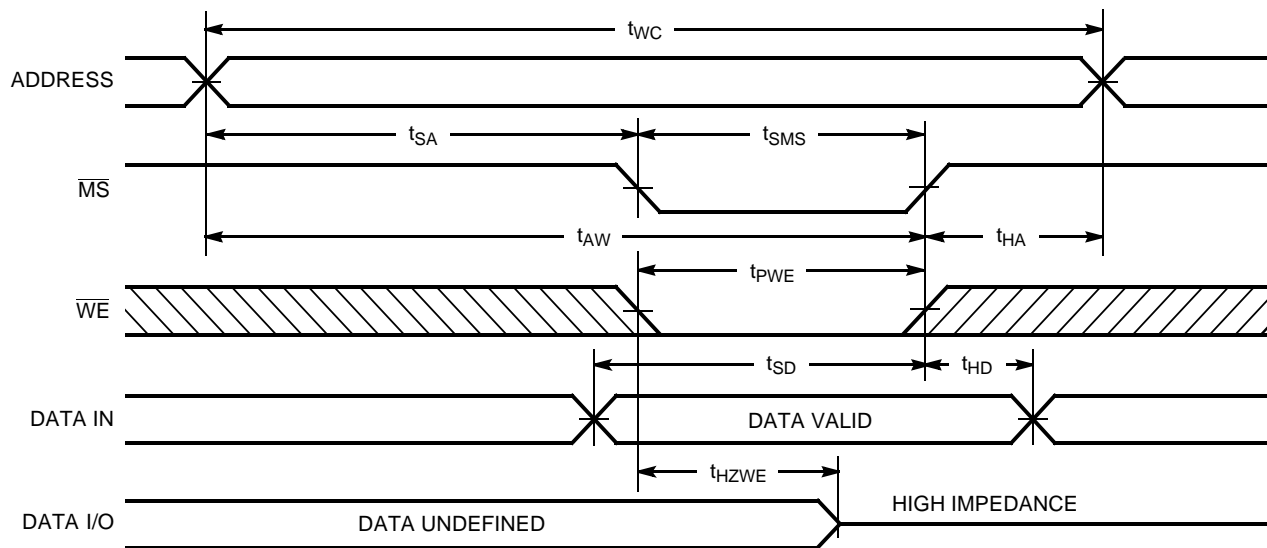
1481-7

**Notes:**

6. Guaranteed, not tested.
7. Device is continuously selected.  $\overline{OE}$ ,  $\overline{MS} = V_{IL}$ .
8. Address valid prior to or coincident with  $\overline{MS}$  transition LOW.

**Switching Waveforms (continued)**
**Read Cycle No. 2**<sup>[8, 9]</sup>

**Write Cycle No. 1**<sup>[5, 10]</sup>

**Notes:**

9.  $\overline{WE}$  is HIGH for read cycle.
10. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

**Switching Waveforms (continued)**
**Write Cycle No. 2**<sup>[5, 10, 11]</sup>


1481-10

**Note:**

11. If  $\overline{MS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

<b>MS</b>	<b>WE</b>	<b>OE</b>	<b>Input/Outputs</b>	<b>Mode</b>
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Type</b>	<b>Package Type</b>	<b>Operating Range</b>
70	CYM1481APS-70C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS-70C			
85	CYM1481APS-85C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS-85C			
100	CYM1481APS-100C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS-100C			
120	CYM1481APS-120C	PS10	36-Pin SIP Module	Commercial
	CYM1481ALPS-120C			

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# Package Diagram

## 36-Pin SIP Module PS10

