# M27C040
# 4M (512K x 8) CHMOS EPROM

- **JEDEC Approved EPROM Pinout**
  - **— 32-Pin DIP**
  - **— Simple Upgrade from Lower Densities**
- **Versatile EPROM Features**
  - **— CMOS and TTL Compatibility**
  - **— Two Line Control**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Time as Fast as 60 Seconds**
- **High-Performance**
  - **— 170 ns, ±10% $V_{CC}$**
  - **— 50 mA $I_{CC}$ Active**

The Intel M27C040 is a 5V-only, 4,194,304-bit Erasable Programmable Read Only Memory, organized as 524,288 words of 8 bits each. It is pin compatible with lower density DIP EPROMs (JEDEC).

The M27C040 represents state-of-the-art 1 micron CMOS manufacturing technology while providing unequaled performance. Its 170 ns speed ($T_{ACC}$) offers no-wait-state operation with high performance CPUs in applications ranging from numerical control to office automation to telecommunications.

The M27C040 is equally at home in both a TTL or CMOS environment. It programs as fast as 60 seconds using Intel's industry leading Quick-Pulse Programming algorithm.



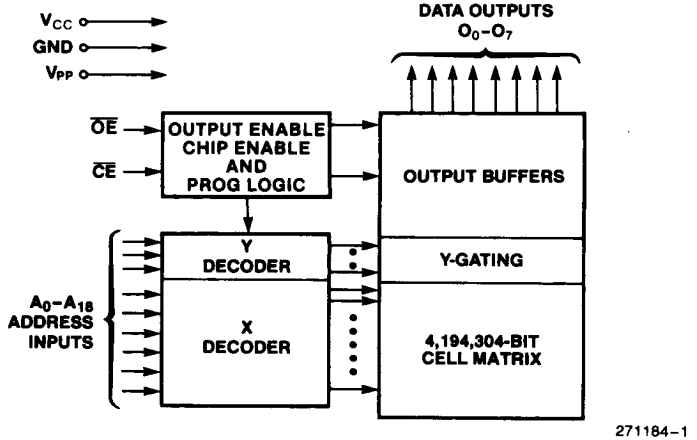



**Figure 1. Block Diagram**

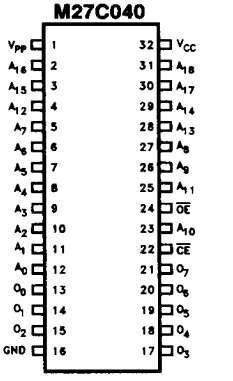


August 1991
Order Number: 271184-001

**Pin Names**

| | |
|---|---|
| $A_0$–$A_{19}$ | ADDRESSES |
| $\overline{CE}$ | CHIP ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| $\overline{PGM}$ | PROGRAM |
| $O_0$–$O_7$ | OUTPUTS |
| NC | NO INTERNAL CONNECT |

| 2Mbit | 1Mbit | 512K | 256K |
|---|---|---|---|
| $V_{PP}$ | $V_{PP}$ | | |
| $A_{16}$ | $A_{16}$ | | |
| $A_{15}$ | $A_{15}$ | $A_{15}$ | $V_{PP}$ |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ |
| $O_0$ | $O_0$ | $O_0$ | $O_0$ |
| $O_1$ | $O_1$ | $O_1$ | $O_1$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ |
| GND | GND | GND | GND |

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| 256K | 512K | 1Mbit | 2Mbit |
|---|---|---|---|
| | | $V_{CC}$ / $\overline{PGM}$ | $V_{CC}$ / $\overline{PGM}$ |
| $V_{CC}$ | $V_{CC}$ | NC | $A_{17}$ |
| $A_{14}$ | $A_{14}$ | $A_{14}$ | $A_{14}$ |
| $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ |
| $A_8$ | $A_8$ | $A_8$ | $A_8$ |
| $A_9$ | $A_9$ | $A_9$ | $A_9$ |
| $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ |
| $\overline{OE}$ | $\overline{OE}/V_{PP}$ | $\overline{OE}$ | $\overline{OE}$ |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ |
| $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ |

**Figure 2. DIP Pin Configuration**

## ABSOLUTE MAXIMUM RATINGS*

Case Temperature
under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to 125°C
Voltage on Any Pin
(except $A_9$, $V_{CC}$ and $V_{PP}$)
with Respect to GND ..... −0.6V to 6.5V(1)
Voltage on $A_9$ with
Respect to GND ..... −0.6V to 13.0V(1)
$V_{PP}$ Supply Voltage with
Respect to GND ..... −0.6V to 14V(1)
$V_{CC}$ Supply Voltage with
Respect to GND ..... −0.6V to 7.0V(1)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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## READ OPERATION DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | | | | ±1.0 | µA | $V_{IN} = 0V$ to 5.5V |
| $I_{LO}$ | Output Leakage Current | | | | ±10 | µA | $V_{OUT} = 0V$ to 5.5V |
| $I_{SB}$ | $V_{CC}$ Standby Current | | | | 1.0 | mA | $\overline{CE} = V_{IH}$ |
| | | | | | 100 | µA | $\overline{CE} = V_{CC} \pm 0.2V$ |
| $I_{CC}$ | $V_{CC}$ Operating Current | 2 | | | 50 | mA | $\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA |
| $I_{PP}$ | $V_{PP}$ Operating Current | 2 | | | 10 | µA | $V_{PP} = V_{CC}$ |
| $I_{OS}$ | Output Short Circuit Current | 3, 5 | | | 100 | mA | |
| $V_{IL}$ | Input Low Voltage | | −0.5 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC} + 0.5$ | V | |
| $V_{OL}$ | Output Low Voltage | | | | 0.45 | V | $I_{OL} = 2.1$ mA |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH} = -400$ µA |
| $V_{PP}$ | $V_{PP}$ Operating Voltage | 4 | $V_{CC} - 0.7$ | | $V_{CC}$ | V | |

**NOTES:**
1. Minimum DC voltage is −0.5V on input/output pins. During transitions, this level may undershoot to −2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is $V_{CC}$ + 0.5V which, during transitions, may overshoot to $V_{CC}$ + 2.0V for periods < 20 ns.
2. Maximum active power usage is the sum $I_{PP} + I_{CC}$. Maximum current is with outputs $O_0$ to $O_7$ unloaded.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. $V_{PP}$ may be connected directly to $V_{CC}$, or may be one diode voltage drop below $V_{CC}$. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
5. Sampled, not 100% tested.

## READ OPERATION AC CHARACTERISTICS(1) $V_{CC}$ = 5.0V ±10%

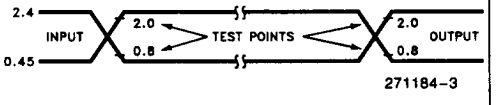
| Versions(4) | | $V_{CC}$ ±10% | 27C040-17 | | 27C040-20 | | Units |
|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Notes | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to Output Delay | | | 170 | | 200 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | 2 | | 170 | | 200 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay | 2 | | 60 | | 70 | ns |
| $t_{DF}$ | $\overline{OE}$ High to Output High Z | 3 | | 50 | | 60 | ns |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First | 3 | 0 | | 0 | | ns |

**NOTES:**
1. See AC Input/Output Reference Waveform for timing measurements.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. Sampled, not 100% tested.
4. Model number prefixes: No prefix = CERDIP.
5. Typical values are for $T_A$ = 25°C and nominal supply voltages.

## CAPACITANCE(3) $T_A$ = 25°C, f = 1MHz

| Symbol | Parameter | Typ(5) | Max | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | Output Capacitance | 8 | 12 | pF | $V_{OUT}$ = 0V |
| $C_{VPP}$ | $V_{PP}$ Capacitance | 18 | 25 | pF | $V_{PP}$ = 0V |

### AC INPUT/OUTPUT REFERENCE WAVEFORM

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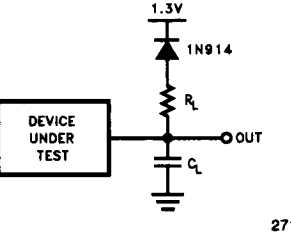
AC test inputs are driven at $V_{OH}$ (2.4 $V_{TTL}$) for a logic "1" and $V_{OL}$ (0.45 $V_{TTL}$) for a logic "0". Input timing begins at $V_{IH}$ (2.0 $V_{TTL}$) and $V_{IL}$ (0.8 $V_{TTL}$). Output timing ends at $V_{IH}$ and $V_{IL}$. Input rise and fall times (10% to 90%) ≤ 10 ns.

### AC TESTING LOAD CIRCUIT




$C_L$ = 100 pF
$C_L$ Includes Jig Capacitance
$R_L$ = 3.3 KΩ

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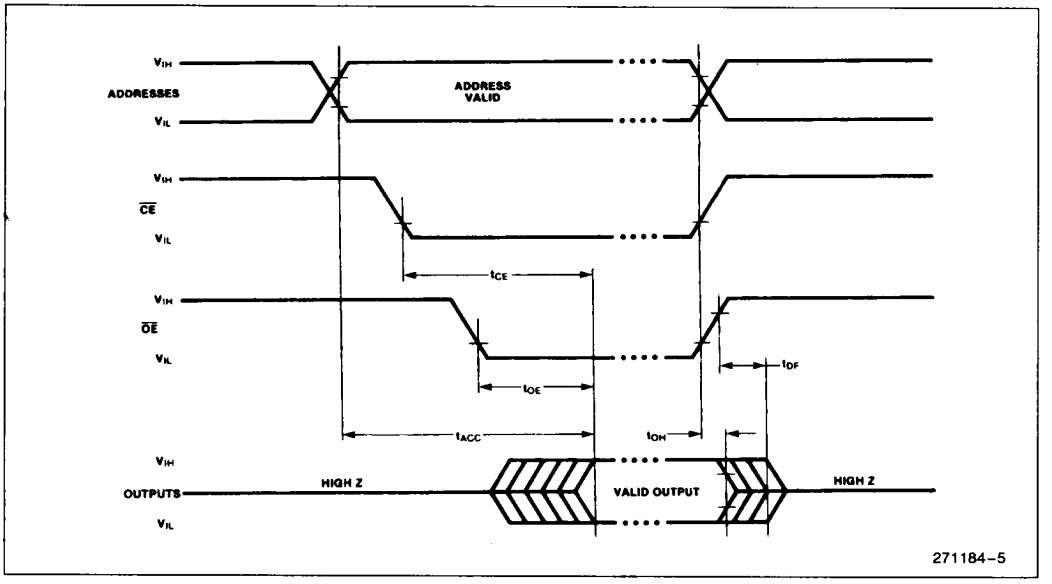
## AC WAVEFORMS




## DEVICE OPERATION

The Mode Selection table lists M27C040 operating modes. Read Mode requires a single 5V power supply. All inputs, except $V_{CC}$ and $V_{PP}$, and $A_9$ during int$_e$ligent Identifier Mode, are TTL or CMOS.

**Table 1. Mode Selection**

| Mode | | Notes | $\overline{CE}$ | $\overline{OE}$ | $A_9$ | $A_0$ | $V_{PP}$ | $V_{CC}$ | Outputs |
|---|---|---|---|---|---|---|---|---|---|
| Read | | 1 | $V_{IL}$ | $V_{IL}$ | X | X | $V_{CC}$ | $V_{CC}$ | $D_{OUT}$ |
| Output Disable | | | $V_{IL}$ | $V_{IH}$ | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Standby | | | $V_{IH}$ | X | X | X | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | | 2 | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $V_{CP}$ | $D_{IN}$ |
| Program Verify | | | $V_{IH}$ | $V_{IL}$ | X | X | $V_{PP}$ | $V_{CP}$ | $D_{OUT}$ |
| Program Inhibit | | | $V_{IH}$ | $V_{IH}$ | X | X | $V_{PP}$ | $V_{CP}$ | High Z |
| int$_e$ligent Identifier | Manufacturer | 2, 3 | $V_{IL}$ | $V_{IL}$ | $V_{ID}$ | $V_{IL}$ | $V_{CC}$ | $V_{CC}$ | 89 H |
| | Device | | $V_{IL}$ | $V_{IL}$ | $V_{ID}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | 3D H |

**NOTES:**
1. X can be $V_{IL}$ or $V_{IH}$
2. See DC Programming Characteristics for $V_{CP}$, $V_{PP}$ and $V_{ID}$ voltages.
3. $A_1$–$A_8$, $A_{10}$–$A_{18}$ = $V_{IL}$

## Read Mode

The M27C040 has two control functions; both must be enabled to obtain data at the outputs. $\overline{CE}$ is the power control and device select. $\overline{OE}$ controls the output buffers to gate data to the outputs. With addresses stable, the address access time ($t_{ACC}$) equals the delay from $\overline{CE}$ to output ($t_{CE}$). Outputs display valid data $t_{OE}$ after $\overline{OE}$'s falling edge, assuming $t_{ACC}$ and $t_{CE}$ times are met.

**$V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.**

## Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two control inputs to accommodate multiple memory connections. Two-line control provides for:

a) lowest possible memory power dissipation

b) complete assurance that data bus contention will not occur

To efficiently use these two control inputs, and address decoder should enable $\overline{CE}$, while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode.

## Standby Mode

Standby Mode substantially reduces $V_{CC}$ current. When $\overline{CE}$ = $V_{IH}$, the outputs are in a high impedance state, independent of $\overline{OE}$.

## Program Mode

***Caution: Exceeding 14V on $V_{PP}$ will permanently damage the device.***

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

Program Mode is entered when $V_{PP}$ is raised to 12.75V. Data is introduced by applying an 8-bit word to the output pins. Pulsing $\overline{CE}$ low while $\overline{OE}$ = $V_{IH}$ programs that data into the device.

## Program Verify

A verify should be performed following a program operation to determine that bits have been correctly programmed. With $V_{CC}$ at 6.25V a substantial program margain is ensured. The verify is performed with $\overline{CE}$ at $V_{IH}$. Valid data is available $t_{OE}$ after $\overline{OE}$ falls low.

## Program Inhibit

Program Inhibit Mode allows parallel programming of multiple EPROMs with different data. $\overline{CE}$-high inhibits programming of non-targeted devices. Except for $\overline{CE}$ and $\overline{OE}$, parallel EPROMs may have common inputs.

## int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode will determine an EPROM's manufacturer and device type, allowing programming equipment to automatically match a device with its proper programming algorithm.

This mode is activated when a programmer forces 12V ±0.5V on $A_9$. With $\overline{CE}$, $\overline{OE}$, $A_1$–$A_8$, and $A_{10}$–$A_{18}$ at $V_{IL}$, $A_0$ = $V_{IL}$ will present the manufacturer code and $A_0$ = $V_{IH}$ the device code. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

## SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels ($I_{SB}$), active current levels ($I_{CC}$), and transient current peaks produced by falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 $\mu$F ceramic capacitor connected between its $V_{CC}$ and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every 8 devices, a 4.7 $\mu$F electrolytic capacitor should be placed at the array's power supply connection between $V_{CC}$ and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

## ERASURE CHARACTERISTICS

Erasure begins when EPROMs are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting can erase an EPROM in approximately 3 years, while it takes approximately 1 week when exposed to direct sunlight. If the device is exposed to these lighting conditions for extended periods, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to ultraviolet light of wavelength 2537Å. The integrated dose (UV intensity $\times$ exposure time) for erasure should be a minimum of 15 Wsec/cm$^2$. Erasure time is approximately 30 minutes using an ultraviolet lamp with a 12000 $\mu$W/cm$^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes. An EPROM can be permanently damaged if the integrated dose exceeds 7258 Wsec/cm$^2$ (1 week @ 12000 $\mu$W/cm$^2$).

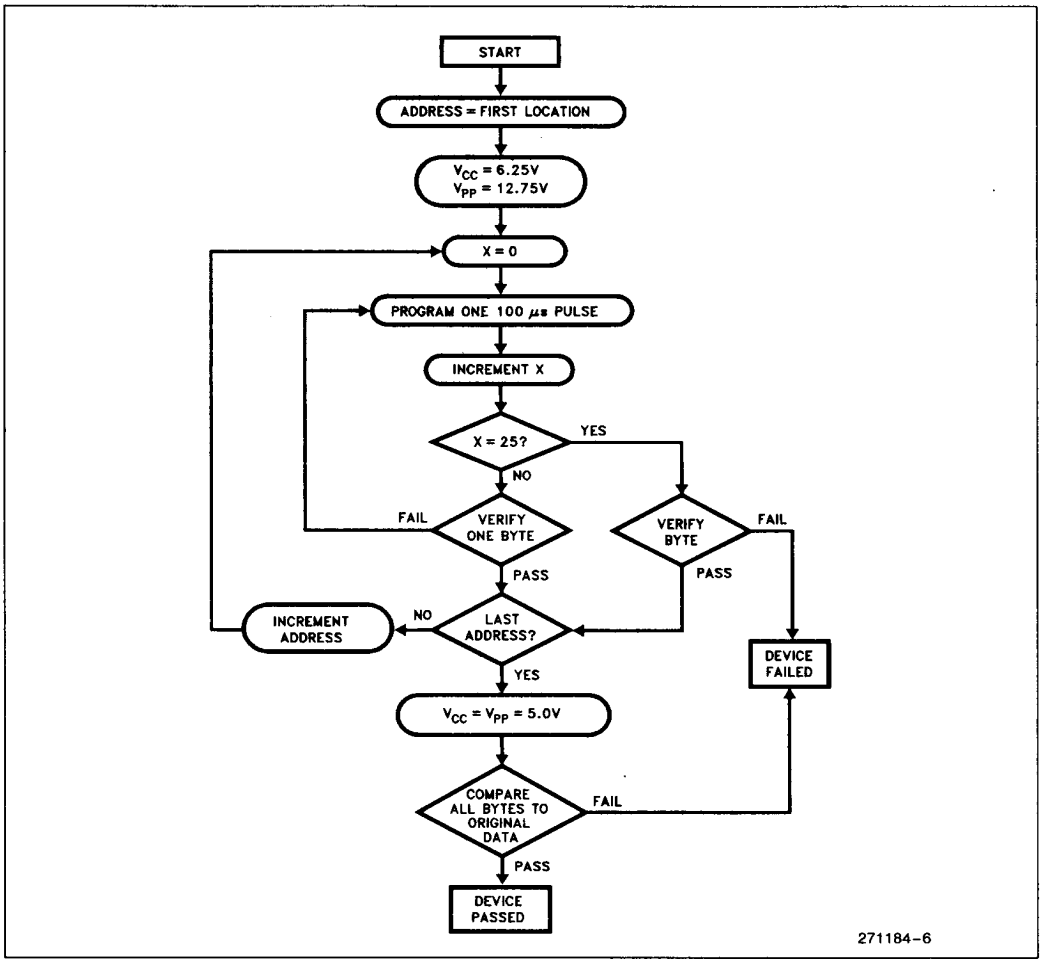



**Figure 3. Quick-Pulse Programming Algorithm**

## Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming Algorithm programs Intel's M27C040. Developed to substantially reduce programming throughput, this algorithm can program the M27C040 as fast as 60 seconds. Actual programming time depends on programmer overhead.

The Quick-Pulse Programming Algorithm employs a 100 μs pulse followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm terminates if 25 attempts fail to program a byte.

The entire program pulse/byte verify sequence is performed with $V_{PP}$ = 12.75V and $V_{CC}$ = 6.25V. When programming is complete, all bytes are compared to the original data with $V_{CC}$ = $V_{PP}$ = 5.0V.

## DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

| Symbol | Parameter | Notes | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | | | | 1 | μA | $V_{IN} = V_{IL}$ or $V_{IH}$ |
| $I_{CP}$ | $V_{CC}$ Program Current | 1 | | | 50 | mA | $\overline{CE} = V_{IL}$ |
| $I_{PP}$ | $V_{PP}$ Program Current | 1 | | | 50 | mA | $\overline{CE} = V_{IL}$ |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.4 | | 6.5 | V | |
| $V_{OL}$ | Output Low Voltage (Verify) | | | | 0.45 | V | $I_{OL} = 2.1$ mA |
| $V_{OH}$ | Output High Voltage (Verify) | | 3.5 | | | V | $I_{OH} = -2.5$ mA |
| $V_{ID}$ | $A_9$ intelligent Identifier Voltage | | 11.5 | 12.0 | 12.5 | V | |
| $V_{PP}$ | $V_{PP}$ Program Voltage | 2, 3 | 12.5 | 12.75 | 13.0 | V | |
| $V_{CP}$ | $V_{CC}$ Supply Voltage (Program) | 2 | 6.0 | 6.25 | 6.5 | V | |

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## AC PROGRAMMING CHARACTERISTICS(4) $T_A = 25°C \pm 5°C$

| Symbol | Parameter | Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VCS}$ | $V_{CP}$ Setup Time | 2 | 2 | | | μs |
| $t_{VPS}$ | $V_{PP}$ Setup Time | 2 | 2 | | | μs |
| $t_{AS}$ | Address Setup Time | | 2 | | | μs |
| $t_{DS}$ | Data Setup Time | | 2 | | | μs |
| $t_{PW}$ | $\overline{CE}$ Program Pulse Width | | 95 | 100 | 105 | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | | μs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | μs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | 5 | | | 150 | ns |
| $t_{DFP}$ | $\overline{OE}$ High to Output High Z | 5, 6 | 0 | | 130 | ns |
| $t_{AH}$ | Address Hold Time | | 0 | | | μs |

**NOTES:**
1. Maximum current is with outputs $O_0$–$O_7$ unloaded.
2. $V_{CP}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
3. When programming, a 0.1 μF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.
4. See AC Input/Output Reference Waveform for timing measurements.
5. $t_{OE}$ and $t_{DFP}$ are device characteristics but must be accommodated by the programmer.
6. Sampled, not 100% tested.

## PROGRAMMING WAVEFORMS