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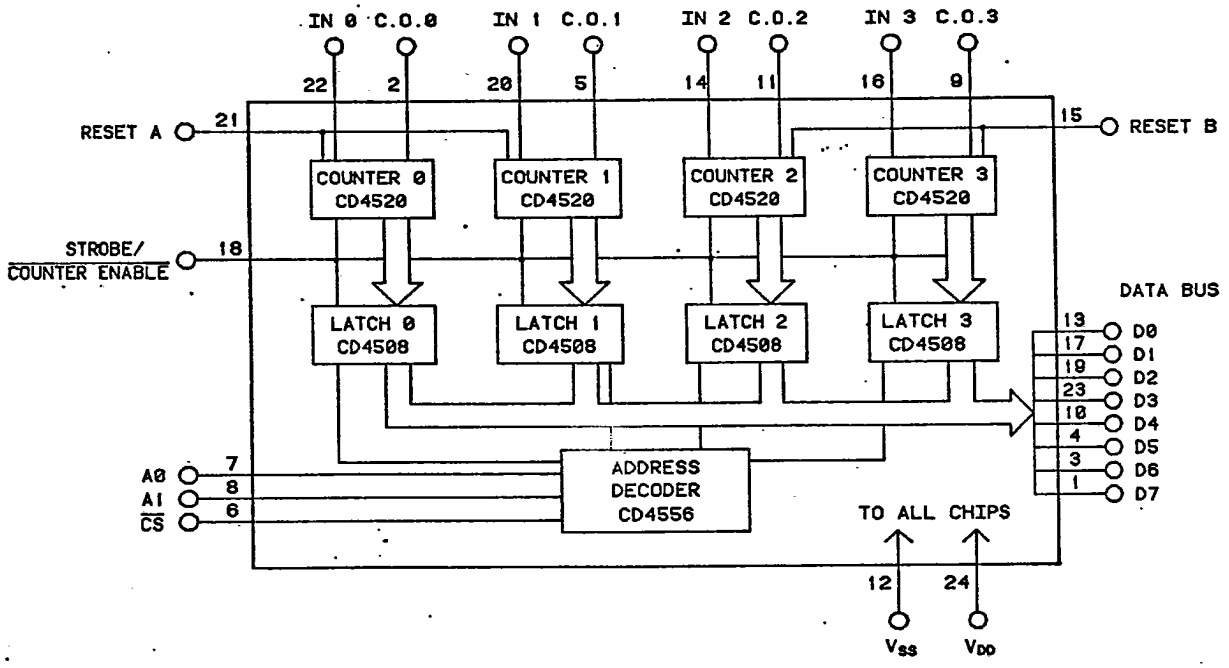
T-45-23-05

D400

QUAD 8 BIT BINARY COUNTER-3-STATE LATCH



The D400 is a hybrid Quad 8 bit binary counter and 3-state latch designed to interface with microprocessor based systems.

Developed during the CRRES satellite program the D400 is made with radiation hardened CMOS (10^6 Rads) packaged in a 24 pin double width hybrid DIP and processed to MIL-STD-883B.

PRELIMINARY DATA SHEET

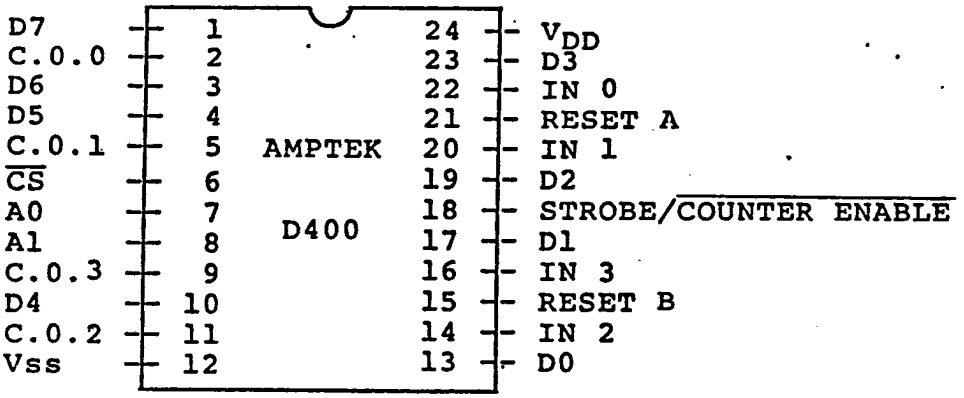
The D400 consists of four identical 8 bit binary counters connected to four 8 bit transparent latches with 3-state outputs. An address decoder allows the selection of one of the four latches to be read out on the eight DATA lines.

Inputs are provided to each of four counters, which are incremented on the negative-going input transition. The output of the last stage, Q8, of each counter is also provided, (C.0.0, C.0.1, C.0.2, C.0.3) so that cascading may be accomplished by connecting the output of one counter to the input of the next. In this way, the D400 may be configured as two 16 bit or one 32 bit counter. Cascading from one D400 package to the next makes possible any conbination of 8 bit counter. (See Note)

The counter outputs are strobed into the latches by a pulse applied to the "STROBE" input. For the duration of this strobe pulse (i.e. while "STROBE" is high), the counter inputs are disabled, to ensure reading a stable count.

Two reset lines are provided. "RESET A" resets counters 0 and 1. "RESET B" resets 2 and 3. RESET is an independent function and a high level on a RESET input always holds the outputs of the respective counters low, regardless of the state of the other inputs. Address lines A_0 and A_1 and chip select $\overline{CS}$ select the latch which is enabled to drive the data lines. With $\overline{CS}$ high, none of the latches is selected and the D_0 - D_7 outputs are in the high impedance state. With $\overline{CS}$ low, the latch selected by A_0 and A_1 is enabled.

CONNECTION DIAGRAM



Top view

Metal case connected to Pin 12 on D400RH; Floating on D400.
Size: .800"x1.375"x.185" (Distance between pin rows: .600" apart).
Weight: 10gr.
PRICE: D400 RH (Radiation Hardened - MIL-STD-883B) 1-24 $900, 25-49 $845.
D400 (MIL-STD-883B) 1-24 $350, 24-49 $325.

NOTE ON CASCADING

The counter in each of the four sections of the D400 is a CD4520B dual 4 bit up counter configured as an 8 bit binary counter.

The clock inputs to all four counters are gated with "STROBE/COUNTER ENABLE" to inhibit counter transitions while the latches are strobed. This gating causes a counter to be incremented if its input is high during the leading edge of "STROBE/COUNTER ENABLE."

If 2 counter sections are directly cascaded, this causes an additional count in the higher order counter whenever carry out ("bit 7") of the lower order counter is high during strobe. The resulting counting sequence is unique and resulting counts may be easily corrected in software.

As an example with two counter sections cascaded to produce a 16 bit counter an actual count of 128 will appear as:

MSB LSB
00000001 10000000
256 128

or

256 + 128 = 384

Where the "256"count is caused by "bit 7" being high during STROBE.

To correct counts, subtract 256 in all cases in which "bit 7" is high.

In this example

384 - 256 = 128

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