PRELIMINARY

Dual SLIC

Dual Subscriber Line Interface Circuit
Le57D11 Device

APPLICATIONS

- **Ideal for low cost, high performance line card applications (CO, DLC)**
- **Meets requirements for countries such as: China, Korea, Japan, Taiwan, and Australia**
- **Fulfills the following China specifications: GF002-9002.1**

FEATURES

- **Dual Channel SLIC device with small footprint**
- **On-chip Thermal Management (TMG) feature in normal and reverse polarity**
- **Control states: Active (normal and reversal polarity), Standby, and Disconnect**
- **On-hook transmission**
- **Low standby power**
- **–39 V to –58 V battery operation**
- **Two-wire impedance set by single external impedance**
- **Per channel fault detection**
- **Device level thermal shutdown**
- **Programmable constant-current feed (Range TBD)**
- **Programmable loop-detect threshold**
- **Programmable ring-trip detect threshold**
- **Only +5 V and battery supply required**
- **Current Gain = 500**

DESCRIPTION

The innovative Le57D11 Dual Channel SLIC device was designed for high-density POTS applications requiring a small footprint SLIC device with significant power savings. By combining the line interface of two channels into one SLIC device, the Le57D11 device enables the design of a low cost, high performance, and fully programmable line interface for multiple country applications worldwide. The on-chip Thermal Management (TMG) feature allows for significantly reduced power dissipation on the device. Another benefit is that it is offered in space-saving package types 44-pin eTQFP and 32-pin PLCC. The small footprint of the SLIC device allows designers to save board space, increasing the density of lines on the board. The Le57D11 device is also designed to significantly reduce the number of external components required for line card design.

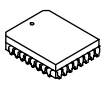
Legerity offers a range of compatible SLAC devices that perform the codec function in a line card. In particular, the Legerity Quad SLAC device combined with the Le57D11 device provides a programmable line circuit that can be configured for varying requirements.

RELATED LITERATURE

- **080147 Am79Q02/021/031 Quad SLAC Data Sheet**
- **080753 Le58QL02/021/031 QLSLAC™ Data Sheet**
- **080748 Le57D11 Evaluation Board User's Guide**

ORDERING INFORMATION

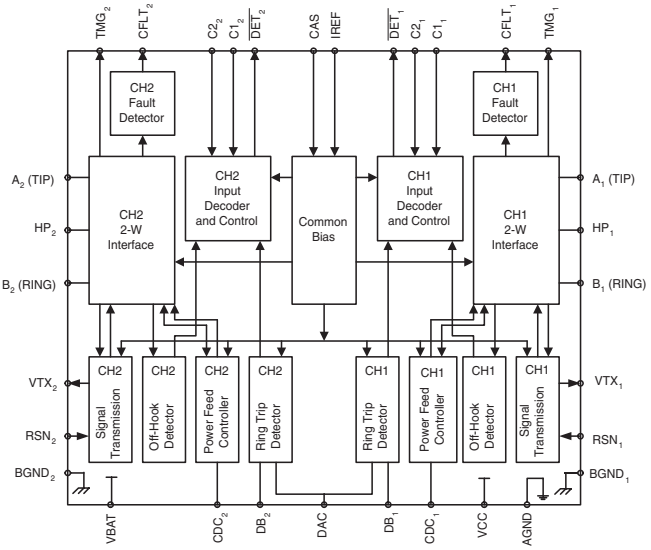
32-Pin PLCC



44-pin eTQFP

Device	Performance Grade
Le57D111JC	32-pin PLCC, 48 dB Polarity Reversal
Le57D113JC	32-pin PLCC, 48 dB No Polarity Reversal
Le57D111TC	44-pin eTQFP, 48 dB Polarity Reversal
Le57D113TC	44-pin eTQFP, 48 dB No Polarity Reversal

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The Le57D11 device is designed for long loop high-density POTS applications requiring a power saving, small footprint SLIC. The Le57D11 device increases line card density by integrating two SLIC devices into a single 32 pin package. This reduction in board space allows for higher density linecard, which allows for amortizing common hardware across more channels. The Le57D11 device gives line card designers a simple control interface that supports four states: Active, Polarity Reversal, Standby, and Disconnect (Ringing). The Le57D11 device is low cost and high performance, providing key features required for POTS markets requiring only loop start. The device includes a thermal management resistor option.

BLOCK DESCRIPTIONS

Fault Detector

These blocks provide fault detection on a per channel basis for short to ground, short to battery, or certain AC faults. The Le57D11 device provides fault detection by having one fault detector in each channel. Under fault conditions — either a short to ground, a short to battery, or specified AC power cross faults — the Le57D11 device detects the longitudinal unbalance and trips the detector. Once the detector is tripped, the CFLT pin is pulled low and keeps toggling between Vth1 and Vth2 (refer Figure 2) until the fault is removed. An external 0.1µF capacitor is connected between the CFLT pin and AGND, which provides a fault trigger delay of about 4 mS (T1) and release delay of 24 mS (T2). During release delay, the affected channel is shutdown which sets Tip and Ring to a Disconnect state. The trigger delay prevents short transients on Tip and Ring from triggering the channel shutdown when a fault is not present.

Figure 1. Fault Detector

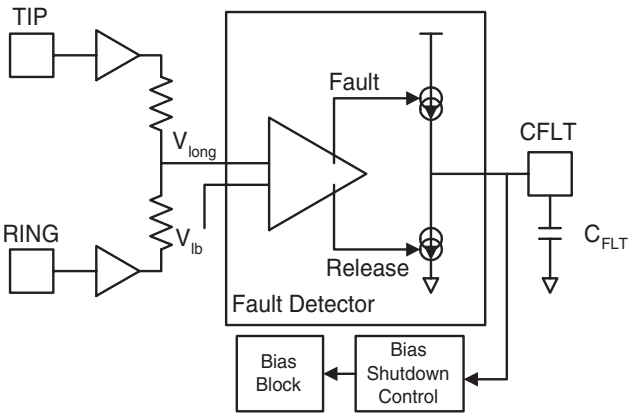
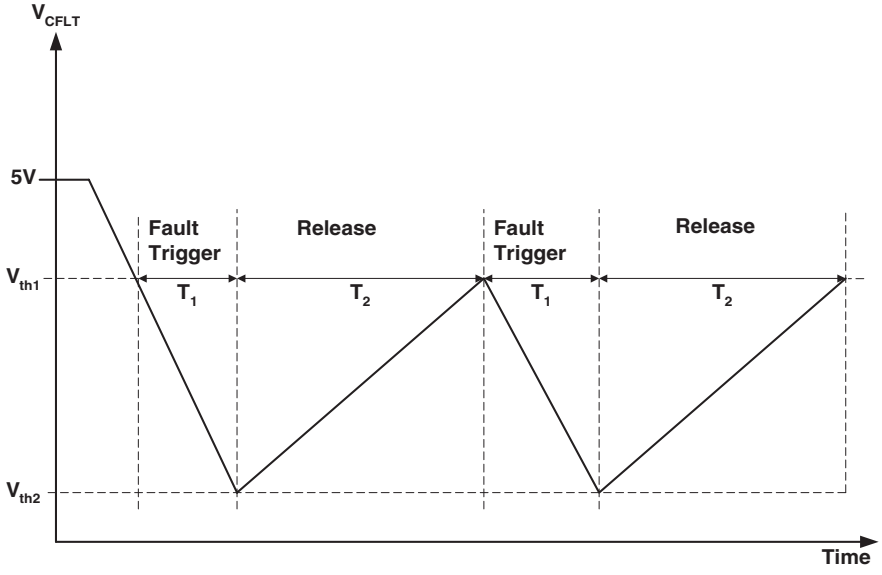


Figure 2. Fault Detection Waveform



$$T1 = \frac{CFLT(V_{th1} - V_{th2})}{I_{trigger}} \qquad T2 = \frac{CFLT(V_{th1} - V_{th2})}{I_{release}}$$

Two-Wire Interface

The two-wire interfaces provide DC current and send voice signals to a telephone apparatus connected to the line card with a two-wire line. The two-wire interface also receives the returning voice signals from the telephone transmitter.

Signal Transmission

The AC line voltage is sensed by a differential amplifier between the A_i (TIP) and HP_i leads. The output of this amplifier is equal to the AC metallic components of the line voltages and is output at VTX_i. The transmission circuit also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage. The longitudinal feedback does not affect metallic signals.

Power Feed Controller and Common Bias

The power feed controllers have three sections: (1) the battery feed circuit, (2) the polarity reversal circuit, and (3) the common bias circuit. The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. The polarity reversal circuit provides the capability to reverse the loop current for pay telephone key pad disable and other applications. The bias circuit provides a filtered reference voltage, which is offset from the subscriber line voltage, and a signal which sets the current limit.

Input Decoder and Control

The input decoder and control block provides a means for a microprocessor or SLAC IC to control such system states as Active, Standby, Disconnect (Ringing), and Polarity Reversal. The input decoder and control block has TTL-compatible inputs, which set the operating states of the SLIC device.

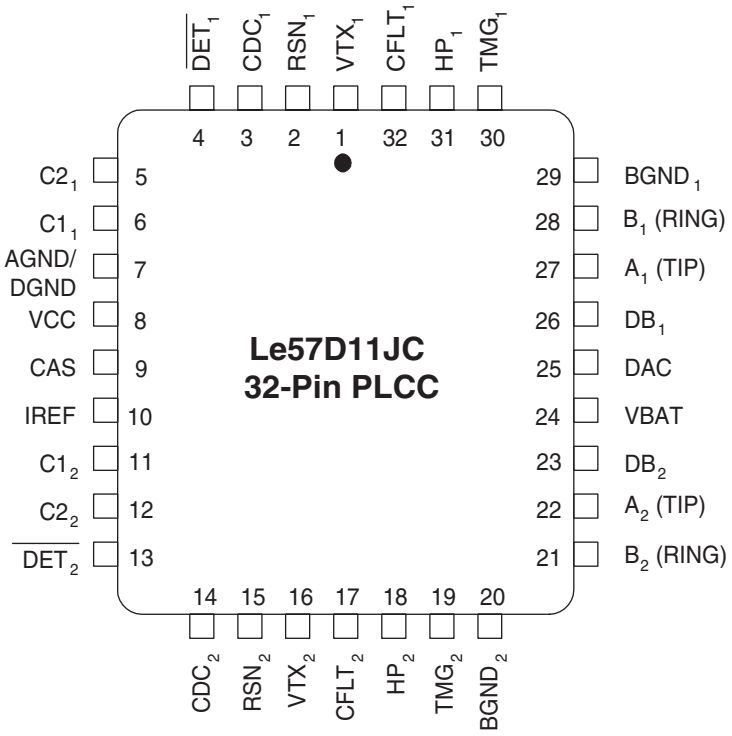
Off-Hook Detector

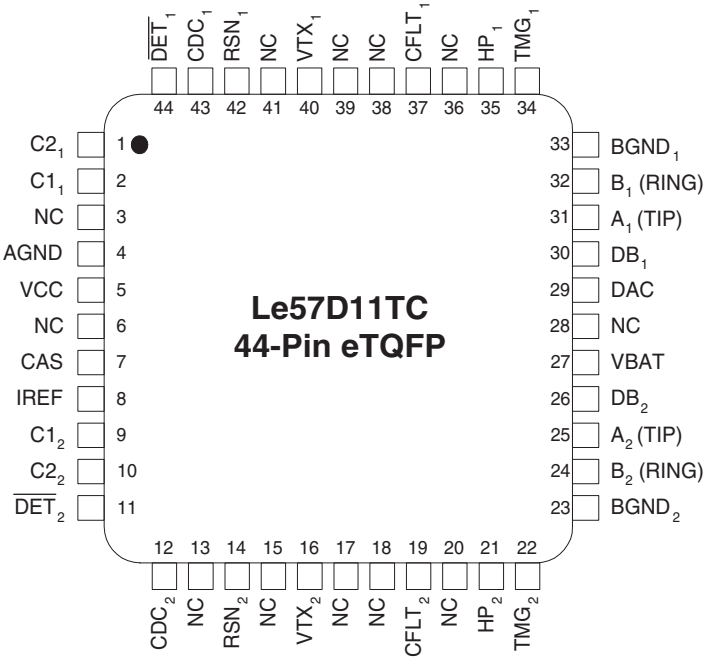
The most important loop monitoring function is off-hook detection. Loop current is programmed for both channels by a single resistor. Loop detect threshold is typically 1/3 of the programmed Loop current in the Active and Reverse Polarity states.

Ring-Trip Detector

In the Disconnect state, the ring-trip detector is active. While the DB_i pin is more negative than the DAC pin, the $\overline{DET}$ pin will be high to indicate on hook. When an off hook condition occurs, the DB_i pin becomes more positive than the DAC pin, and the $\overline{DET}$ pin will go low to indicate off hook during ringing (ring-trip) has been detected. The system implements the Ringing state using external control of a ring relay in combination with the Disconnect SLIC state, which enables the ring-trip detector.

CONNECTION DIAGRAMS





Note:

1. *Pin 1 is marked for orientation.*
2. *NC = No Connect*
3. *e = exposed pad*

PIN DESCRIPTIONS

Pin Name	Type	Description
A_1 (TIP)	Input/Output	Output of A (TIP) power amplifier of channel 1.
A_2 (TIP)	Input/Output	Output of A (TIP) power amplifier of channel 2.
AGND	Ground	Analog and digital ground.
B_1 (RING)	Input/Output	Output of B (RING) power amplifier of channel 1.
B_2 (RING)	Input/Output	Output of B (RING) power amplifier of channel 2.
$BGND_1$	Ground	Battery (power) ground of channel 1
$BGND_2$	Ground	Battery (power) ground of channel 2.
$C1_1$	Input	State decoder inputs of channel 1.
$C2_1$	Input	
$C1_2$	Input	State decoder inputs of channel 2.
$C2_2$	Input	
CAS	Capacitor	Pin for capacitor to filter reference voltage when operating in anti-saturation region.
CDC_1	Capacitor	DC feed filter capacitor and DC feed programming pin of channel 1.
CDC_2	Capacitor	DC feed filter capacitor and DC feed programming pin of channel 2.
$CFLT_1$	Input/Output	Fault detector output of channel 1. Connect a capacitor from $CFLT_1$ to AGND to set fault detector timing.
$CFLT_2$	Input/Output	Fault detector output of channel 2. Connect a capacitor from $CFLT_2$ to AGND to set fault detector timing.
DAC	Input	Ring-trip negative of both channels. Negative input to ring-trip comparator.
DB_1	Input	Ring-trip positive of channel 1. Positive input to ring-trip comparator.
DB_2	Input	Ring-trip positive of channel 2. Positive input to ring-trip comparator.
$\overline{DET}_1$	Output	Switch-hook/Ring-trip detector output of channel1. Logic low indicates that a detector is tripped.
$\overline{DET}_2$	Output	Switch-hook/Ring-trip detector output of channel 2. Logic low indicates that a detector is tripped.
HP_1	Capacitor	Connect High-pass filter capacitor from HP_1 to B_1 (RING).
HP_2	Capacitor	Connect High-pass filter capacitor from HP_2 to B_2 (RING).
IREF	Resistor	Connection for reference resistor that programs loop detector threshold and DC feed current of both channels.
RSN_1	Input	Receive Summing Node of channel 1. The metallic current (both AC and DC) between A_1 (TIP) and B_1 (RING) is equal to 500 times the current into this pin. The networks that program receive gain and two-wire impedance of channel 1 connect to this node.
RSN_2	Input	Receive Summing Node of channel 2. The metallic current (both AC and DC) between A_2 (TIP) and B_2 (RING) is equal to 500 times the current into this pin. The networks that program receive gain and two-wire impedance of channel 2 connect to this node.
TMG_1	Output	Thermal management of channel 1. External resistor connects from TMG_1 to VBAT to offload power from the SLIC device.
TMG_2	Output	Thermal management of channel 2. External resistor connects from TMG2 to VBAT to offload power from the SLIC device.
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VTX_1	Output	Transmit audio signal of channel 1. This output is a scaled version of the A and B metallic voltage. VTX also sources the two-wire input impedance programming network.
VTX_2	Output	Transmit audio signal of channel 2. This output is a scaled version of the A and B metallic voltage. VTX_2 also sources the two-wire input impedance programming network.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability

Storage temperature	–55 to +150º C
V_{CC} with respect to AGND	–0.4 to +7.0 V
V_{BAT} with respect to AGND: Continuous 10 ms	 +0.4 to –70 V +0.4 to –75 V
$BGND_1$, $BGND_2$ with respect to AGND	+3 to –3 V
A_1 (TIP), A_2 (TIP), B_1 (RING), B_2 (RING) to BGND: Continuous 10 ms (F = 0.1 Hz) 1 µs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	 V_{BAT} to + 1 V –70 to +5 V –80 to +8 V –90 to +12 V
Current from A_1 (TIP), A_2 (TIP), B_1 (RING), B_2 (RING)	±150 mA
DB_1, DB_2, and DAC inputs: Voltage on ring-trip inputs	 V_{BAT} to 0 V
Current into ring-trip inputs	±10 mA
$C1_1$, $C2_1$, $C1_2$, $C2_2$, $CFLT_1$, $CFLT_2$ Input Voltage	 –0.4 to V_{CC} + 0.4 V
Maximum power dissipation, continuous: T_A = 70º C, No heat sink (see note) In 32-pin PLCC package In 44-pin eTQFP	 1.7 W 3.3 W
Thermal Data (Junction to Ambient): In 32-pin PLCC package In 44-pin eTQFP	θ_{JA} 43º C/W typ 22.7º C/W typ
Thermal Data (Junction to Case): In 32-pin PLCC package In 44-pin eTQFP	θ_{JC} 16º C/W typ 9.2º C/W typ
ESD immunity/pin (Human Body Model)	1.5 kV
ESD immunity/pin (Charge Device Model)	1 kV

Note:

1. *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165º C. The device should never see this temperature, and operation above 145º C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*
2. *Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

Operating Ranges

Legerity guarantees the performance of this device over commercial (0° to 70° C) and industrial (–40° to 85° C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	–40° to 85° C

Electrical Ranges

V_{CC}	4.75 to 5.25 V
V_{BAT}	–39 to –58 V
DB1, DB2, and DAC	V_{BAT} to –2 V
AGND	0 V
BGND1, BGND2 with respect to AGND	–100 to + 100 mV
Load resistance on VTX to ground	20 kΩ minimum

Note:

The operating ranges define those limits between which the functionality of the device is guaranteed.

SPECIFICATIONS

Transmission Performance

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
2-wire return loss	200 Hz to 3.4 kHz (See Figure 8)	26			dB	1, 4
Analog output (VTX) impedance			3	20	Ω	4
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.77			Vrms	2b
THD (Total Harmonic Distortion)	0 dBm		–64	–50	dB	5
	+7 dBm		–55	–40		
THD, On hook	0dBm, R_{LAC} = 600 Ω			–36	dB	5

Crosstalk Between Channels

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Crosstalk coupling loss	F = 200 Hz to 3.4 kHz		80		dB	4

Longitudinal Capability

(See Figure 7.)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz, 0° C to +70° C	48			dB	4
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal current per pin (A or B)	Active state (off hook)	8.5	20		mArms	8
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω/pin	
Idle Channel Noise	C-Message, R_L = 600 Ω		7	12	dBrnc	4
	Psophometric, 600 Ω		–83	–78	dBmP	

Insertion Loss and Balance Return Signal

(See Figure 5 and Figure 6.)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Gain accuracy, 4- to 2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	
Gain accuracy, 2- to 4-wire	0 dBm, 1 kHz	–9.64	–9.54	–9.44		
Gain accuracy, 4- to 2-wire	On hook	–0.35		+0.35		4
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz	–0.15		+0.15		
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.15		+0.15		
Gain tracking On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35		
Group delay	0 dBm, 1 kHz		4		µs	4, 7

Line Characteristics

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_L, Short Loops, Active state	R_{LDC} = 600 Ω	26.4	30	33.6	mA	
I_L, Long Loops, Active state	R_{LDC} = 1930 Ω, BAT = –42.75 V, T_A = 25°C	18	19			
I_L, Accuracy, Standby state	$I_L = \left(\frac{\lvert VBAT\rvert - 3V}{(R_L + 5K)}\right), T_A = 25°C$	$0.7I_L$	I_L	$1.3I_L$		
I_L, Loop current, Disconnect state	R_L = 0			100	µA	
VAB, Open Circuit voltage	V_{BAT} = –48 V	+38.3	+40.3		V	

Power Supply Rejection Ratio, Active Normal State

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{CC}	50 Hz to 3.4 kHzV_{RIPPLE} = 100 mV_{rms}	30	40		dB	5
V_{BAT}	50 Hz to 3.4 kHzV_{RIPPLE} = 500 mV_{PP}	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4

Power Dissipation

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
On hook, Standby state (both Stdby)			40	100	mW	
On hook, Active state (Active)			200	400		
Off hook, Active state (Active)	R_L = 300 Ω, R_{TMG} = 1600 Ω		1400	2000		
One channel, Active/ One channel, Stdby	R_L = 300 Ω, R_{TMG} = 1600 Ω		720	1050		

Supply Currents

Battery = – 48 V

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_{CC}, On-hook V_{CC} supply current	Standby state (both Stdby)		4.4		mA	
	Active state, BAT = –48 V (both active)		12.6			
I_{BAT}, On-hook V_{BAT} supply current	Standby state (both Stdby)		0.4			
	Active state, BAT = –48 V (both active)		5.6			

RFI Rejection

(See Figure 9.)

Description	Test Conditions	Min	Typ	Max	Unit	Note
VTX1 or VTX2	f = .01 MHz to 100 MHz HF gen output = 1.5 Vrms CAX = CBX = 33 nF			1	mVrms	4
	CAX = CBX = 2.2 nF			3		

Logic Inputs

(Applies to C11, C12, C21, and C22.)

Description	Test Conditions	Min	Typ	Max	Unit	Note
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				

Logic Output

(Applies to $\overline{DET1}$, $\overline{DET2}$, CFLT1, and CFLT2.)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				

Ring-Trip Detector Input

(Applies to DAC, DB1, and DB2.)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Bias Current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6

CFLT1, CFLT2

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Sinking Current (ITrigger)			60		µA	
Sourcing Current (IRelease)			10			

CFLT Toggle Range

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Vth1			3.0	3.3	V	
Vth2			0.8	1.1		

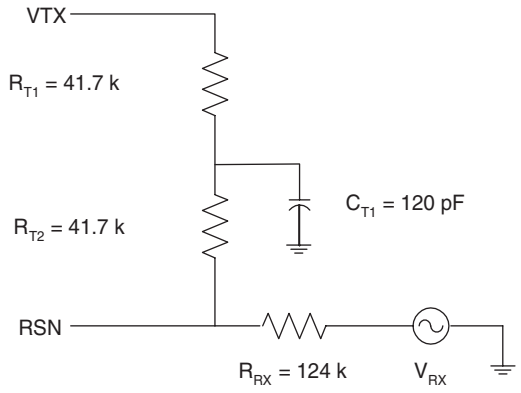
Loop Detector

Description		Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Off-hook threshold	Active		9		11	mA	
On-hook threshold	Active		8.5		10.5		
Off-hook threshold	Standby		4		6		
On-hook threshold	Standby		3.8		5.8		
Hysteresis			0		2		

Note:

1. *Unless otherwise noted, test conditions are BAT = –52 V; V_{CC} = +5 V; R_{L1}, R_{L2}= 600 Ω; R_{TMG1}, R_{TMG2} = 1600 Ω; no fuse resistors; C_{HP1}, C_{HP2}= 100 nF; C_{DC1},C_{DC2}= 1.5 µF; C_{CAS} = 0.33 µF; R_{REF}=15 K; two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*

Figure 3. AC Input Impedance Programming Network



2. *a. Z when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*

SLIC Decoding

(For X, Channel = 1 or 2)

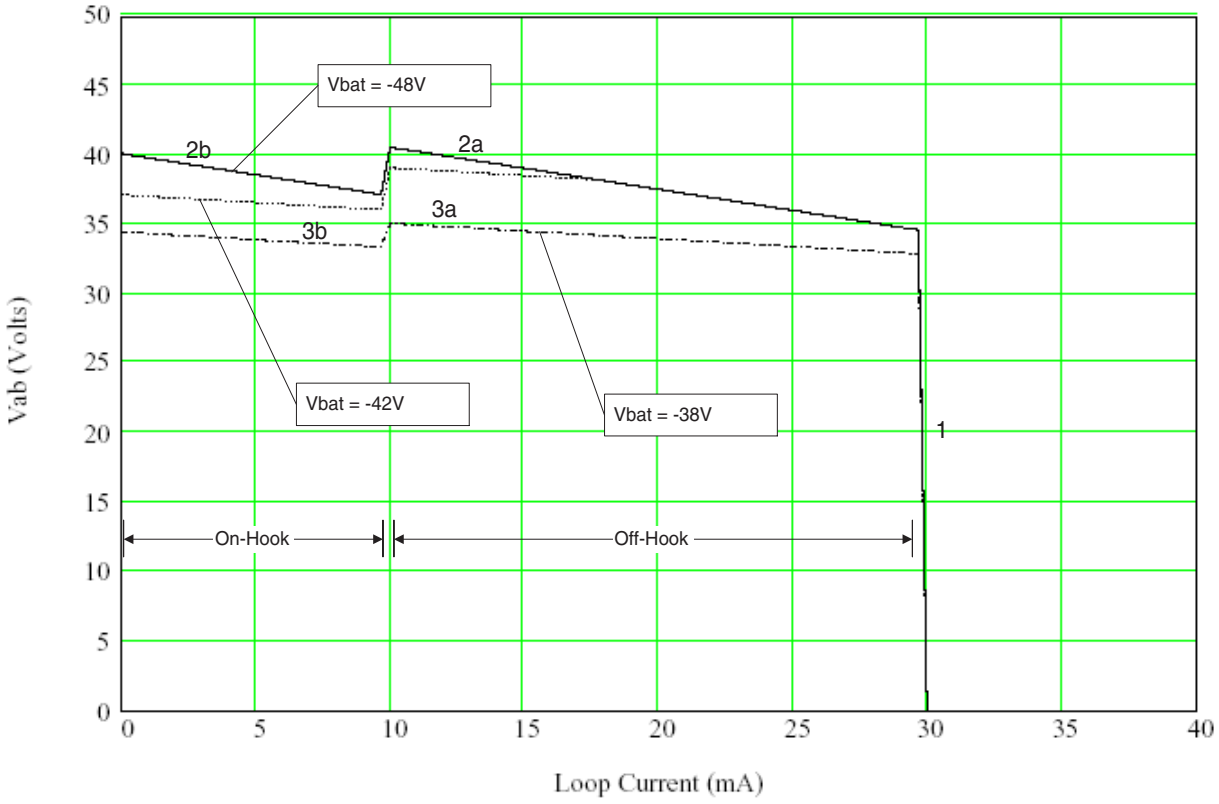
State	C2x	C1x	Two-Wire Status	$\overline{\text{DETx}}$ output
0	0	0	Disconnect	Ring-Trip Detector
1	0	1	Active	Loop Detector
2	1	1	Polarity Reversed	Loop Detector
3	1	0	Standby	Loop Detector

User-Programmable Components

$Z_T = 166.7(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 166.7(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{REF} = \frac{450}{I_{LOOP}}$ $C_{DC} = 1.5\ \mu F$	I_{LOOP} is the desired loop current in the constant-current region. Loop detect threshold is typically 1/3 of programmed Loop current.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{\lvert V_{BAT} \rvert - 3\ V}{5000\Omega + R_L}$	Standby loop current (resistive region).
Thermal Management Equations (Normal, Active, and Polarity Reverse States)	
$R_{TMG} \geq \left(\frac{\lvert V_{BAT} \rvert - 6\ V}{I_{LOOP}} - 70\ \Omega \right)$	R_{TMG} is connected from TMG to VBAT and limits power within the SLIC in Active and Off-Hook states.
$P_{RTMG} = \frac{(\lvert V_{BAT} \rvert - 6\ V - (I_L \bullet R_L))^2}{(R_{TMG} + 70\ \Omega)^2} \bullet R_{TMG}$	Power dissipated in the TMG resistor, R_{TMG} during Active and Off-Hook states.
$P_{SLIC} = \lvert V_{BAT} \rvert \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in Active state.

DC Feed Characteristics

Load Line (Typical)



R_{FEED} = 26.7K Internal $\quad I_{SWTH} = \frac{150}{R_{REF}} \quad R_{REF}$ = 15 K

Note:

1. *Constant current region:* $V_{AB1} = I_L R_L' = \frac{(450)}{R_{REF}} R_L'$, where $R_L' = R_L + 2R_F$

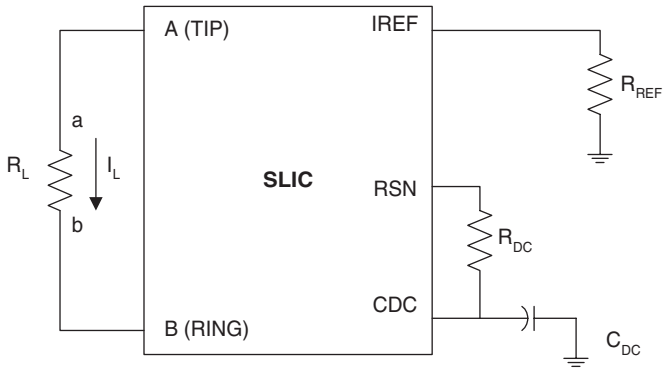
2a. *Battery-independent anti-sat (Off-hook):* $V_{AB2a} = 43.6\ V - I_L \frac{R_{FEED}}{88}$

2b. *Battery tracking anti-sat (On-hook):* $V_{AB2b} = V_{AB2a} - 3.5$

3a. *Battery tracking anti-sat (Off-hook):* $V_{AB3a} = |V_{BAT}| - 1.8 - I_L \frac{R_{FEED}}{240}$

3b. *Battery tracking anti-sat (On-hook):* $V_{AB3b} = V_{AB3a} - 0.33 \cdot |V_{BAT}| + 10.8$

Figure 4. Feed Programming



Note:

To choose the correct value for R_{DC}, please contact the manufacturer.

Test Circuits

Figure 5. Two-to-Four Wire Insertion Loss

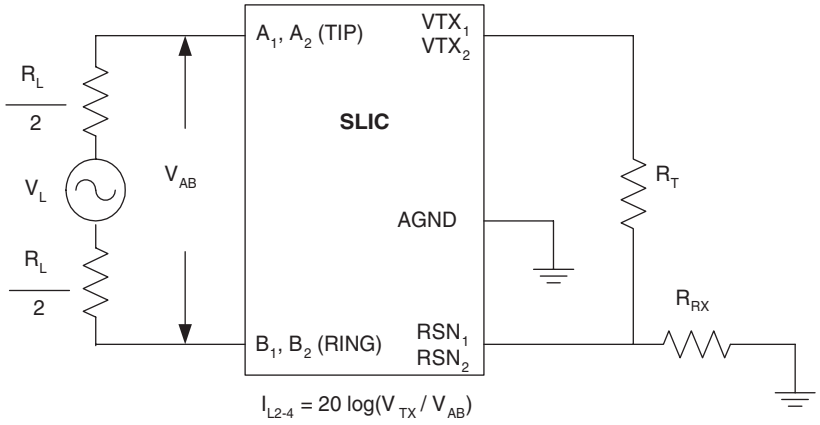


Figure 6. Four-to-Two Wire Insertion Loss and Balance Return Signals

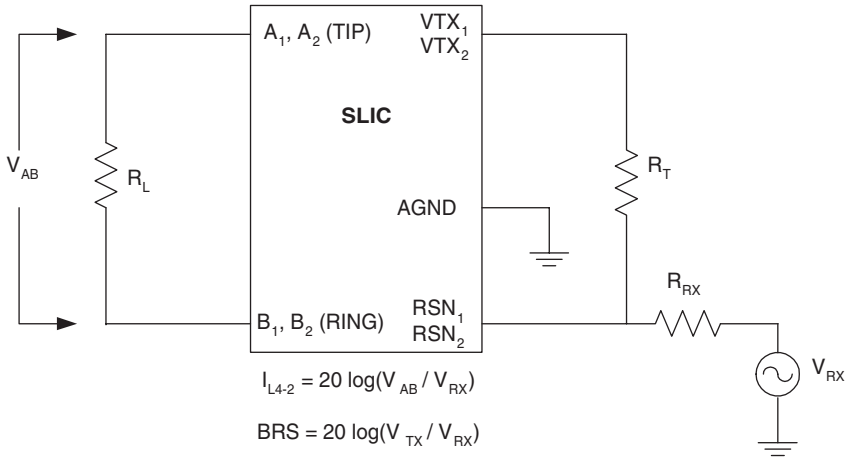


Figure 7. Longitudinal Balance

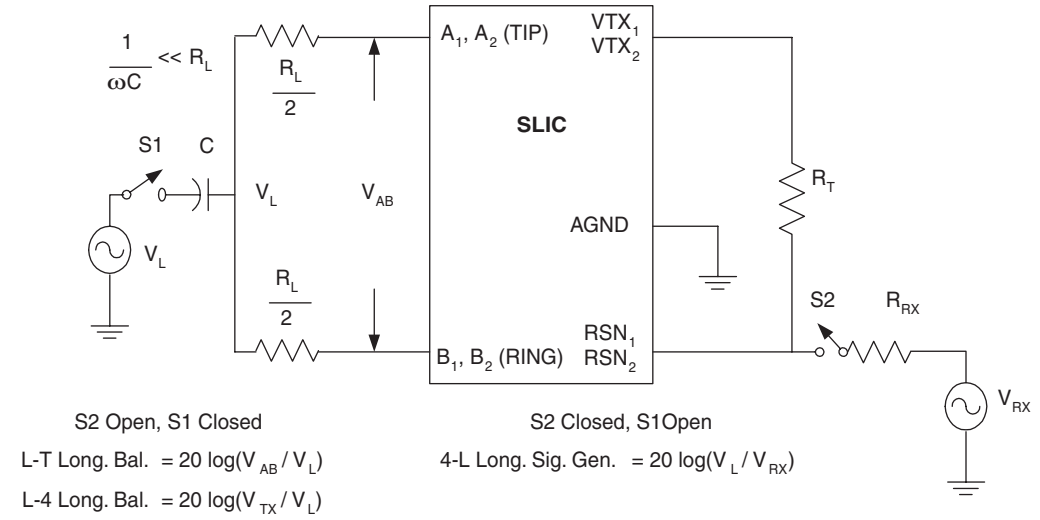


Figure 8. Two-Wire Return Loss Test Circuit

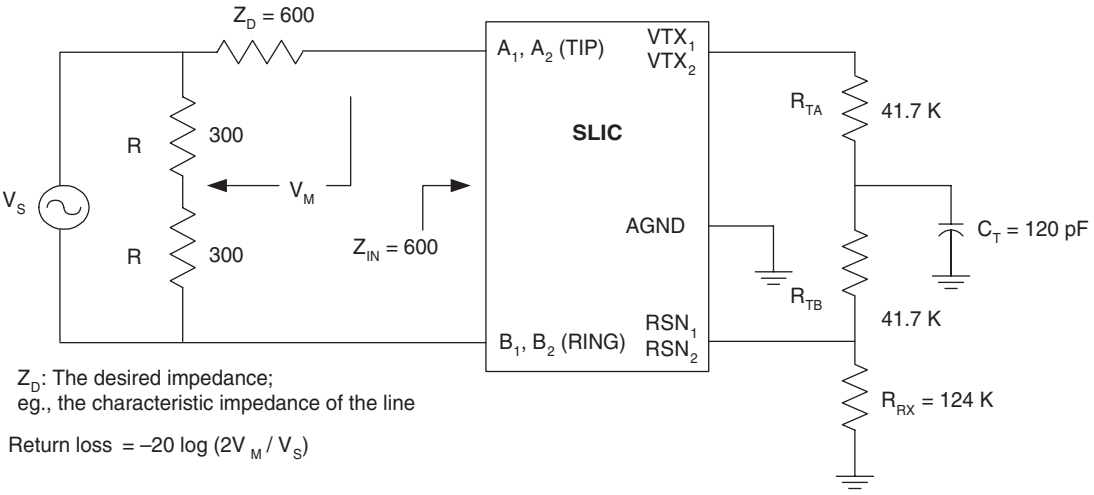


Figure 9. RFI Test Circuit

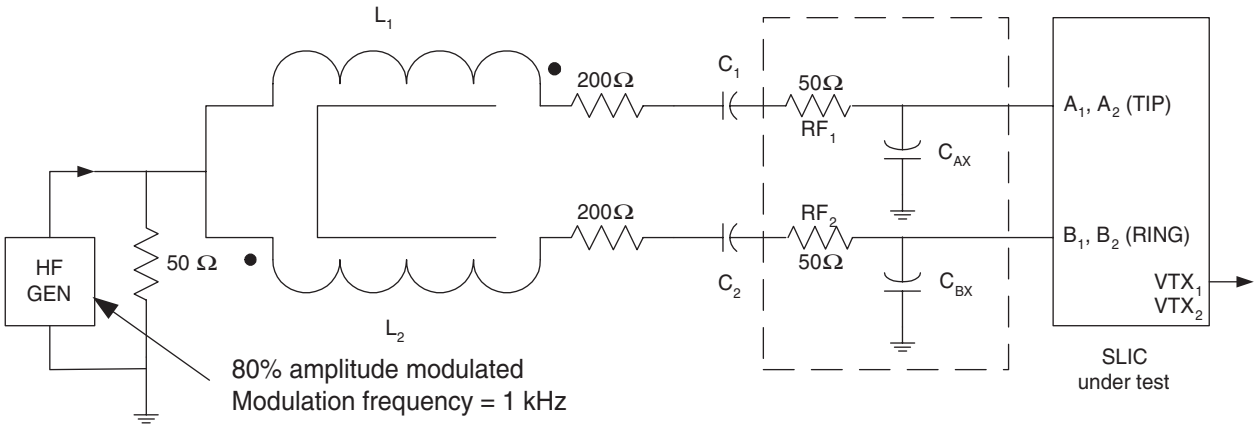
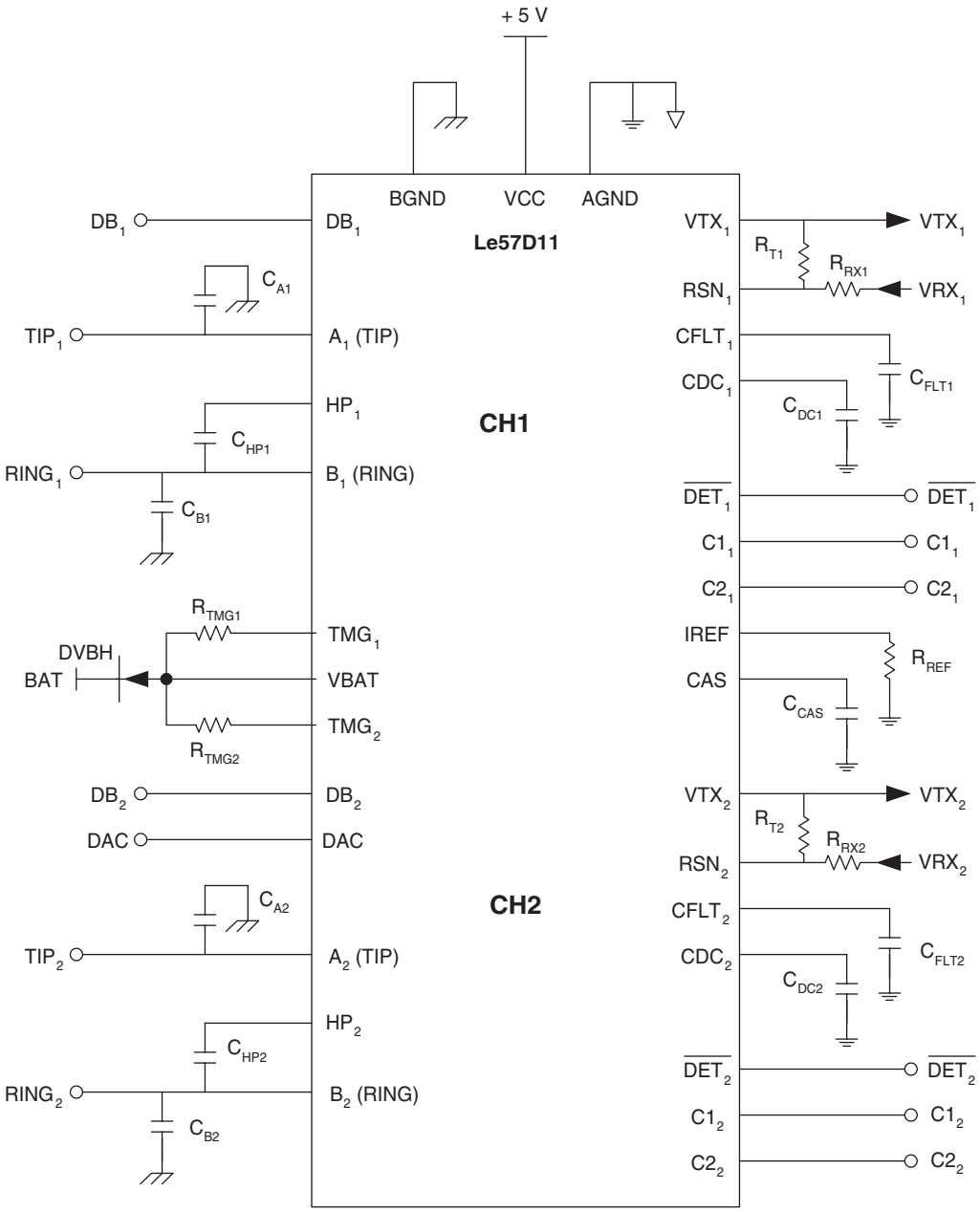
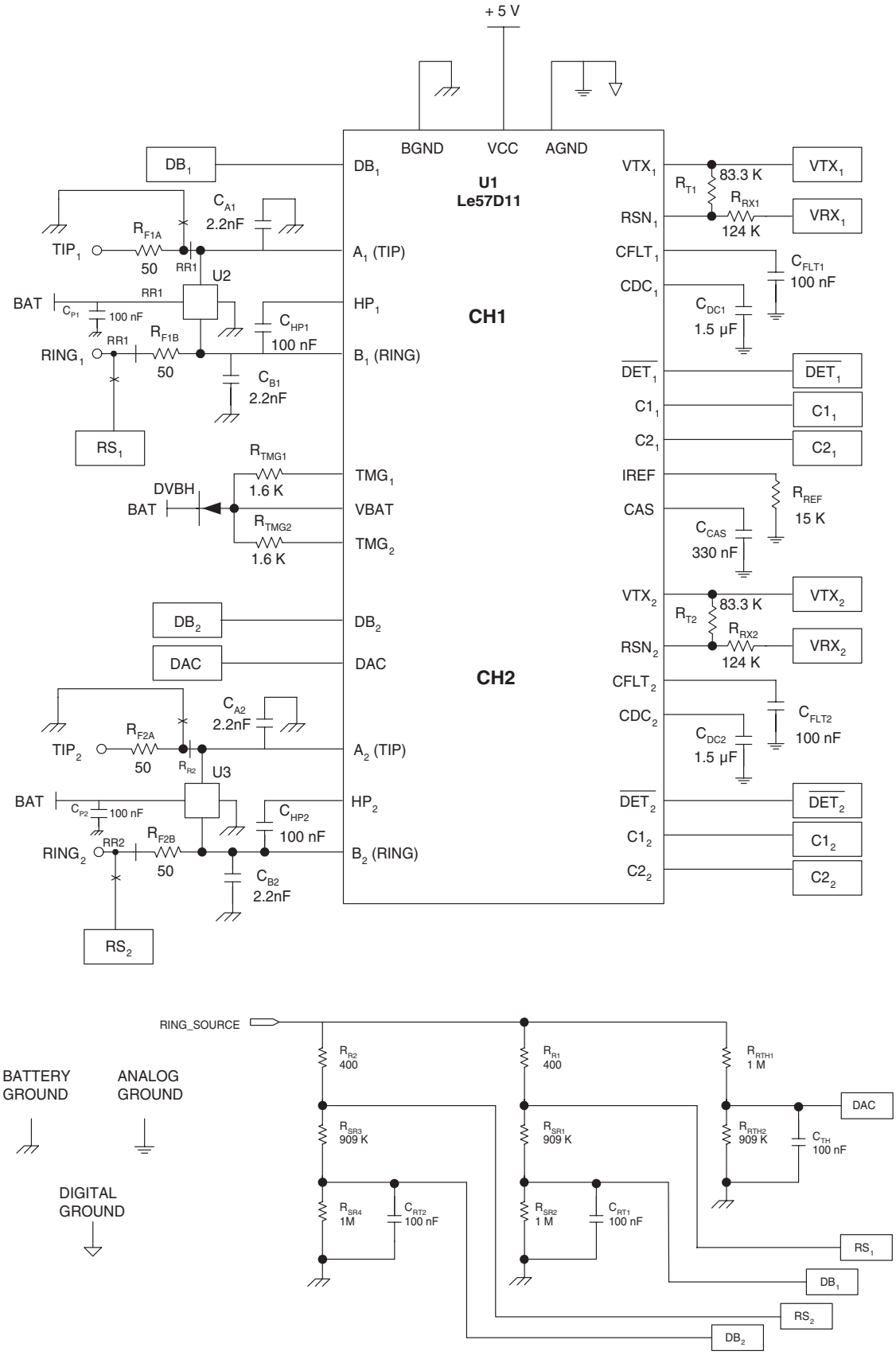


Figure 10. Le57D11 Test Circuit



APPLICATION CIRCUIT



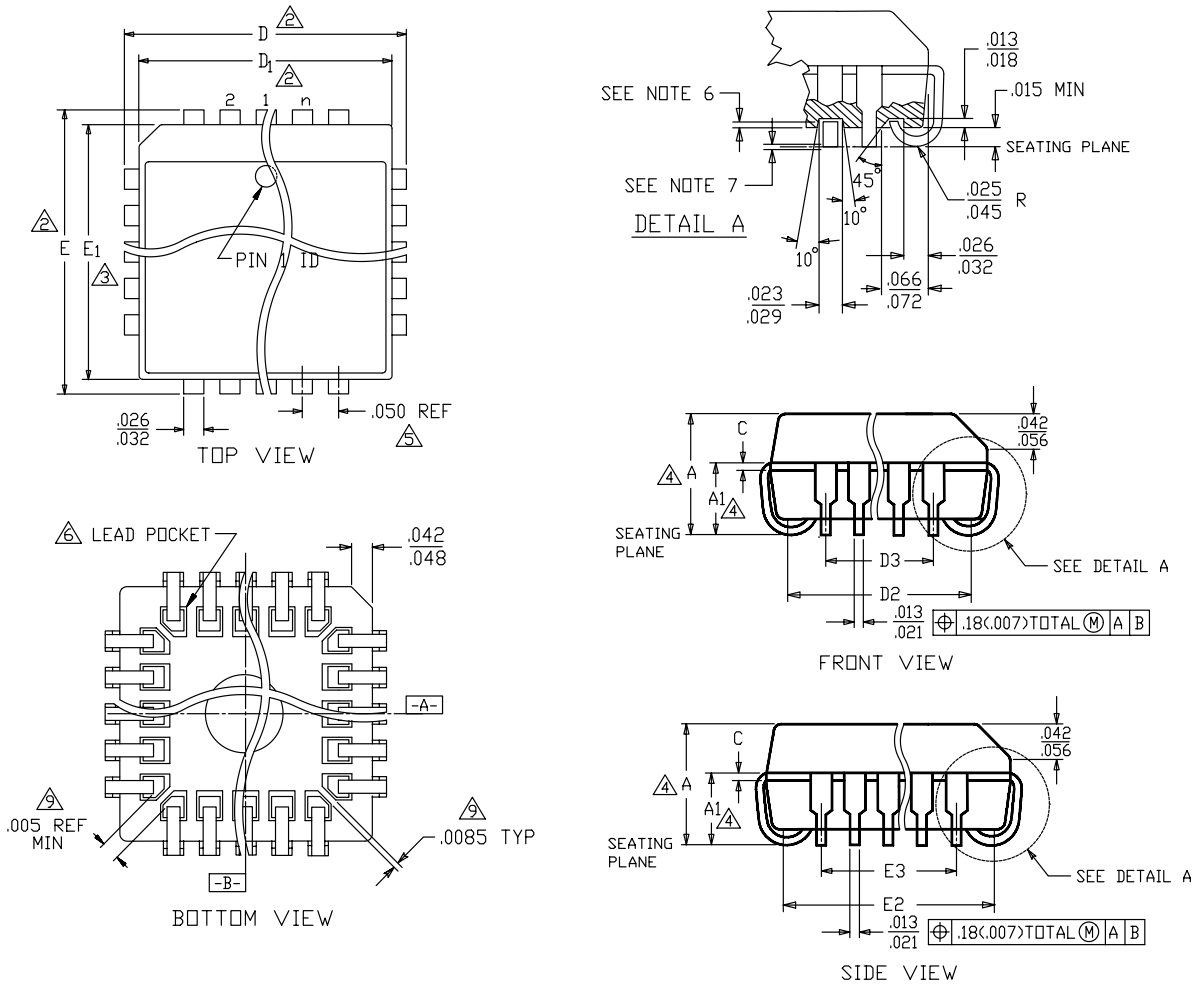
LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2).

Item	Quantity	Type	Value	Tol.	Rating	Comments	Note
C_{A1}, C_{B1}, C_{A2}, C_{B2}	4	Capacitor (X7R)	2200 pF	20%	100 V		
C_{HP1}, C_{HP2}, C_{P1}, C_{P2}, C_{RT1}, C_{RT2}, C_{TH}	7	Capacitor (X7R)	100 nF	20%	100 V		
C_{FLT1}, C_{FLT2}	2	Capacitor (X7R)	100 nF	20%	16 V		
C_{DC1}, C_{DC2}	2	Capacitor (X7R)	1.5 µF	10%	16 V		
R_{F1A}, R_{F1B}, R_{F2A}, R_{F2B}	2	Resistor Hybrid	50	1%			
R_{REF}	1	SMT	15 k	1%	1/10 W		
R_{T1}, R_{T2}	2	SMT	83.3 k	1%	1/10 W		
R_{RX1}, R_{RX2}	2	SMT	124 k	1%	1/10 W		
DVBH	1	MURS 120 (D0-41) DIODE					
R_{R1}, R_{R2}	2	Resistor Hybrid	400	1%			
U2, U3	2	TISP61089					
R_{RTH1}, R_{SR2}, R_{SR4}	3	SMT	1 M	1%	1/4 W		
R_{SR1}, R_{SR3}, R_{RTH2}	3	SMT	909 k	1%	1/4 W		
U1	1	Le57D11					
R_{TMG1} R_{TMG2}	2	SMT	1.6 k	1%	2 W		
C_{CAS}	1	Capacitor (X7R)	330 nF	20%	50 V		

PHYSICAL DIMENSIONS

PL032



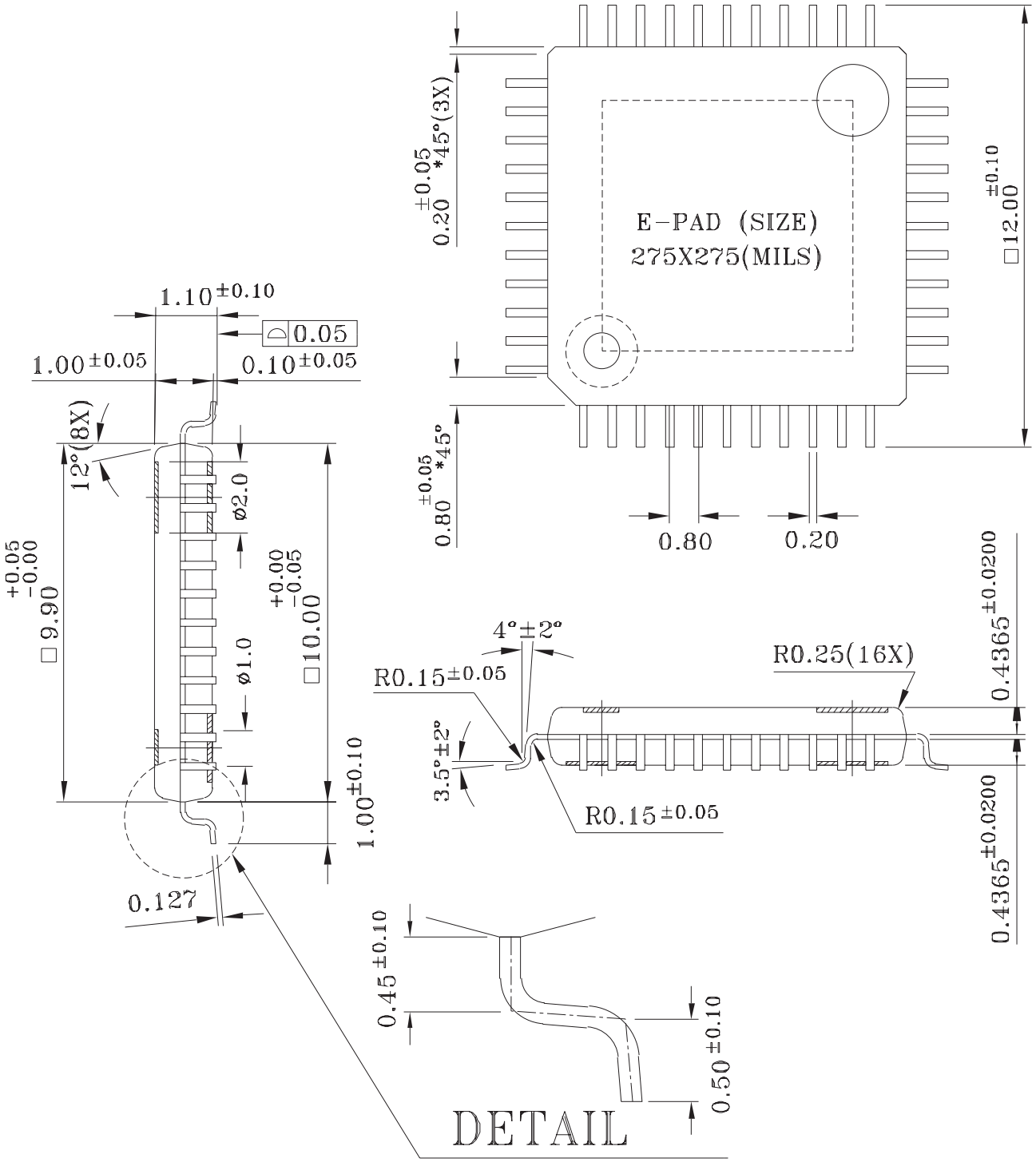
PACKAGE	PL 032	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

NOTES:

Dwg rev AH; 08/00

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005".
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

eTQFP


E-PAD (SIZE)
275X275(MILS)
0.80
0.20
DETAIL
R0.15±0.05
R0.25(16X)
4°±2°
3.5°±2°
12°(8X)
1.10±0.10
0.05
1.00±0.05
0.10±0.05
ø2.0
ø1.0
□9.90
□10.00
1.00±0.10
0.127
0.45±0.10
0.50±0.10
0.4365±0.0200
0.4365±0.0200
□12.00±0.10

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