LF3330
Vertical Digital Image Filter

FEATURES

- 83 MHz Data Rate
- 12-bit Data and Coefficients
- On-board Memory for 256 Coefficient Sets
- LF Interface™ Allows All 256 Coefficient Sets to be Updated Within Vertical Blanking
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Seven 3K x 12-bit, Programmable Two-Mode Line Buffers
- Separate Input Port for Odd and Even Field Filtering
- 8 Filter Taps
- Cascadable for More Filter Taps
- Supports Interleaved Data Streams
- 3.3 Volt Power Supply
- 5 Volt Tolerant I/O
- Available 100% Screened to MIL-STD-883, Class B

DESCRIPTION

The **LF3330** filters digital images in the vertical dimension at real-time video rates. The input and coefficient data are both 12 bits and in two's complement format. The output is also in two's complement format and may be rounded to 16 bits.

The filter is an 8-tap FIR filter with all required line buffers contained on-chip. The line buffers can store video lines with lengths from 4 to 3076 pixels.

Multiple LF3330s can be cascaded together to create larger vertical filters.

Due to the length of the line buffers, interleaved data can be fed directly into the device and filtered without separating the data into individual data streams. The number of interleaved data sets that the device can handle is limited only by the length of the on-chip line buffers. If the interleaved video line has 3076 data values or less, the filter can handle it.

The LF3330 contains enough on-board memory to store 256 coefficient sets. The LF Interface™ allows all 256 coefficient sets to be updated within vertical blanking.

Selectable 16-bit data output with user-defined rounding and limiting minimizes the constraints put on coefficient sets for various filter implementations.

LF3330 BLOCK DIAGRAM

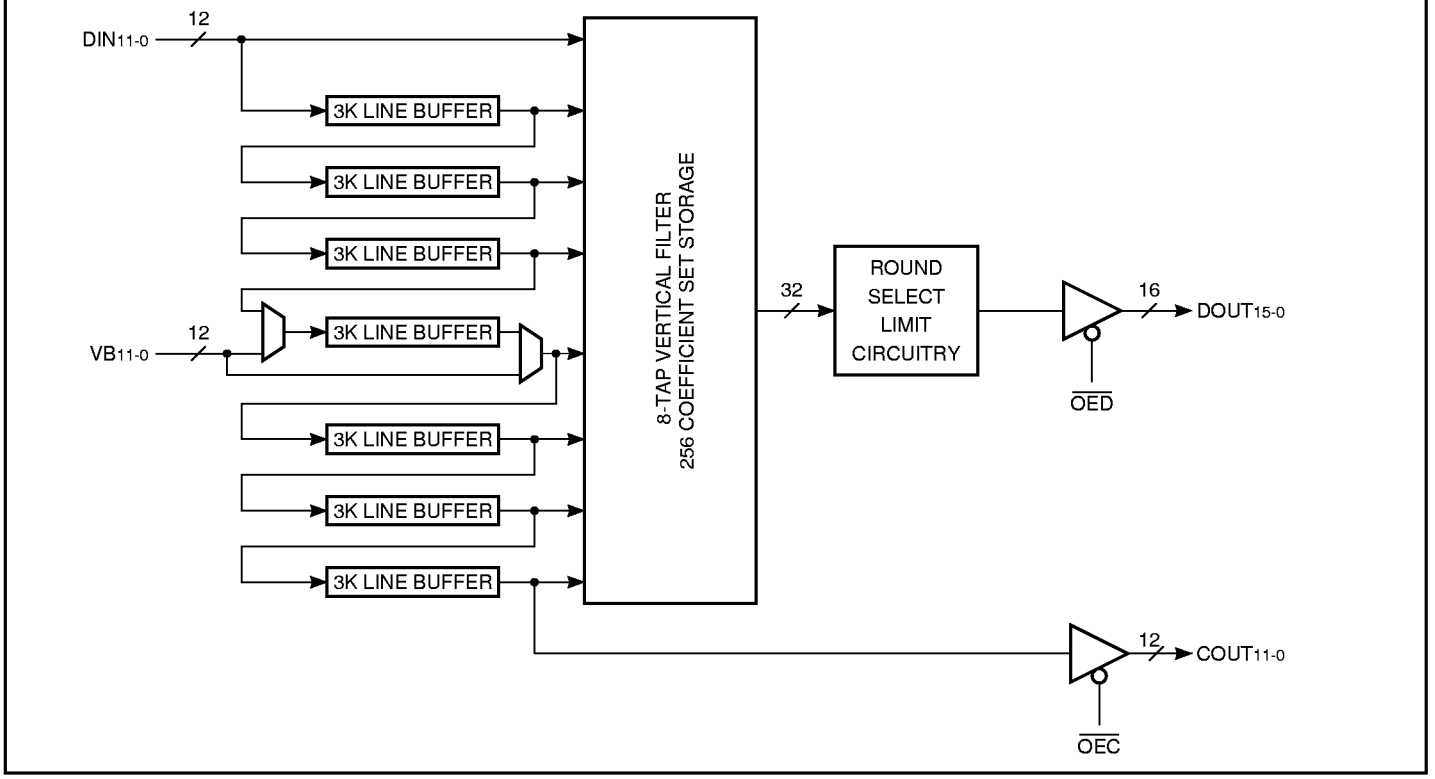

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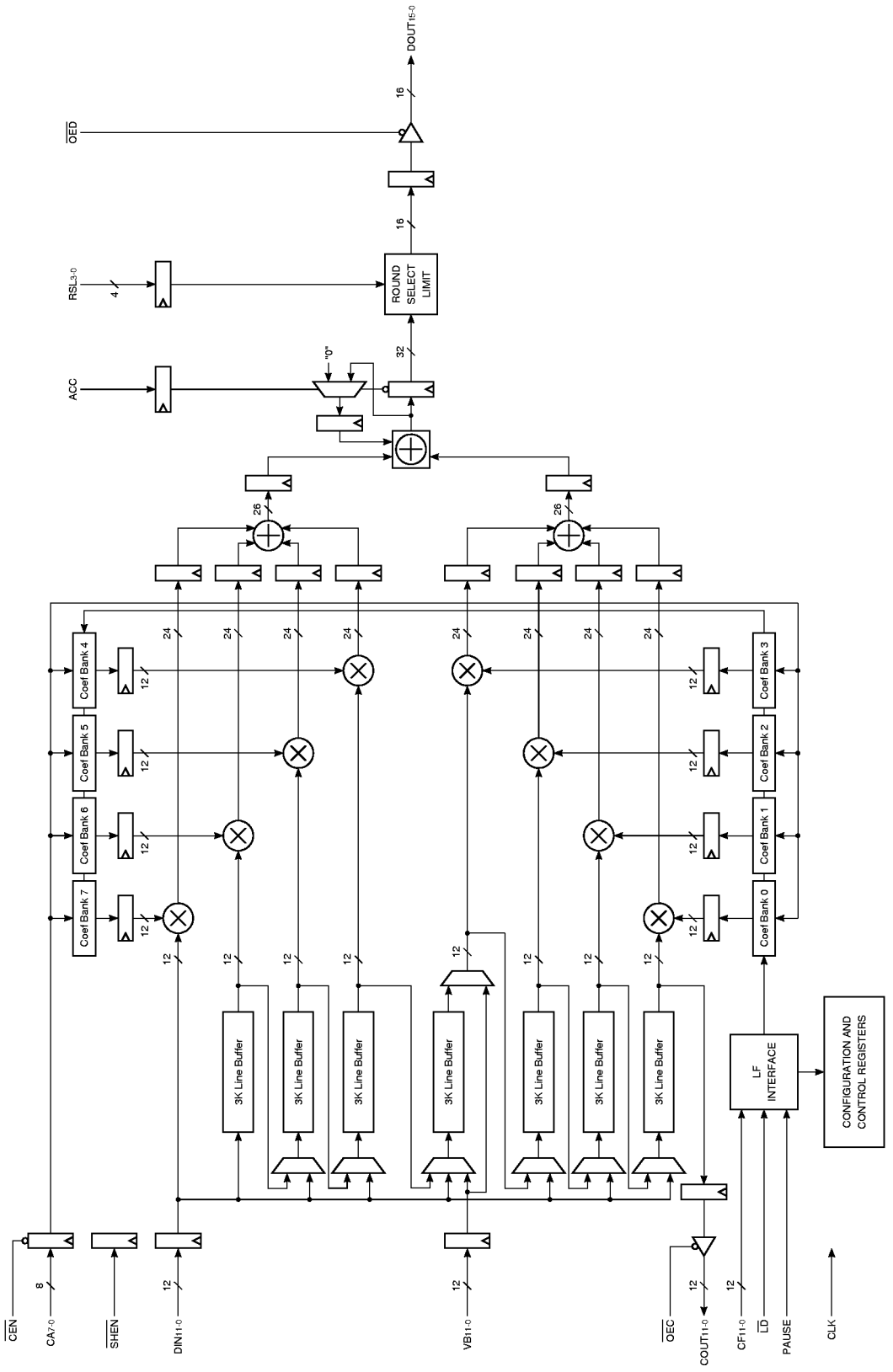
FIGURE 1. LF3330 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

DIN11-0 — Data Input

DIN11-0 is the 12-bit registered data input port. Data is latched on the rising edge of CLK.

VB11-0 — Field Filtering Data Input

VB11-0 is the 12-bit registered data input port used only when implementing Odd and Even Field Filtering (see Functional Description section for a full discussion). Data is latched on the rising edge of CLK.

CF11-0 — Coefficient Input

CF11-0 is used to load data into the coefficient banks and configuration/control registers. Data present on CF11-0 is latched into the LF Interface™ on the rising edge of CLK when LD is LOW (see the LF Interface™ section for a full discussion).

CA7-0 — Coefficient Address

CA7-0 determines which row of data in the coefficient banks is fed to the multipliers. CA7-0 is latched into the Coefficient Address Register on the rising edge of CLK when $\overline{CEN}$ is LOW.

Outputs

DOUT15-0 — Data Output

DOUT15-0 is the 16-bit registered data output port.

FIGURE 2. INPUT FORMATS

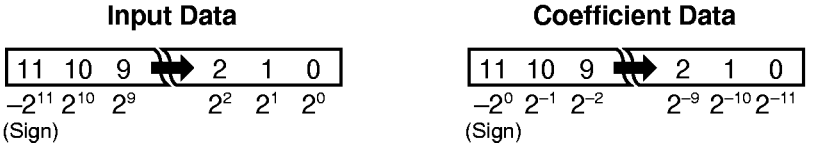


TABLE 1. OUTPUT FORMATS

SLCT4-0	S15	S14	S13	· · ·	S8	S7	· · ·	S2	S1	S0
00000	F15	F14	F13	· · ·	F8	F7	· · ·	F2	F1	F0
00001	F16	F15	F14	· · ·	F9	F8	· · ·	F3	F2	F1
00010	F17	F16	F15	· · ·	F10	F9	· · ·	F4	F3	F2
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
01110	F29	F28	F27	· · ·	F22	F21	· · ·	F16	F15	F14
01111	F30	F29	F28	· · ·	F23	F22	· · ·	F17	F16	F15
10000	F31	F30	F29	· · ·	F24	F23	· · ·	F18	F17	F16

COUT11-0 — Cascade Data Output

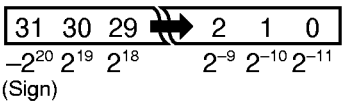
COUT11-0 is a 12-bit cascade output port. COUT11-0 on one device should be connected to DIN11-0 of another LF3330.

Controls

$\overline{LD}$ — Coefficient Load

When $\overline{LD}$ is LOW, data on CF11-0 is latched into the LF Interface™ on the rising edge of CLK. When $\overline{LD}$ is HIGH, data can not be latched into the LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{LD}$ is required in order for the input circuitry to function properly. Therefore, $\overline{LD}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

FIGURE 3. ACCUMULATOR FORMAT



PAUSE — LF Interface™ Pause

When PAUSE is HIGH, the LF Interface™ loading sequence is halted until PAUSE is returned to a LOW state. This effectively allows the user to load coefficients and control registers at a slower rate than the master clock (see the LF Interface™ section for a full discussion).

$\overline{CEN}$ — Coefficient Address Enable

When $\overline{CEN}$ is LOW, data on CA7-0 is latched into the Coefficient Address Register on the rising edge of CLK. When $\overline{CEN}$ is HIGH, data on CA7-0 is not latched and the register's contents will not be changed.

TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
11-0	Line Buffer Length	See Line Buffer Description Section

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
0	Line Buffer Mode	0 : Delay Mode 1 : Recirculate Mode
1	Line Buffer Load	0 : Normal Load 1 : Parallel Load
2	Odd and Even Field Filtering Port Enable	0 : VB Port Disabled 1 : VB Port Enabled
3	Odd and Even Field Filtering Line Buffer Enable	0 : VB Line Buffer Disabled 1 : VB Line Buffer Enabled
11-4	Reserved	Must be set to "0"

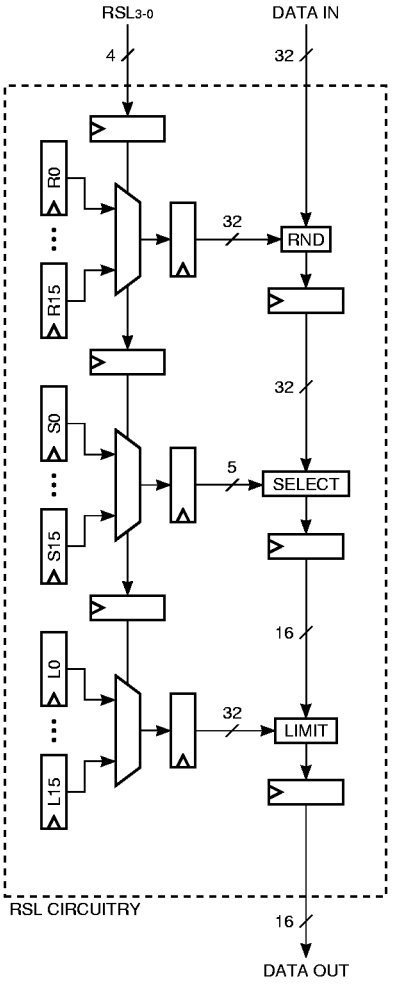
TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
0	Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
11-1	Reserved	Must be set to "0"

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0 : First Device 1 : Cascaded Device
11-1	Reserved	Must be set to "0"

FIGURE 4. RSL CIRCUITRY



ACC — Accumulator Control

When ACC is HIGH, the accumulator is enabled for accumulation and the accumulator output register is disabled for loading. When ACC is LOW, no accumulation is performed and the accumulator output register is enabled for loading. ACC is latched on the rising edge of CLK.

$\overline{SHEN}$ — Shift Enable

$\overline{SHEN}$ enables or disables the loading of data into the input/cascade registers and the line buffers. When $\overline{SHEN}$ is LOW, data is loaded into the input/cascade registers and shifted through the line buffers on the rising edge of CLK. When $\overline{SHEN}$ is HIGH, data can not be loaded into the input/cascade registers or shifted through the line buffers and their contents will not be changed.

RSL3-0 — Round/Select/Limit Control

RSL3-0 determines which of the sixteen user-programmable round/select/limit registers are used in the round/select/limit circuitry. A value of 0 on RSL3-0 selects round/select/limit register 0. A value of 1 selects round/select/limit register 1 and so on. RSL3-0 is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

$\overline{OED}$ — DOUT Output Enable

When $\overline{OED}$ is LOW, DOUT15-0 is enabled for output. When $\overline{OED}$ is HIGH, DOUT15-0 is placed in a high-impedance state.

$\overline{OEC}$ — COUT Output Enable

When $\overline{OEC}$ is LOW, COUT15-0 is enabled for output. When $\overline{OEC}$ is HIGH, COUT15-0 is placed in a high-impedance state.

FUNCTIONAL DESCRIPTION

Line Buffers

The maximum delay length of each line buffer is 3076 cycles and the minimum is 4 cycles. Configuration Register 0 (CR_0) determines the delay length of the line buffers. The line buffer length is equal to the value of CR_0 plus 4. A value of 0 for CR_0 sets the line buffer length to 4. A value of 3072 for CR_0 sets the line buffer length to 3076. Any values for CR_0 greater than 3072 are not valid.

The line buffers have two modes of operation: delay mode and recirculate mode. Bit 0 of Configuration Register 1 determines which mode the line buffers are in. In delay mode, the data input to the line buffer is delayed by an amount determined by CR_0. In recirculate mode, the output of the line buffer is routed back to the input of the line buffer allowing the line buffer contents to be read multiple times.

Bit 1 of Configuration Register 1 allows the line buffers to be loaded in parallel. When Bit 1 is "1", the input register (DIN_{11-0}) loads all seven line buffers in parallel. This allows all the line buffers to be preloaded with data in the amount of time it normally takes to load a single line buffer.

Odd and Even Field Filtering

The LF3330 is capable of odd and even field filtering. Bit 2 of Configuration Register 1 enables the VB Data Input port required for odd and even field filtering. Bit 3 of the same configuration register enables the line buffer in the VB Data path. Line buffer length is set to the length written to Configuration Register 0. If line buffer parallel load is enabled and odd and even field filtering is enabled, the data for the VB line buffer comes from the VB Data Input port.

Interleaved Data

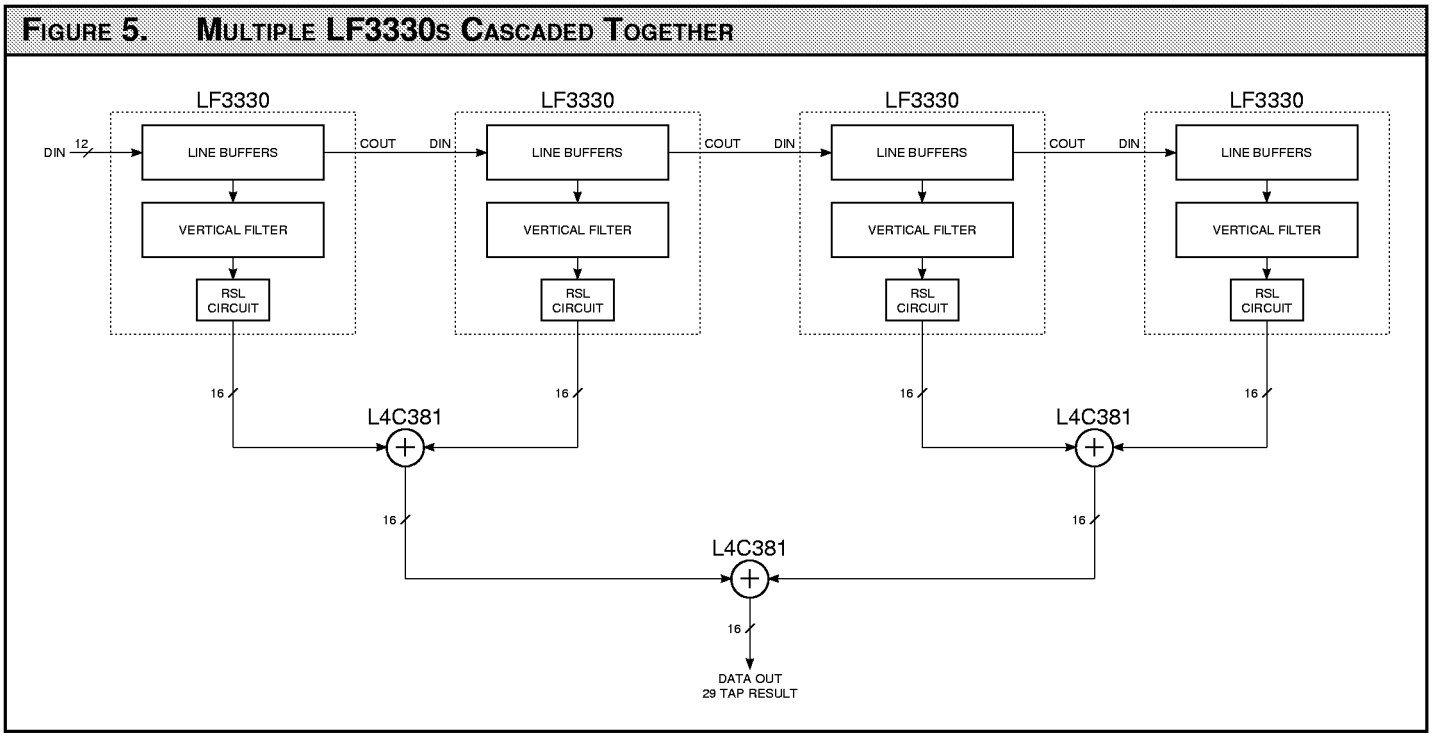
The LF3330 is capable of handling interleaved data. The number of data sets it can handle is determined by the number of data values contained in a video line. If the interleaved video line has 3076 data values or less, the LF3330 can handle it no matter how many data sets are interleaved together.

Cascading

A cascade port is provided to allow cascading of multiple devices for more filter taps (see Figure 5). $COUT_{11-0}$ of one device should be connected to DIN_{11-0} of another device. As many LF3330s as desired may be cascaded together. However, the outputs of the LF3330s must be added together with external adders.

The first line buffer on a cascaded device must have its length shortened by two delays. This is to account for the added delays of the input register on the device and the cascade output register from the previous LF3330. If Bit 0 of Configuration Register 3 is set to "1", the length of the first line buffer will be reduced by two. This will make its effective length the same as the other line buffers on the device. If Bit 0 of Configuration Register 3 is set to "0", the length of the first line buffer will be the same as the other line buffers. When cascading devices, the first LF3330 should have Bit 0 of Configuration Register

FIGURE 5. MULTIPLE LF3330S CASCADED TOGETHER



3 set to "0". Any LF3330s cascaded after the first LF3330 should have Bit 0 of Configuration Register 3 set to "1". When not cascading, Bit 0 of Configuration Register 3 should be set to "0".

It is important to note that the first multiplier on all cascaded devices should not be used. This is because the first multiplier does not have a line buffer in front of it. The coefficient value sent to the first multiplier on a cascaded device should be "0".

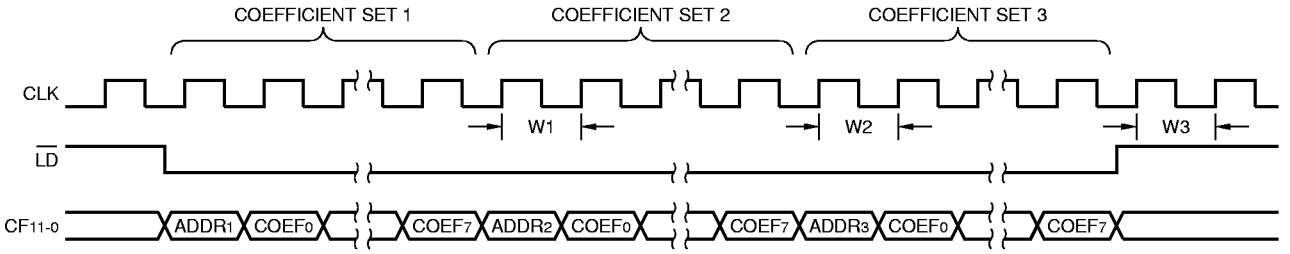
Rounding

The filter output may be rounded by adding the contents of one of the sixteen round registers to the filter output (see Figure 4). Each round register is 32 bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard half-LSB rounding. RSL3-0 determines which of the sixteen round registers are used in the rounding operation. A value of 0 on RSL3-0 selects round register 0. A value of 1 selects round register 1 and so on. RSL3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data. If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

Output Select

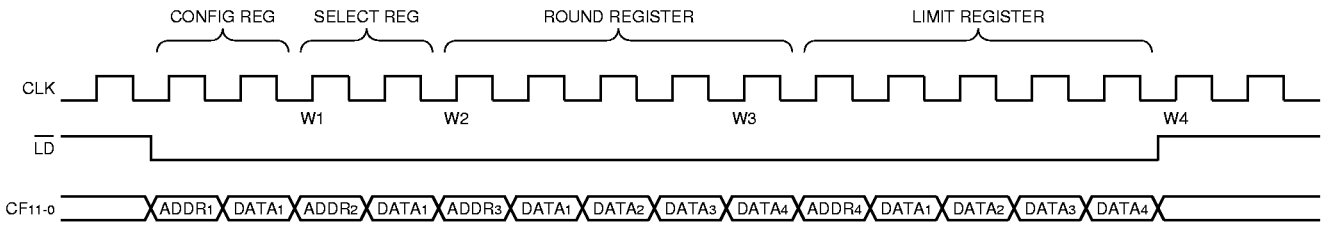
The word width of the filter output is 32 bits. However, only 16 bits may be sent to DOUT15-0. The select circuitry determines which 16 bits are passed (see Table 1). There are sixteen select registers which control the select circuitry. Each select register is 5 bits wide and user-programmable. RSL3-0 determines which of the sixteen select registers are used in the select circuitry. Select register 0 is chosen by loading a 0 on RSL3-0. Select register 1 is chosen by loading a 1 on RSL3-0 and so on. RSL3-0 may be changed every clock cycle if desired. This allows the 16-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

FIGURE 6. COEFFICIENT BANK LOADING SEQUENCE



W1: Coefficient Set 1 written to coefficient banks during this clock cycle.
W2: Coefficient Set 2 written to coefficient banks during this clock cycle.
W3: Coefficient Set 3 written to coefficient banks during this clock cycle.

FIGURE 7. CONFIGURATION/CONTROL REGISTER LOADING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.
W3: Round Register loaded with new data on this rising clock edge.
W4: Limit Register loaded with new data on this rising clock edge.

Limiting

An output limiting function is provided for the output of the filter. The limit registers determine the valid range of output values when limiting is enabled (Bit 0 in Configuration Register 2). There are sixteen 32-bit limit registers. RSL3-0 determines which limit register is used during the limit operation. A value of 0 on RSL3-0 selects limit register 0. A value of 1 selects limit register 1 and so on. Each limit register contains both an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. RSL3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Coefficient Banks

The coefficient banks store the coefficients which feed into the multipliers in the filter. There is a separate bank for each multiplier. Each bank can hold 256 12-bit coefficients. The banks are loaded using the LF Interface™. Coefficient bank loading is discussed in the LF Interface™ section.

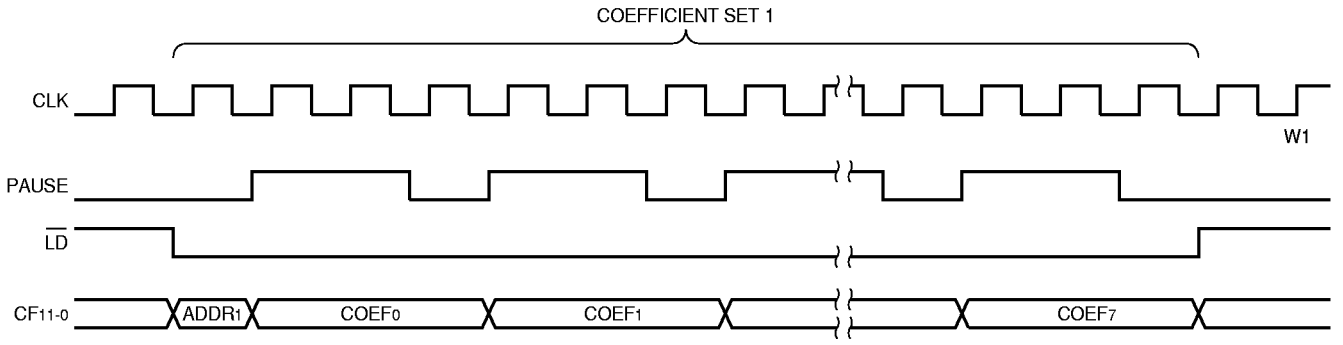
Configuration and Control Registers

The configuration registers determine how the LF3330 operates. Tables 2 through 5 show the formats of the four configuration registers. There are three types of control registers: round, select, and limit. There are sixteen round registers. Each round register is 32 bits wide. RSL3-0 determines which round register is used for rounding.

There are sixteen select registers. Each select register is 5 bits wide. RSL3-0 determines which select register is used for the select circuitry.

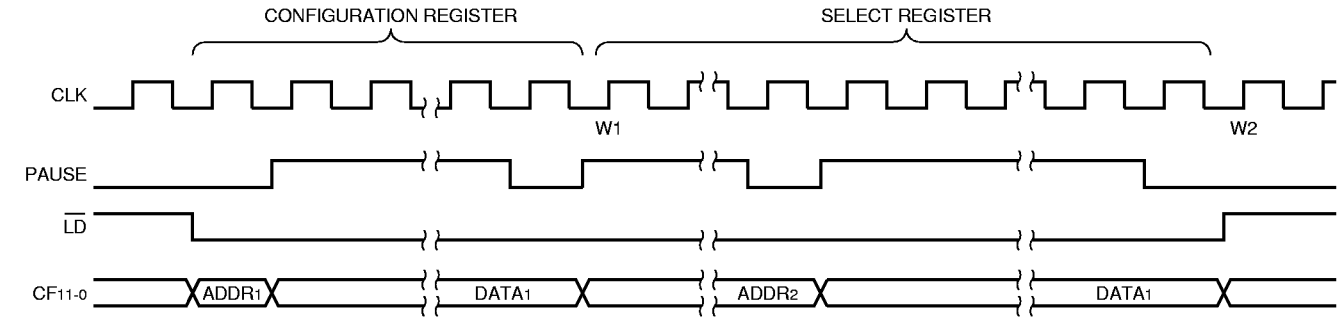
There are sixteen limit registers. Each limit register is 32 bits wide and stores both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper

FIGURE 8. COEFFICIENT BANK LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Configuration Register loaded with new data on this rising clock edge.

FIGURE 9. CONFIGURATION AND SELECT REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



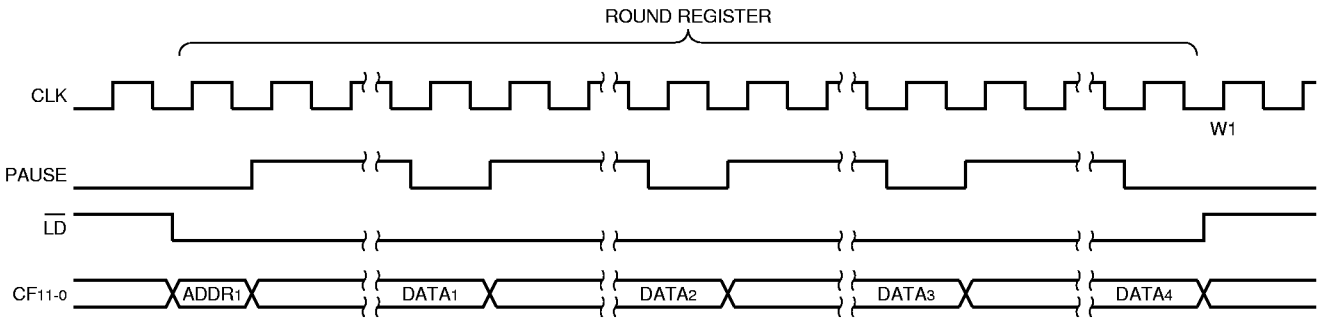
W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.

limit is stored in bits 31-16. RSL3-0 determines which limit register is used for limiting when limiting is enabled. Configuration and control register loading is discussed in the LF Interface™ section.

LF Interface™

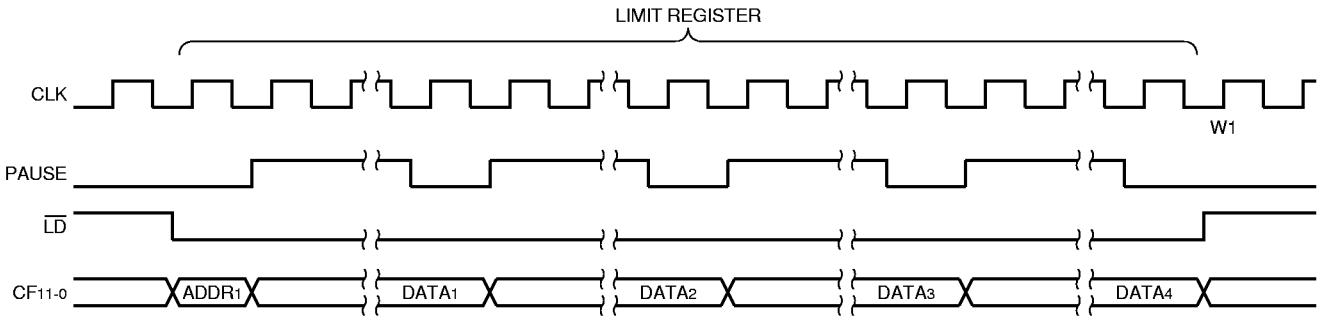
The LF Interface™ is used to load data into the coefficient banks and configuration/control registers. $\overline{LD}$ is used to enable and disable the LF Interface™. When $\overline{LD}$ goes LOW, the LF Interface™ is enabled for data input. The first value fed into the interface on CF11-0 is an address which determines what the interface is going to load. The three most

FIGURE 10. ROUND REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Round Register loaded with new data on this rising clock edge.

FIGURE 11. LIMIT REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Limit Register loaded with new data on this rising clock edge.

TABLE 10. COEFFICIENT BANK LOADING FORMAT

	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
1st Word - Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word - Bank 0	0	0	1	0	0	0	0	1	0	0	0	0
3rd Word - Bank 1	0	1	0	1	0	1	0	0	0	0	1	1
4th Word - Bank 2	1	1	0	0	0	1	1	1	0	1	1	0
5th Word - Bank 3	1	0	0	1	1	1	1	0	0	0	1	1
6th Word - Bank 4	0	1	1	1	0	0	0	0	0	0	0	1
7th Word - Bank 5	1	0	0	0	0	0	1	1	0	0	1	0
8th Word - Bank 6	1	1	1	1	0	0	1	0	0	0	0	0
9th Word - Bank 7	0	0	0	1	0	1	0	0	0	0	1	1

significant bits (CF11-9) determine if the LF Interface™ will load coefficient banks or configuration/control registers (see Table 6). The nine least significant bits (CF8-0) are the address for whatever is to be loaded (see Tables 7 through 9). For example, to load address 15 of the coefficient banks, the first data value into the LF Interface™ should be 00FH. To load limit register 10, the first data value should be E0AH. The first address value should be loaded into the interface on the same clock cycle that latches the HIGH to LOW transition of $\overline{LD}$ (see Figures 6 and 7).

The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the interface will expect eight values to be loaded into the device after the address value. The eight values are coefficients 0 through 7. When loading configuration or select registers, the interface will expect one value after the address value. When loading round or limit registers, the interface will expect four values after the address value. Figures 6 and 7 show the data loading sequences for the coefficient banks and configuration/control registers.

PAUSE allows the user to effectively slow the rate of data loading through the LF Interface™. When PAUSE is HIGH, the LF Interface™ is held until PAUSE is returned to a LOW. Figures 8 through 11 display the effects of PAUSE while leading coefficient and control data.

Table 10 shows an example of loading data into the coefficient banks. The following data values are written into address 10 of coefficient banks 0 through 7: 210H, 543H, C76H, 9E3H, 701H, 832H, F20H, 143H. Table 11 shows an example of loading data into a

Table 6. CF11-9 Decode

11	10	9	DESCRIPTION
0	0	0	Coefficient Banks
0	0	1	Configuration Registers
0	1	1	Select Registers
1	0	1	Round Registers
1	1	1	Limit Registers

Table 7. Round Registers

REGISTER	ADDRESS (HEX)
0	A00
1	A01
•	•
•	•
•	•
14	A0E
15	A0F

Table 8. Select Registers

REGISTER	ADDRESS (HEX)
0	600
1	601
•	•
•	•
•	•
14	60E
15	60F

Table 9. Limit Registers

REGISTER	ADDRESS (HEX)
0	E00
1	E01
•	•
•	•
•	•
14	E0E
15	E0F

Table 11. Configuration Register Loading Format

	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
1st Word - Address	0	0	1	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	0	0	1	1

Table 12. Round Register Loading Format

	CF11	CF10	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
1st Word - Address	1	0	1	0	0	0	0	0	1	1	0	0
2nd Word - Data	R	R	R	R	1	0	1	0	0	0	1	0*
3rd Word - Data	R	R	R	R	1	1	1	1	0	1	0	0
4th Word - Data	R	R	R	R	1	0	0	0	0	0	1	1
5th Word - Data	R	R	R	R	0**	1	1	1	0	1	1	0

R = Reserved. Must be set to "0".
* This bit represents the LSB of the Round Register.
** This bit represents the MSB of the Round Register.

configuration register. Data value 003H is written into Configuration Register 2. Table 12 shows an example of loading data into a round register. Data value 7683F4A2H is written into round register 12. Table 13 shows an example of loading data into a select register. Data value 00FH is loaded into select register 2. Table 14 shows an example of loading data into limit register 7. Data value 3B60H is loaded as the lower limit and 72A4H is loaded as the upper limit.

It takes 9S clock cycles to load S coefficient sets into the device. Therefore, it takes 2304 clock cycles to load all 256 coefficient sets. Assuming an 83 MHz clock rate, all 256 coefficient sets can be updated in less than 27.7 µs, which is well within vertical blanking time. It takes 5S clock cycles to load S round or limit registers. Therefore, it takes 160 clock cycles to update all round and limit registers. Assuming an 83 MHz clock rate, all round/limit registers can be updated in 1.92 µs.

The coefficient banks and configuration/control registers are not loaded with data until all data values for the specified address are loaded into the LF Interface™. In other words, the coefficient banks are not written to until all eight coefficients have been loaded into the LF Interface™. A round register is not written to until all four data values are loaded. After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed. As long as data is loaded into the interface, $\overline{LD}$ must remain LOW. After all desired coefficient banks and configuration/control registers are loaded with data, the LF Interface™ must be disabled. This is done by setting $\overline{LD}$ HIGH on the clock cycle after the clock cycle which latches the last data value. It is important that the LF Interface™ remain disabled when not loading data into it.

TABLE 13. SELECT REGISTER LOADING FORMAT

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	0	1	1	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	1	1	1	1

TABLE 14. LIMIT REGISTER LOADING FORMAT

	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
1st Word - Address	1	1	1	0	0	0	0	0	0	1	1	1
2nd Word - Data	R	R	R	R	0	1	1	0	0	0	0	0
3rd Word - Data	R	R	R	R	0*	0	1	1	1	0	1	1
4th Word - Data	R	R	R	R	1	0	1	0	0	1	0	0
5th Word - Data	R	R	R	R	0**	1	1	1	0	0	1	0

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit.
** This bit represents the MSB of the Upper Limit.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +4.5 V
Input signal with respect to ground	–0.5 V to 5.5 V
Signal applied to high impedance output	–0.5 V to 5.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA
ESD Classification (MIL-STD-883E METHOD 3015.7)	Class 3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ V_{CC} ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ V_{CC} ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		5.5	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			200	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

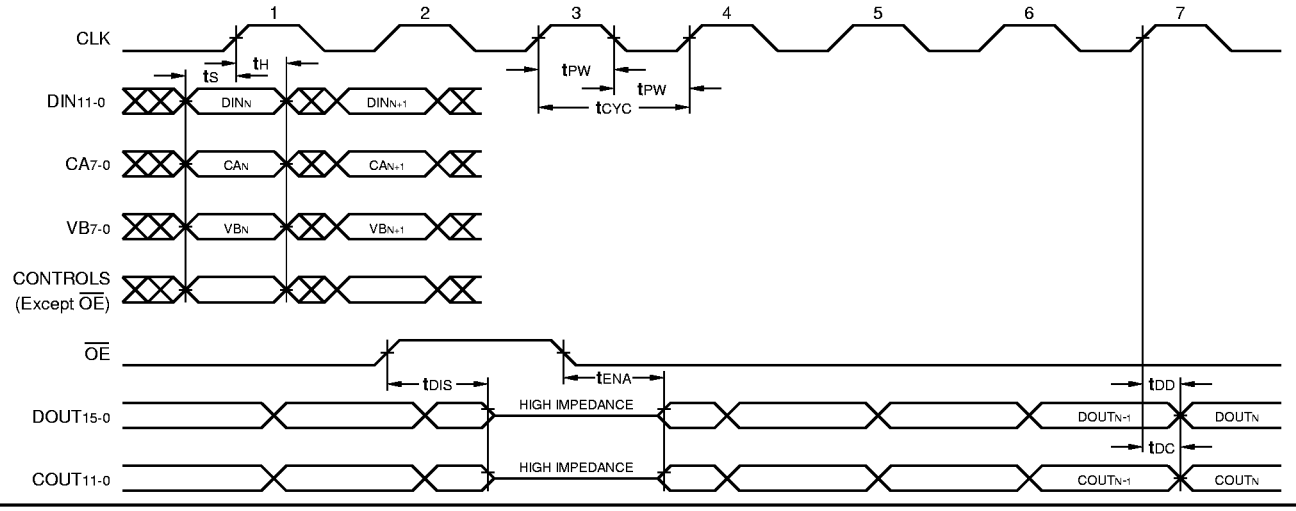
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3330–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Clock Cycle Time	25		15		12	
t_{PW}	Clock Pulse Width	10		7		4	
t_S	Input Setup Time	8		5		4	
t_H	Input Hold Time	0.5		0.5		0.5	
t_{DD}	Data Output Delay		13		8.5		8
t_{DC}	Cascade Data Output Delay		13		8.5		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		10		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		10		10

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF3330–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Clock Cycle Time	25		15	
t_{PW}	Clock Pulse Width	4		4	
t_S	Input Setup Time	5		5	
t_H	Input Hold Time	0.5		0.5	
t_{DD}	Data Output Delay		13		8.5
t_{DC}	Cascade Data Output Delay		13		8.5
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		10

SWITCHING WAVEFORMS: DATA I/O



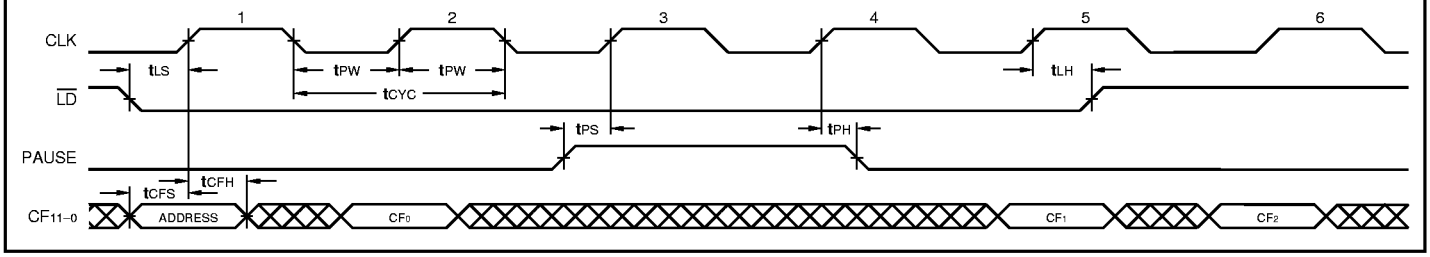
Commercial Operating Range (0°C to +70°C)

		LF3330–					
		25		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CFS}	Coefficient Input Setup Time	8		5		5	
t_{CFH}	Coefficient Input Hold Time	0		0		0	
t_{LS}	Load Setup Time	8		6		4	
t_{LH}	Load Hold Time	0		0		0	
t_{PS}	PAUSE Setup Time	8		5		4	
t_{PH}	PAUSE Hold Time	0.5		0.5		0.5	

Military Operating Range (–55°C to +125°C)

		LF3330–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{CFS}	Coefficient Input Setup Time	8		5	
t_{CFH}	Coefficient Input Hold Time	0		0	
t_{LS}	Load Setup Time	8		4	
t_{LH}	Load Hold Time	0		0	
t_{PS}	PAUSE Setup Time	8		4	
t_{PH}	PAUSE Hold Time	0.5		0.5	

Switching Waveforms: LF Interface™



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

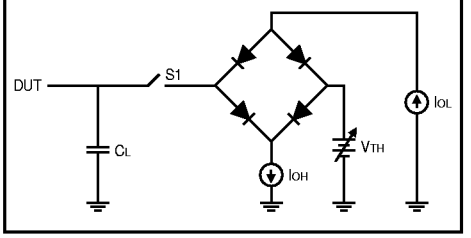
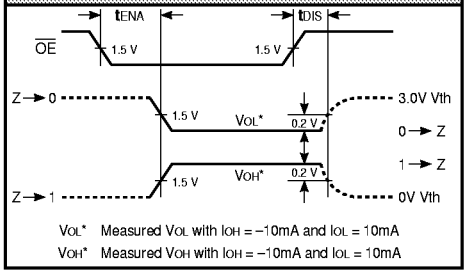
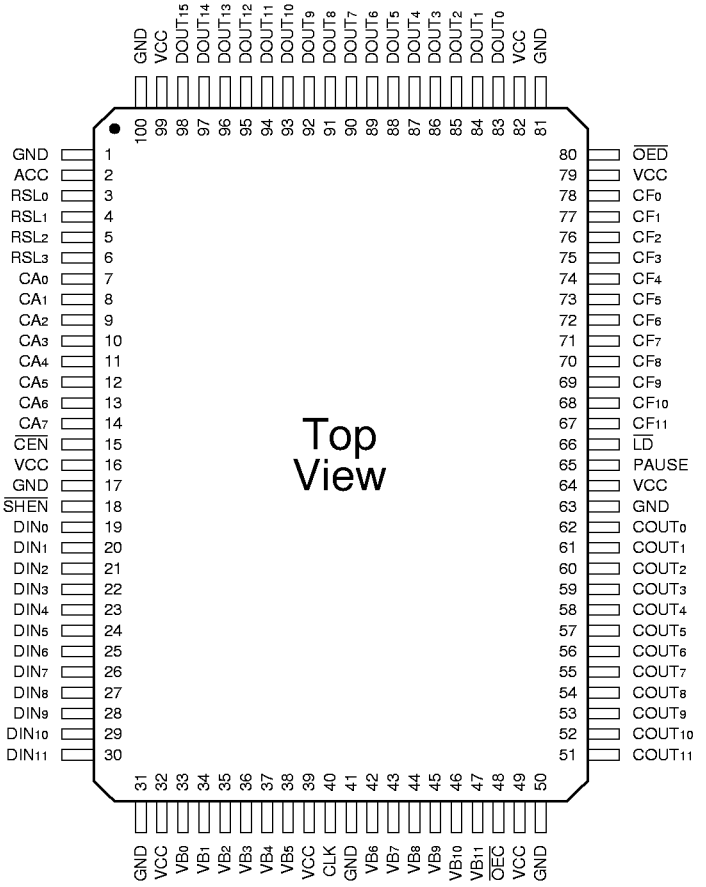


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

100-pin



Speed	Plastic Quad Flatpack (Q2)	Ceramic Quad Flatpack (F6)
	0°C to +70°C — Commercial Screening	
25 ns 15 ns 12 ns	LF3330QC25 LF3330QC15 LF3330QC12	
	–55°C to +125°C — Commercial Screening	
25 ns 15 ns 12 ns		
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns 15 ns		LF3330FMB25 LF3330FMB15

LF3330 Rev. A Errata Sheet
Vertical Digital Image Filter

Die Revision A of the LF3330 Vertical Filter, forces a timing dependency between the Configuration Register and $\overline{SHEN}$ not documented in the data sheet. While this timing dependency may no longer be required for future revisions of the LF3330, full compatibility with future releases will be maintained.

Configuration Register 0 and $\overline{SHEN}$ Timing Dependency

When configuring or re-configuring the LF3330 there is a corresponding timing relationship between a write to Configuration Register 0 (CR0 - address 200H) and the active level of $\overline{SHEN}$. In order to assure correct operation, $\overline{SHEN}$ must be held active for at least the 'Line Buffer Length + 2' clock cycles from the data write to Configuration Register 0 (CR0). Configuration Register 0's corresponding value determines the delay length of the line buffers.

Documented in the data sheets, the maximum delay length of each line buffer is 3076 clock cycles and the minimum delay is 4 clock cycles. Subsequently, the line buffer length is equal to the value of CR0 plus 4; writing 0 to CR0 will set the line buffer length to a value of 4. Conversely, writing 3072 to CR0 will set the line buffer length to a value of 3076. Any values greater than 3072 are invalid.

The active level of $\overline{SHEN}$ enables or disables the loading of data into the input /cascade registers and the line buffers. A LOW input permits data to be loaded and a HIGH input disables data input, leaving the previous register contents unchanged. The timing dependency is only related to the loading of the line buffer length into CR0 - address 200H.

LF Interface™

The LF Interface™ is used to load data into the coefficient banks and the Configuration/Control Registers; $\overline{LD}$ is used to enable or disable the LF Interface™. A LOW input permits data loading; conversely, a HIGH disables the LF Interface™. When data is not being loaded into the LF Interface™, $\overline{LD}$ should be inactive. When $\overline{SHEN}$ is held for the duration of 'Line Buffer Length + 2' clock cycles from the data write to Configuration Register 0 (CR0), data can be loaded through the LF Interface™.

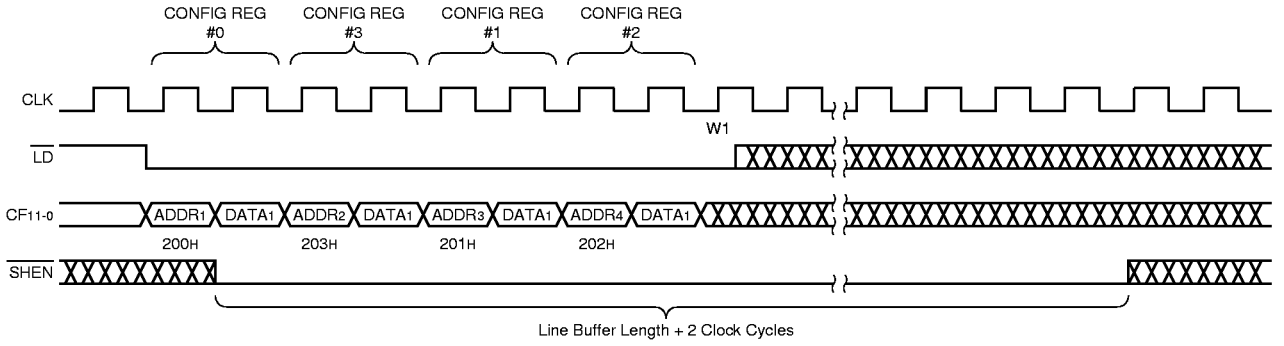
PAUSE is used to effectively slow the rate of loading data through the LF Interface™ when interfacing with a microprocessor or controller. It is recommended that $\overline{SHEN}$ be active when addressing CR0 and continue to hold it LOW prior to the data write to CR0. Once again, $\overline{SHEN}$ must be held active for at least the 'Line Buffer Length + 2' clock cycles from the data write to CR0.

For example, if a line buffer length of 1024 is required, the value of 1020 will be loaded into CR_0. $\overline{SHEN}$ must be held active for at least 1026 clock cycles (1024 + 2) from the data write to Configuration Register 0 (CR0).

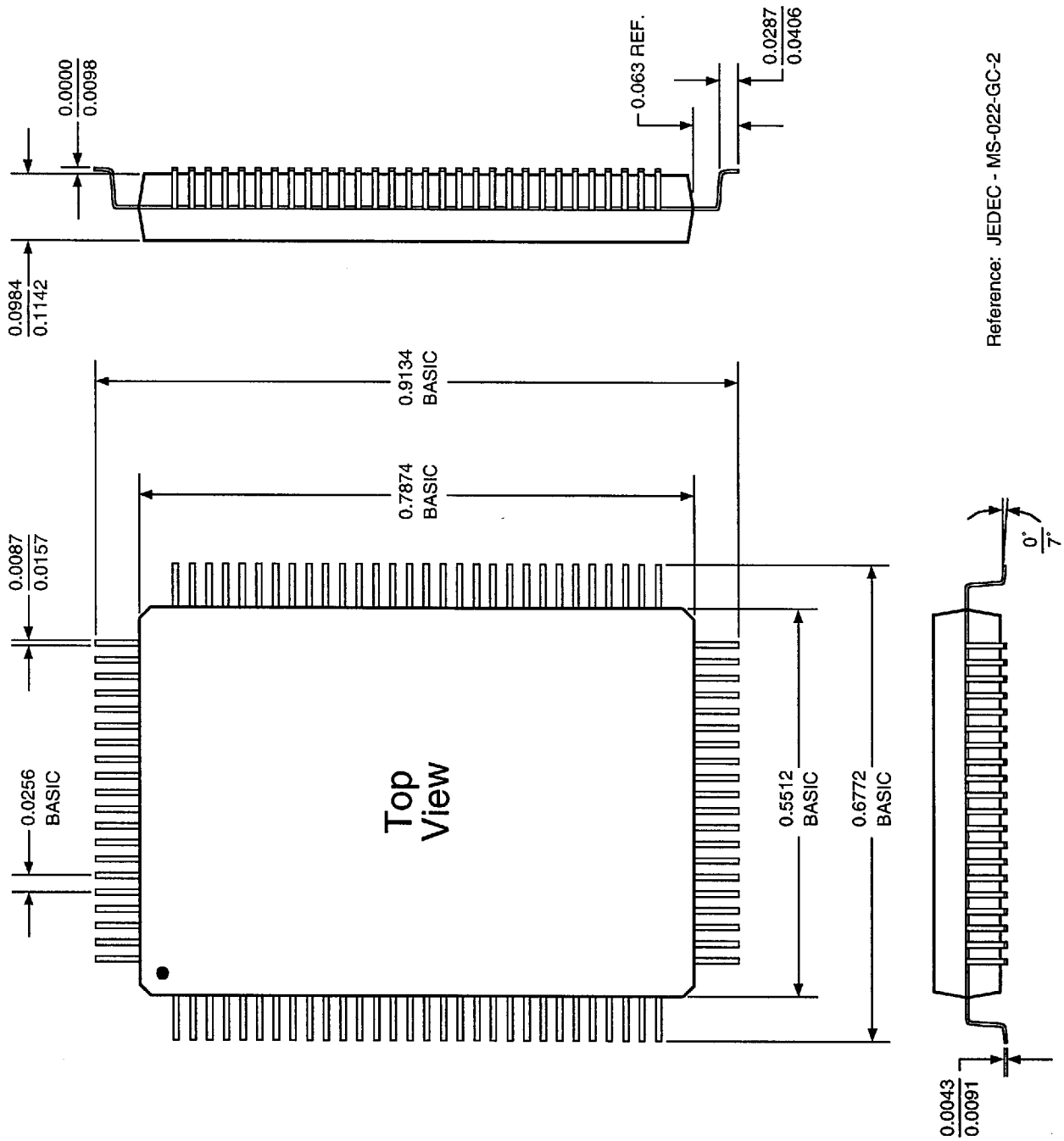
Performing a write to CR0 first will decrease the active delay time of $\overline{SHEN}$ when configuration or re-configuration involves more than one write to the Configuration/Control Registers. Meanwhile, when $\overline{SHEN}$ is active, all remaining functions of the LF Interface™ are available.

Figure 1 shows the corresponding timing relationship between Configuration Register 0 and $\overline{SHEN}$.

FIGURE 1. CONFIGURATION REGISTER 0 AND $\overline{SHEN}$ TIMING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.



LOGIC DEVICES INCORPORATED 1320 Orleans Drive Sunnyvale, CA 94089 (408) 542-5400	TITLE PLASTIC QUAD FLATPACK 100-PIN	DOCUMENT NUMBER MD-Q2	REV B
		DATE 01/13/97	SHEET 1 OF 1

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