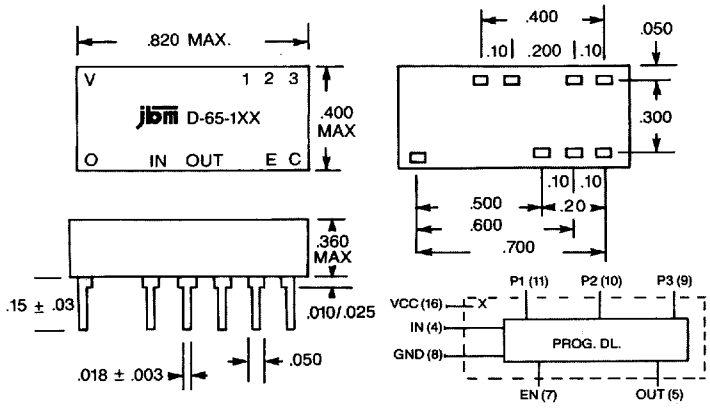
* See DESC Listing pg. 28

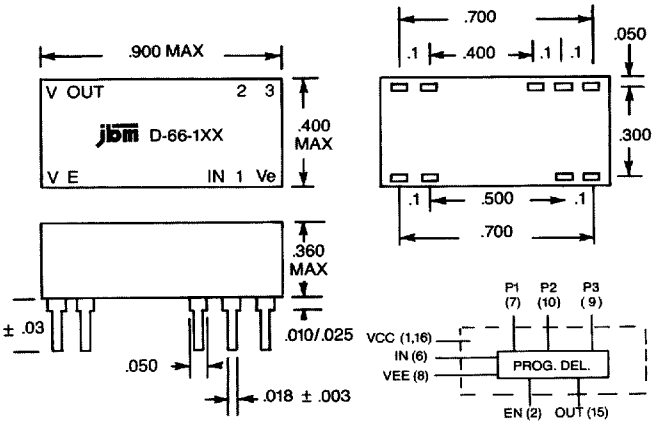
D-65-100 SERIES*

TTL 3 Bit
Programmables



D-66-100 SERIES*

10K ECL 3 Bit
Programmables



3 Bit TTL Programmable...

DELAY LINE CHARACTERISTICS

Input Characteristics:

V_{IH} Logic "1" Input Voltage ..... 2.0V Min.
V_{IL} Logic "0" Input Voltage ..... .8V Max.
I_{IH} Logic "1" Input Current ..... −30mA @ 3.0V
I_{IL} Logic "0" Input Current ..... −6mA @ .45V

Output Characteristics:

V_{OH} Logic "1" Output Voltage ..... 2.4V Min.
V_{OL} Logic "0" Output Voltage ..... .4V Max.
I_{CC} ..... 50mA Max.
V_{CC} ..... 4.5 to 5.5 Volts

Test Conditions:
Delays at 25°C with PWI @ 1.5 × Maximum Delay with 5.0 VDC, Pulse Space 3 × Pw.

FEATURES

- Utilizes hermetic/ceramic integrated circuits screened to MIL-STD-883, LEVEL B

Environment:

Operating temperature .....
−55°C to +125°C
Storage temperature .....
−65°C to +125°C

3 Bit ECL Programmable...

DELAY LINE CHARACTERISTICS

Input Characteristics:

V_{IH} Logic "1" Input Voltage ..... −.98V Min.
V_{IL} Logic "0" Input Voltage ..... −1.63V Max.
I_{IH} Logic "1" Input Current ..... 25mA Max.
I_{IL} Logic "0" Input Current ..... .5μA Max.

Output Characteristics:

V_{OH} Logic "1" Output Voltage ..... −.96V Min.
V_{OL} Logic "0" Output Voltage ..... −1.65V Max.
I_{CC} ..... 120mA Max.
V_{EE} ..... −5.2V ±5%

Test Conditions:
Delays at 25°C with PWI @ 20 ns D-66-132 to −136
with 5.2 V TO Vee. 150 ns D-66-137 to −149

TTL			DELAY SPECIFICATIONS IN (ns) NANOSECONDS									ECL		
Program Pins 3		0	1	2	3	4	5	6	7	Delay Time	Delay Time	Program Pins 3		0
Part 2		0	0	1	1	0	0	1	1	Per	Step	Part 2		0
Numbers 1		0	1	0	1	0	1	0	1	Step	Tol.	Numbers 1		0
D-65-142	7 ± 2 ns	14 ns	1	2	3	4	5	6	7	1 ns	± .3 ns	D-66-132	3 ± 2 ns	10 ns
D-65-143	7 ± 2 ns	21 ns	2	4	6	8	10	12	14	2 ns	± .4 ns	D-66-133	3 ± 2 ns	17 ns
D-65-144	7 ± 2 ns	28 ns	3	6	9	12	15	18	21	3 ns	± .5 ns	D-66-134	3 ± 2 ns	24 ns
D-65-151	7 ± 2 ns	35 ns	4	8	12	16	20	24	28	4 ns	± .5 ns	D-66-135	3 ± 2 ns	31 ns
D-65-145	7 ± 2 ns	42 ns	5	10	15	20	25	30	35	5 ns	± .5 ns	D-66-136	3 ± 2 ns	38 ns
D-65-152	7 ± 2 ns	49 ns	6	12	18	24	30	36	42	6 ns	± .6 ns	D-66-137	3 ± 2 ns	45 ns
D-65-153	7 ± 2 ns	56 ns	7	14	21	28	35	42	49	7 ns	± .7 ns	D-66-138	3 ± 2 ns	52 ns
D-65-154	7 ± 2 ns	63 ns	8	16	24	32	40	48	56	8 ns	± .8 ns	D-66-139	3 ± 2 ns	59 ns
D-65-155	7 ± 2 ns	70 ns	9	18	27	36	45	54	63	9 ns	± .9 ns	D-66-140	3 ± 2 ns	66 ns
D-65-146	7 ± 2 ns	77 ns	10	20	30	40	50	60	70	10 ns	± 1 ns	D-66-141	3 ± 2 ns	73 ns
D-65-147	7 ± 2 ns	112 ns	15	30	45	60	75	90	105	15 ns	± 1 ns	D-66-142	3 ± 2 ns	108 ns
D-65-148	7 ± 2 ns	147 ns	20	40	60	80	100	120	140	20 ns	± 1.5 ns	D-66-143	3 ± 2 ns	143 ns
D-65-156	7 ± 2 ns	182 ns	25	50	75	100	125	150	175	25 ns	± 1.5 ns	D-66-144	3 ± 2 ns	178 ns
D-65-157	7 ± 2 ns	217 ns	30	60	90	120	150	180	210	30 ns	± .2 ns	D-66-145	3 ± 2 ns	213 ns
D-65-158	7 ± 2 ns	252 ns	35	70	105	140	175	210	245	35 ns	± .2 ns	D-66-146	3 ± 2 ns	248 ns
D-65-149	7 ± 2 ns	287 ns	40	80	120	160	200	240	280	40 ns	± 2.5 ns	D-66-147	3 ± 2 ns	283 ns
D-65-159	7 ± 2 ns	322 ns	45	90	135	180	225	270	315	45 ns	± 2.5 ns	D-66-148	3 ± 2 ns	318 ns
D-65-150	7 ± 2 ns	357 ns	50	100	150	200	250	300	350	50 ns	± 2.5 ns	D-66-149	3 ± 2 ns	353 ns

Max Deviation From Programmed Delay 1 ns or 5%

*Steps 1 to 7 Reference to Zero