

FEATURES

- ❑ 40 MHz Maximum Sampling Rate
- ❑ 320 MHz Multiply-Accumulate Rate
- ❑ 8 Filter Cells
- ❑ 8-bit Unsigned or 9-bit Two's Complement Data/Coefficients
- ❑ 26-bit Data Outputs
- ❑ Shift-and-Add Output Stage for Combining Filter Outputs
- ❑ Expandable Data Size, Coefficient Size, and Filter Length
- ❑ User-Selectable 2:1, 3:1, or 4:1 Decimation
- ❑ DECC SMD No. 5962-92097
- ❑ Available 100% Screened to MIL-STD-883, Class B
- ❑ Replaces Harris HSP43891 and HSP43891/883
- ❑ Package Styles Available:
 - 84-pin Plastic LCC, J-Lead
 - 100-pin Plastic Quad Flatpack
 - 84-pin Ceramic PGA

DESCRIPTION

The LF43891 is a video-speed digital filter that contains eight filter cells (taps) cascaded internally and a shift-and-add output stage. A 9×9 multiplier, three decimation registers, and a 26-bit accumulator are contained in each filter cell. The output stage of the LF43891 contains a 26-bit accumulator which can add the contents of any filter stage to the output stage accumulator shifted right by 8 bits. 8-bit unsigned or 9-bit two's complement format for data and coefficients can be independently selected.

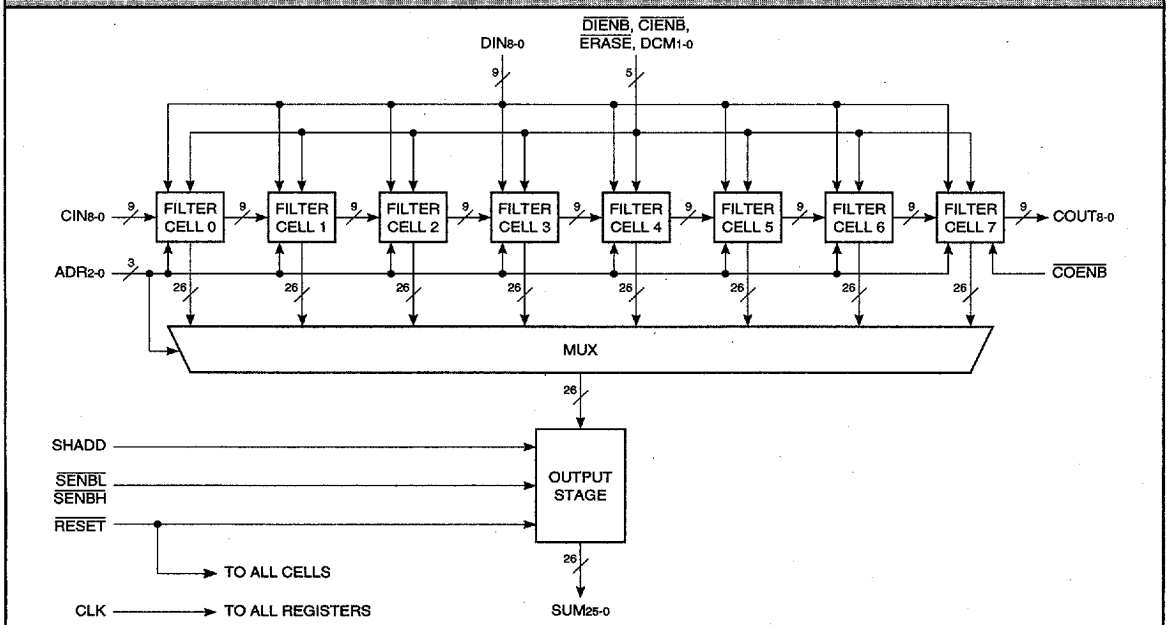
Expanded coefficients and word sizes can be processed by cascading multiple LF43891s to implement larger filter lengths without affecting the sample rate. By reducing the sample

rate, a single LF43891 can process larger filter lengths by using multiple passes. The sampling rate can range from 0 to 40 MHz. Over 1000 taps may be processed without overflows due to the architecture of the device.

The output sample rate can be reduced to one-half, one-third, or one-fourth the input sample rate by using the three decimation registers contained in every filter cell. Matrix multiplication, $N \times N$ spatial correlations/convolutions, and other 2-D operations for image processing can also be achieved using these registers.

2

LF43891 BLOCK DIAGRAM

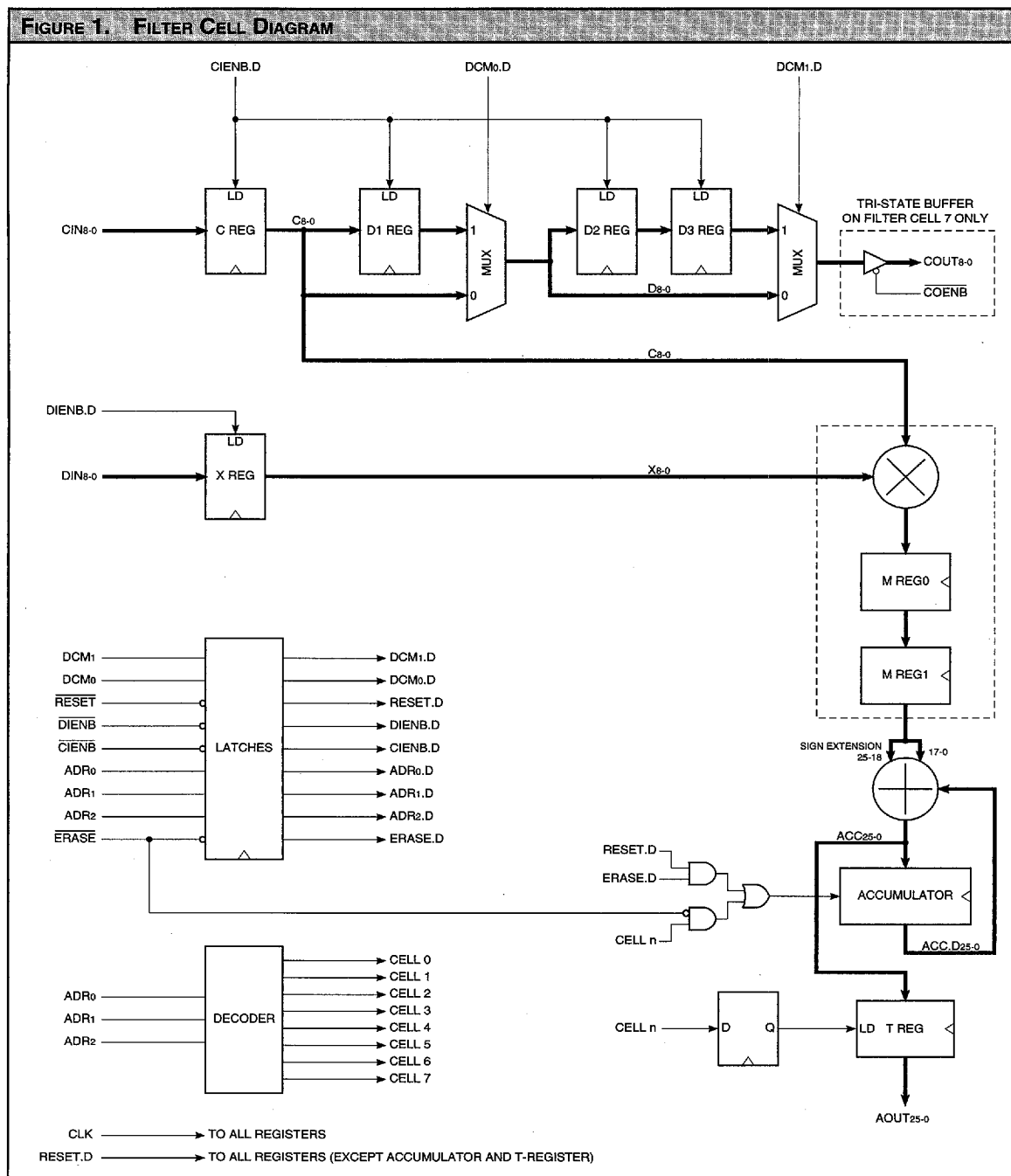


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FIGURE 1. FILTER CELL DIAGRAM



FILTER CELL DESCRIPTION

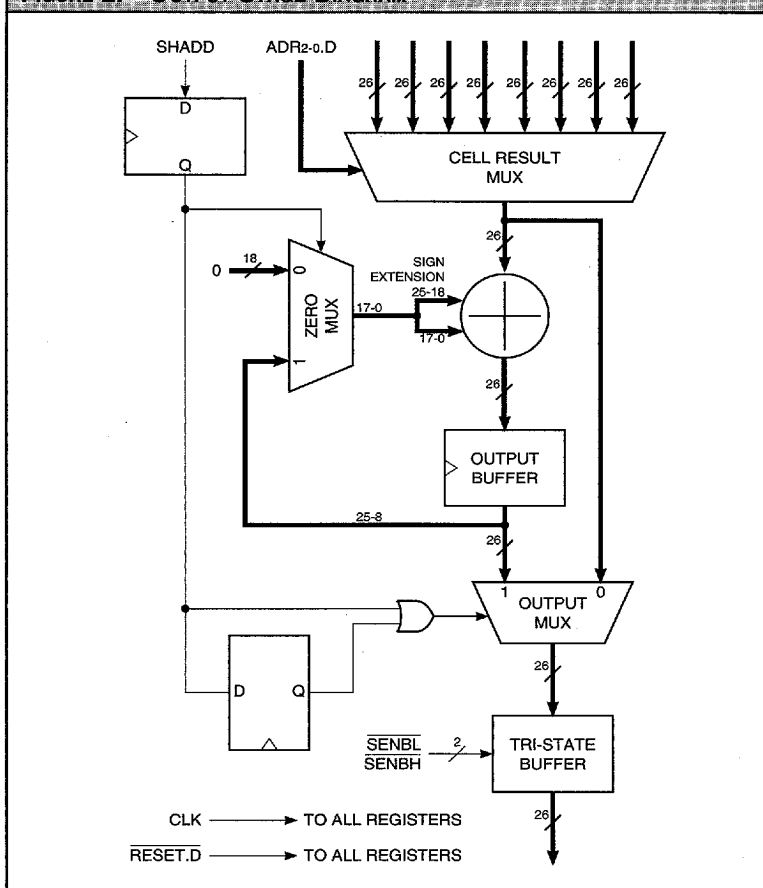
9-bit coefficients are loaded into the C register (CIN8-0) and are output as COUT8-0 (the $\overline{\text{COENB}}$ signal enables the COUT8-0 outputs). The path taken by the coefficients varies according to the decimation mode chosen. With no decimation, the coefficients move directly from the C register, bypassing all decimation registers, and are available at the output on the following clock cycle. When decimation is chosen, the coefficient output is delayed by 1, 2, or 3 clock cycles depending on how many decimation registers the coefficients pass through (D1, D2, or D3). The number of decimation registers the coefficients pass through is determined by DCM1-0. Refer to Table 1 for choosing a decimation mode.

$\overline{\text{CIENB}}$ enables the C and D registers for coefficient loading. The registers are loaded on the rising edge of CLK when $\overline{\text{CIENB}}$ is LOW. $\overline{\text{CIENB}}$ is latched and delayed internally which enables the registers for loading one clock cycle after $\overline{\text{CIENB}}$ goes active (loading takes place on the second rising edge of CLK after $\overline{\text{CIENB}}$ goes LOW). Therefore, $\overline{\text{CIENB}}$ must be LOW one clock cycle before the coefficients are placed on the CIN8-0 inputs. The coefficients are held when $\overline{\text{CIENB}}$ is HIGH.

$\overline{\text{DIENB}}$ enables the X register for the loading of data. The X register is loaded on the rising edge of CLK when $\overline{\text{DIENB}}$ is LOW. $\overline{\text{DIENB}}$ is latched and delayed internally (loading takes place on the second rising edge of CLK after $\overline{\text{DIENB}}$ goes LOW). Therefore, $\overline{\text{DIENB}}$ must be LOW one clock cycle before the data is placed on the DIN8-0 inputs. The X register is loaded with all zeros when $\overline{\text{DIENB}}$ is HIGH.

The output of the C register (C8-0) and X register (X8-0) provide the inputs of the 9 x 9 multiplier. The multiplier is followed by two pipeline registers,

FIGURE 2. OUTPUT STAGE DIAGRAM



M REG0 and M REG1. The output of the multiplier is sign extended and is used as one of the inputs to the 26-bit adder. The output of the 26-bit accumulator provides the second input to the adder. Both the accumulator and T register are loaded simultaneously with the output of the adder.

The accumulator is loaded with the output of the adder on every clock cycle unless cleared. Clearing the accumulator can be achieved using two methods. The first method, when both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are LOW, causes all accumulators and all

registers in the device to be cleared together. $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ go active.

The second method, when only $\overline{\text{ERASE}}$ is LOW, clears a single accumulator of a selected cell. The cell is selected using the ADR2-0 inputs (decoded to Cell n). $\overline{\text{ERASE}}$ is latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{ERASE}}$ goes active. Refer to Table 2 for clearing registers and accumulators.

TABLE 1. DECIMATION MODE SELECTION		
DCM1	DCM0	Decimation Function
0	0	Decimation registers not used
0	1	One decimation register used (decimation by one-half)
1	0	Two decimation registers used (decimation by one-third)
1	1	Three decimation registers used (decimation by one-fourth)

TABLE 2. REGISTER AND ACCUMULATOR CLEARING		
ERASE	RESET	Clearing Effect
0	0	All accumulators and all registers are cleared
0	1	Only the accumulator addressed by ADR2-0 is cleared
1	0	All registers are cleared (accumulators are not cleared)
1	1	No clearing occurs, internal state remains the same

OUTPUT STAGE DESCRIPTION

The 26-bit adder contained in the output stage can add the contents of any filter cell accumulator (selected by ADR2-0) with the 18 most significant bits of the output buffer. The result is stored back into the output buffer.

The complete operation takes only one clock cycle. The eight least significant bits of the output buffer are lost.

The Zero multiplexer is controlled by the SHADD input signal. This allows selection of either the 18 most significant bits of the output buffer or all zeros for the adder input. When SHADD is LOW, all zeros will be selected. When SHADD is HIGH, the 18 most significant bits of the output buffer are selected enabling the shift-and-add operation. SHADD is latched and delayed internally by one clock cycle.

The output multiplexer is also controlled by the SHADD input signal. This allows selection of either a filter cell accumulator, selected by ADR2-0, or the output buffer to be output to the SUM25-0 bus. Only the 26 least significant bits from either a filter cell accumulator or the output buffer are output on SUM25-0. If SHADD is LOW during two consecutive clock

cycles (low during the current and previous clock cycle), the output multiplexer selects the contents of a filter cell accumulator addressed by ADR2-0. Otherwise, the output multiplexer selects the contents of the output buffer.

If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change to reflect any updates to the addressed cell accumulator. Only the result from the first selection of the cell (first clock cycle) will be output. This allows the interface of slow memory devices where the output needs to be active for more than one clock cycle. Normal FIR operation is not affected because ADR2-0 is changed sequentially.

NUMBER SYSTEMS

Data and coefficients can be represented as either 8-bit unsigned or 9-bit two's complement numbers. All values are represented as 9-bit two's complement numbers internally. If the most significant or sign bit is a zero, the multiplier can multiply 8-bit unsigned numbers.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DIN8-0 — Data Input

9-bit data is latched into the X register of each filter cell simultaneously. The $\overline{\text{DIENB}}$ signal enables loading of the data.

CIN8-0 — Coefficient Input

9-bit coefficients are latched into the C register of Filter Cell 0. The $\overline{\text{CIENB}}$ signal enables loading of the coefficients.

Outputs

SUM25-0 — Data Output

The 26-bit result from an individual filter cell will appear when ADR2-0 is used to select the filter cell result. SHADD in conjunction with ADR2-0 is used to select the output from the shift-and-add output stage.

COUT8-0 — Coefficient Output

The 9-bit coefficient output from Filter Cell 7 can be connected to the CIN8-0 coefficient input of the same LF43891 to recirculate the coefficients. COUT8-0 can also be connected to the CIN8-0 of another LF43891 to cascade the devices. The $\overline{\text{COENB}}$ signal enables the output of the coefficients.

Controls

DIENB — Data Input Enable

The DIENB input enables the X register of every filter cell. While DIENB is LOW, the X registers are loaded with the data present at the DIN8-0 inputs on the rising edge of CLK. While DIENB is HIGH, all bits of DIN8-0 are forced to zero and a rising edge of CLK will load the X register of every filter cell with all zeros. DIENB must be low one clock cycle prior to presenting the input data on the DIN8-0 input since it is latched and delayed internally.

CIENB — Coefficient Input Enable

The CIENB input enables the C and D registers of every filter cell. While CIENB is LOW, the C and appropriate D registers are loaded with the coefficient data on the rising edge of CLK. While CIENB is HIGH, the contents of the C and D registers are held and the CLK signal is ignored. By using CIENB in its active state, coefficient data can be shifted from cell to cell. CIENB must be low one clock cycle prior to presenting the coefficient data on the CIN8-0 input since it is latched and delayed internally.

COENB — Coefficient Output Enable

The COENB input enables the COUT8-0 output. When COENB is LOW, the outputs are enabled. When COENB is HIGH, the outputs are placed in a high-impedance state.

DCM1-0 — Decimation Control

The DCM1-0 inputs select the number of decimation registers to use (Table 1). Coefficients are passed from one cell to another at a rate determined by DCM1-0. When no decimation registers are selected, the coefficients are passed from cell to cell on every rising edge of CLK (no decimation). When one decimation register is selected, the coefficients are passed from cell to cell on every other rising edge of CLK (2:1 decimation). When two decimation registers are selected, the coefficients are passed from cell to cell on every third rising edge of CLK (3:1 decimation) and so on. DCM1-0 is latched and delayed internally.

ADR2-0 — Cell Accumulator Select

The ADR2-0 inputs select which cell's accumulator will be available at the SUM25-0 output or added to the output stage accumulator. In both cases, ADR2-0 is latched and delayed by one clock cycle. If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change if the contents of the accumulator changes. Only the result from the first selection of the cell (first clock cycle) by ADR2-0 will be available. ADR2-0 is also used to select which accumulator to clear when ERASE is LOW.

SENBH — MSB Output Enable

When SENBH is LOW, SUM25-16 is enabled. When SENBH is HIGH, SUM25-16 is placed in a high-impedance state.

SENB — LSB Output Enable

When SENB is LOW, SUM15-0 is enabled. When SENB is HIGH, SUM15-0 is placed in a high-impedance state.

RESET — Register Reset Control

When RESET is LOW, all registers are cleared simultaneously except the cell accumulators. RESET can be used with ERASE to clear all cell accumulators. RESET is latched and delayed internally. Refer to Table 2.

ERASE — Accumulator Erase Control

When ERASE is LOW, the cell accumulator specified by ADR2-0 is cleared. When RESET is LOW in conjunction with ERASE, all cell accumulators are cleared. Refer to Table 2.

MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
VCC supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-0.5 V to VCC + 0.5 V
Signal applied to high impedance output	-0.5 V to VCC + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ VCC ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ VCC ≤ 5.50 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions (Note 4)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	VCC = Min., IOH = -400 μA	2.6			V
VOL	Output Low Voltage	VCC = Min., IOL = 2.0 mA			0.4	V
VIH	Input High Voltage		2.0		VCC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ VIN ≤ VCC (Note 12)			±10	μA
IOZ	Output Leakage Current	(Note 12)			±10	μA
ICC1	VCC Current, Dynamic	(Notes 5, 6)			160	mA
ICC2	VCC Current, Quiescent	(Note 7)			750	μA
CIN	Input Capacitance	TA = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	TA = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

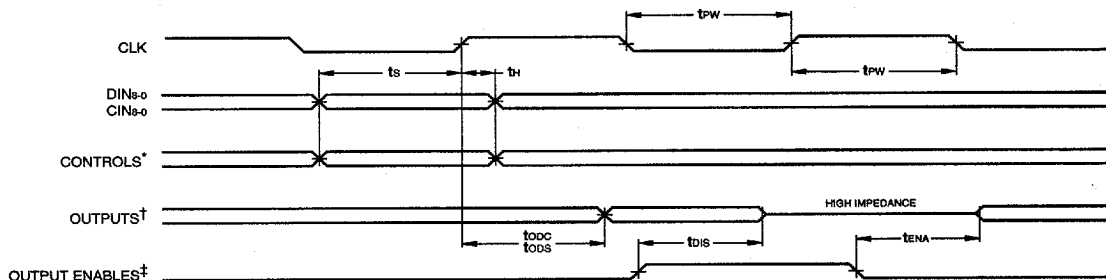
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol Parameter		LF43891-							
		50		40		33		25	
		Min	Max	Min	Max	Min	Max	Min	Max
t _{CYC}	Cycle Time	50		39		33		25	
t _{PW}	Clock Pulse Width	20		16		13		10	
t _S	Input Setup Time	16		14		13		10	
t _H	Input Hold Time	0		0		0		0	
t _{ODC}	Coefficient Output Delay		24		20		18		16
t _{ODS}	Sum Output Delay		27		25		21		18
t _{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15		12
t _{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15		12

MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol Parameter		LF43891-					
		50		40		33	
		Min	Max	Min	Max	Min	Max
t _{CYC}	Cycle Time	50		39		33	
t _{PW}	Clock Pulse Width	20		16		13	
t _S	Input Setup Time	20		17		13	
t _H	Input Hold Time	0		0		0	
t _{ODC}	Coefficient Output Delay		24		20		18
t _{ODS}	Sum Output Delay		31		25		21
t _{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15
t _{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15

SWITCHING WAVEFORMS



*includes \overline{DIENB} , \overline{CIENB} , ERASE, RESET, SHADD, DCM1-o, and ADR2-o.

†includes SUM2s-o and COUTs-o.

‡includes SENBL, SENBH, and \overline{COENB} .

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 pF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.

b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

11. For the tENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the tDIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

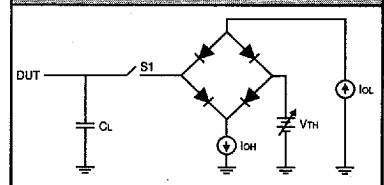
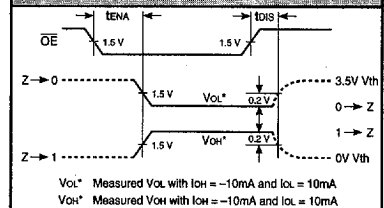


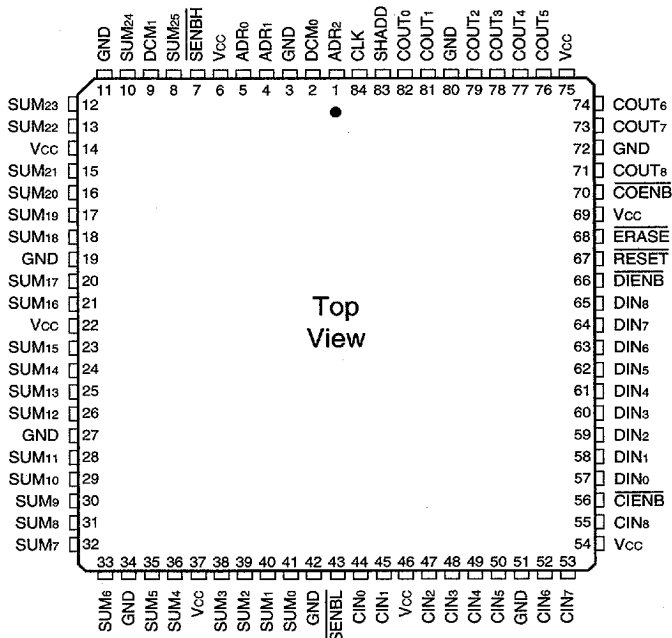
FIGURE B. THRESHOLD LEVELS



10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

ORDERING INFORMATION

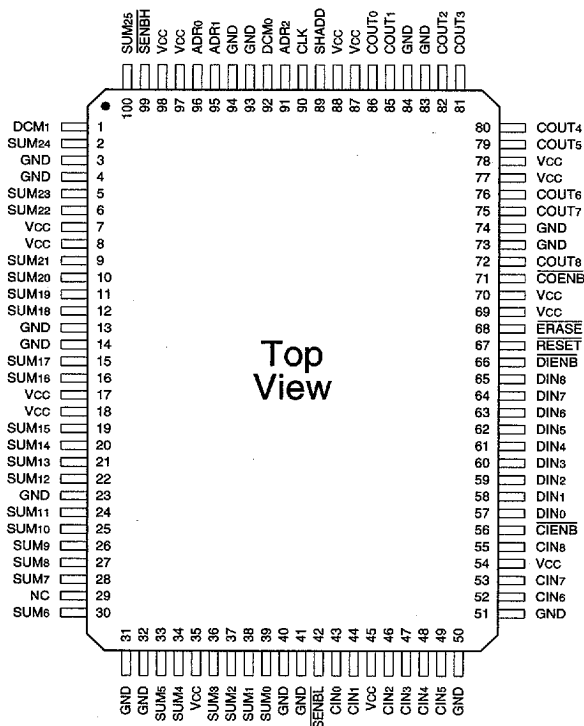
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891JC50
40 ns	LF43891JC40
33 ns	LF43891JC33
25 ns	LF43891JC25

ORDERING INFORMATION

100-pin



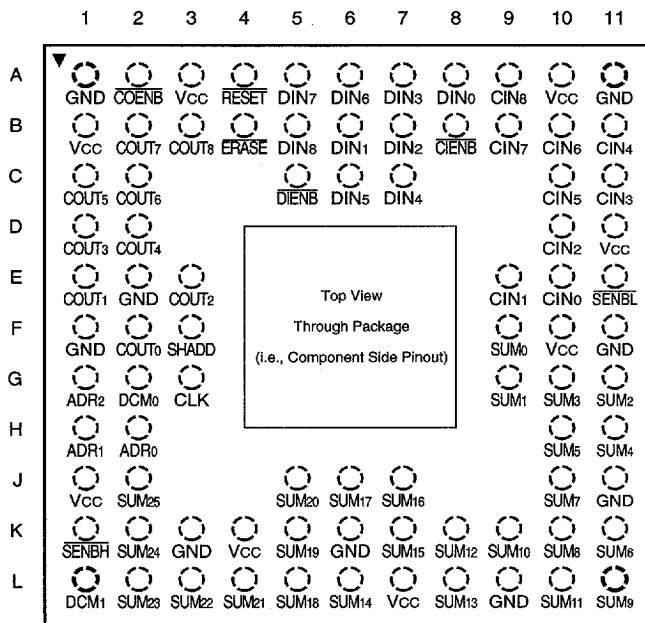
Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891QC50
40 ns	LF43891QC40
33 ns	LF43891QC33
25 ns	LF43891QC25

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ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891GC50
40 ns	LF43891GC40
33 ns	LF43891GC33
25 ns	LF43891GC25
	-55°C to +125°C — COMMERCIAL SCREENING
50 ns	LF43891GM50
40 ns	LF43891GM40
33 ns	LF43891GM33
	-55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	LF43891GMB50
40 ns	LF43891GMB40
33 ns	LF43891GMB33

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