National Semiconductor

February 1995

LF441 Low Power JFET Input Operational Amplifier

General Description

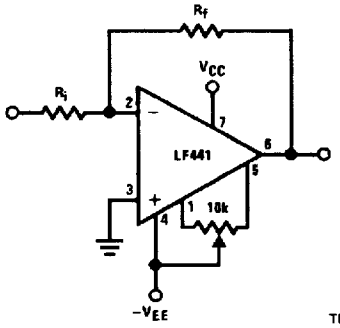
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM741	200 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	0.5 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



TL/H/9297–1

Ordering Information

LF441XYZ

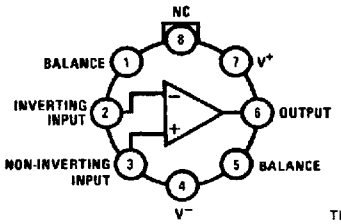
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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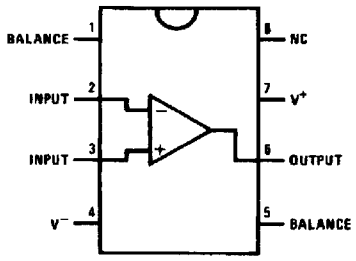
Top View

Note: Pin 4 connected to case.

Order Number LF441MH/883
See NS Package Number H08A

Dual-In-Line Package



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Top View
Order Number LF441ACN,
LF441CM or LF441CN
See NS Package Number M08A or N08E

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF441A	LF441
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package	M Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW	
$T_{j\,max}$	150°C	115°C	
θ_{jA}(Typical)		130°C/W	185°C/W
Board Mount in still air	165°C/W		
Board Mount in 400 LF/min air flow	65°C/W		
θ_{jC}	25°C/W		
Operating Temp. Range	(Note 3)	(Note 3)	
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C	

	LF441A	LF441
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) Rating to be Determined

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF441A			LF441			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$			0.3	0.5		1	5	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$ (Note 5)			7	10		10		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\,k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18, −17		±11	+14, −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$		80	100		70	95		dB

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		70	90		dB
I_S	Supply Current			150	200		150	250	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF441A and for $V_S = \pm 15V$ for the LF441. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF441A is 100% tested to this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

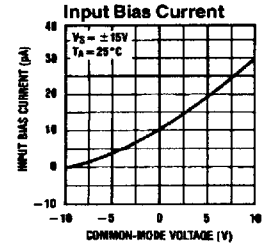
Note 8: Refer to RETS441X for LF441MH military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

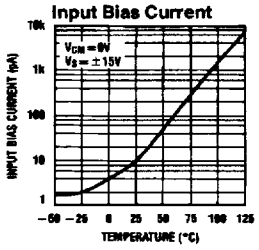
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

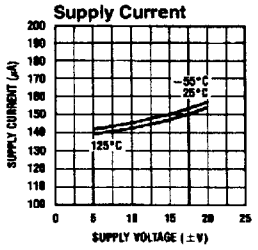
Input Bias Current



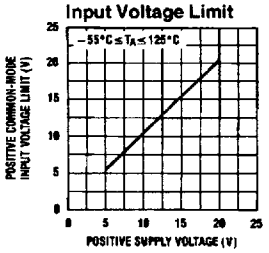
Input Bias Current



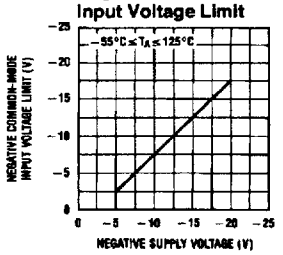
Supply Current



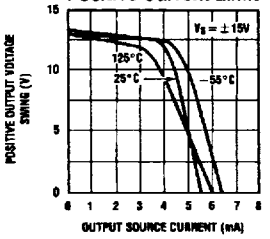
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



Positive Current Limit



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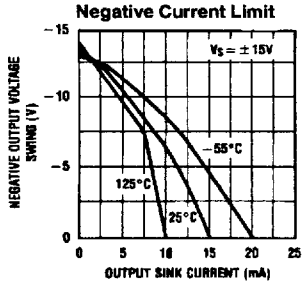
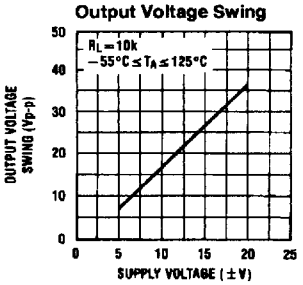
Typical Performance Characteristics (Continued)

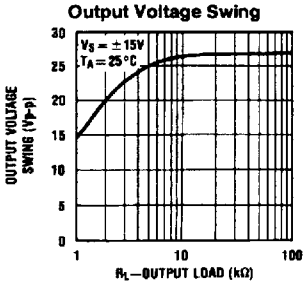
Negative Current Limit



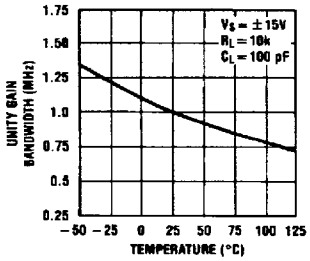
Output Voltage Swing



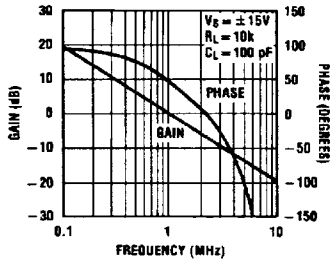
Output Voltage Swing



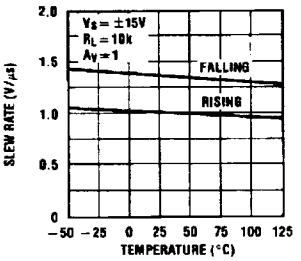
Gain Bandwidth



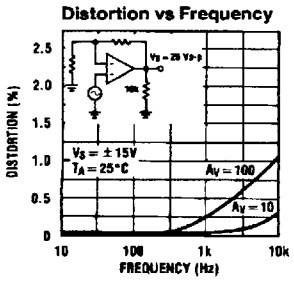
Bode Plot



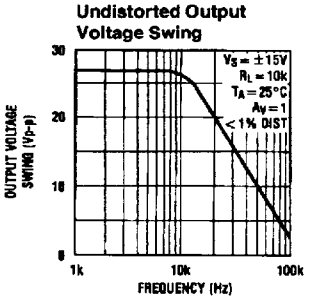
Slew Rate



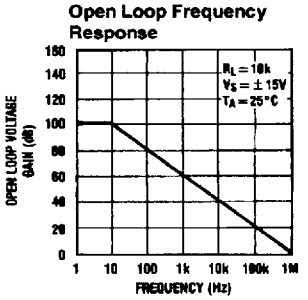
Distortion vs Frequency



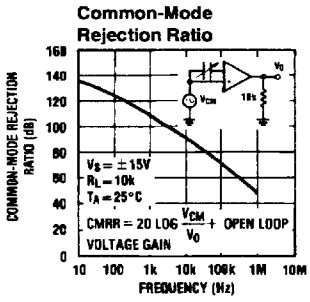
Undistorted Output Voltage Swing



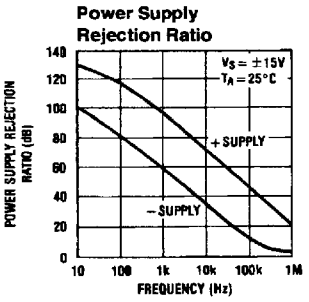
Open Loop Frequency Response



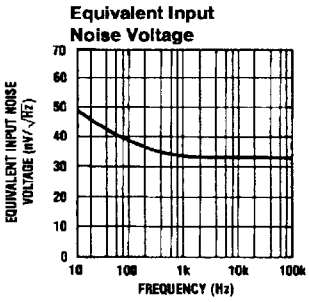
Common-Mode Rejection Ratio



Power Supply Rejection Ratio



Equivalent Input Noise Voltage



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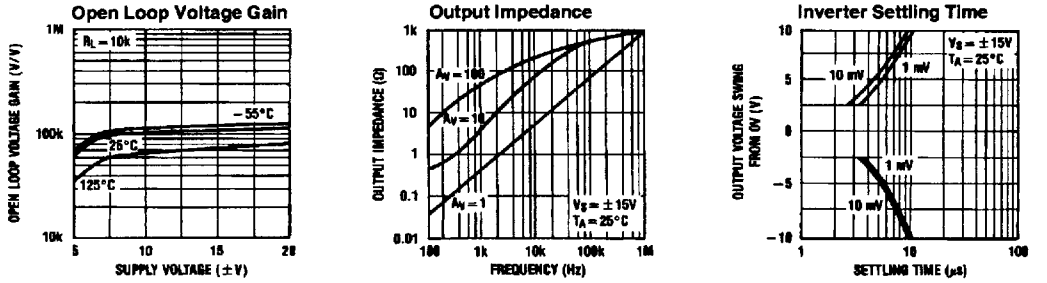
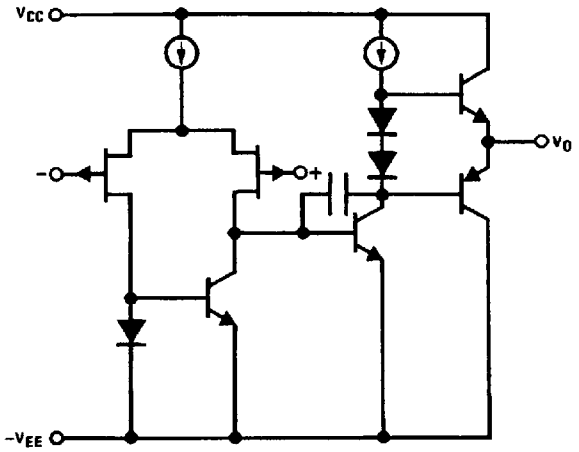
Typical Performance Characteristics (Continued)



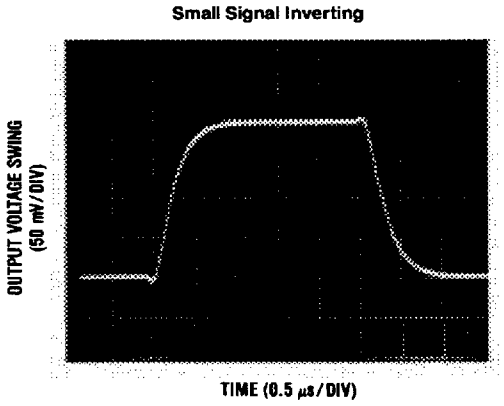
TL/H/9297–7

Simplified Schematic



TL/H/9297–3

Pulse Response R_L = 10 kΩ, C_L = 10 pF



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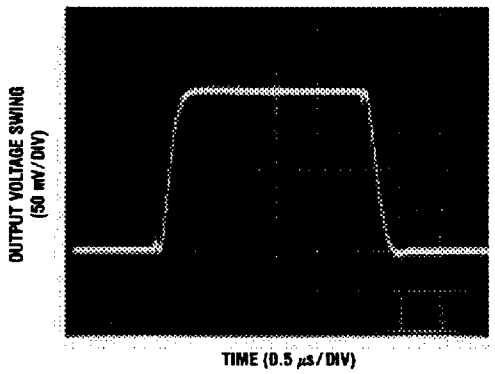
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$ (Continued)

Small Signal Non-Inverting



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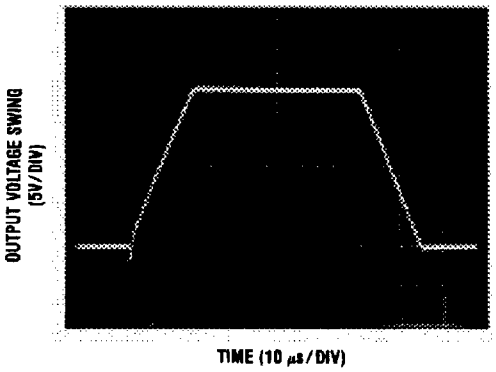
Large Signal Inverting



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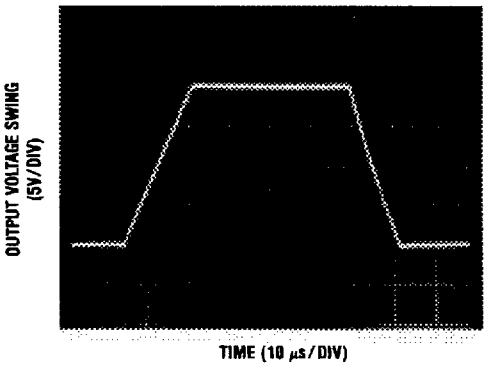
Large Signal Non-Inverting



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Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of ±3V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

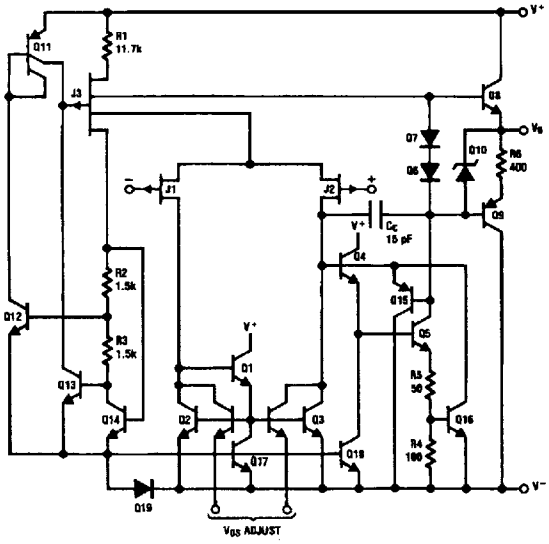
The amplifier will drive a 10 kΩ load resistance to ±10V over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

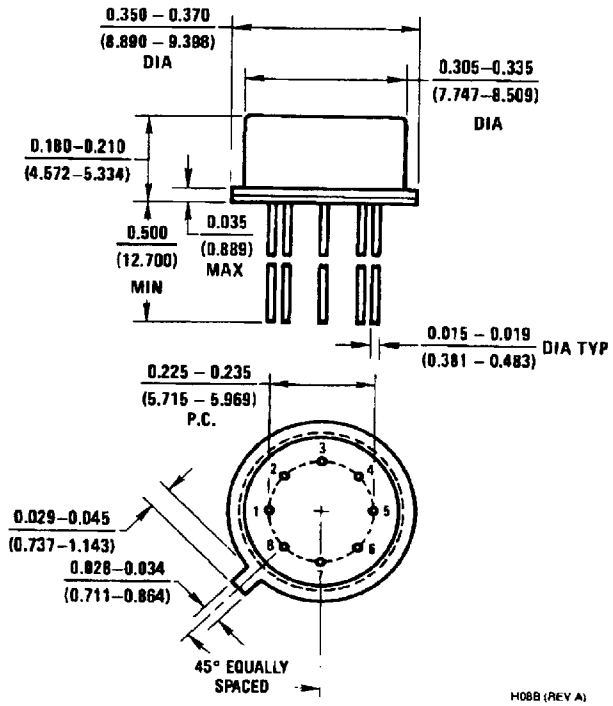
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic

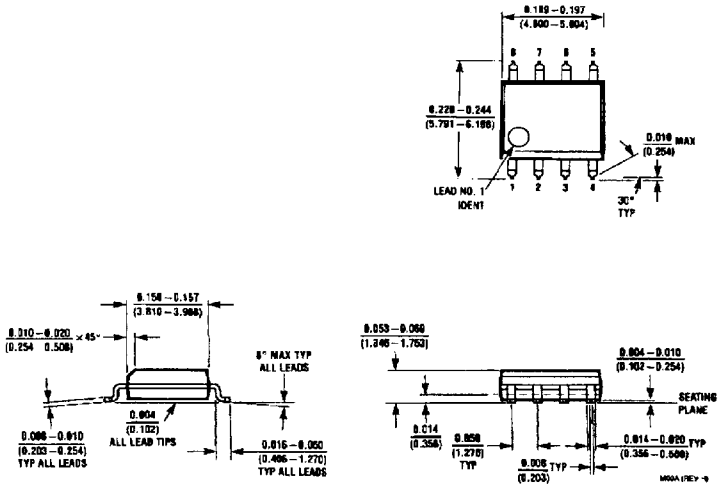


TL/H/9297–13

Physical Dimensions inches (millimeters)

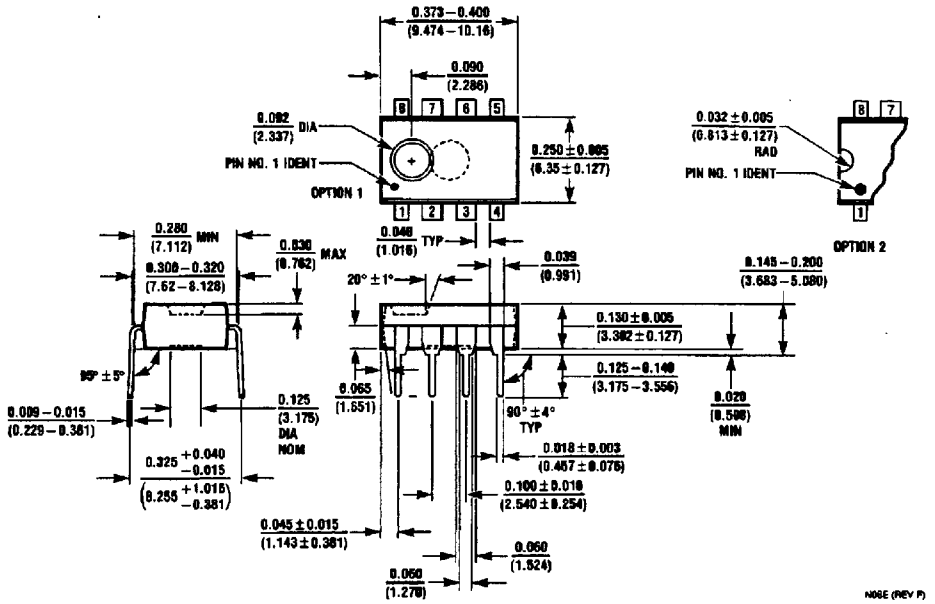


Metal Can Package (H)
Order Number LF441MH/883
NS Package Number H08A



Dual-In-Line Package(M)
Order Number LF441CM
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF441ACN or LF441CN
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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