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National Semiconductor

LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

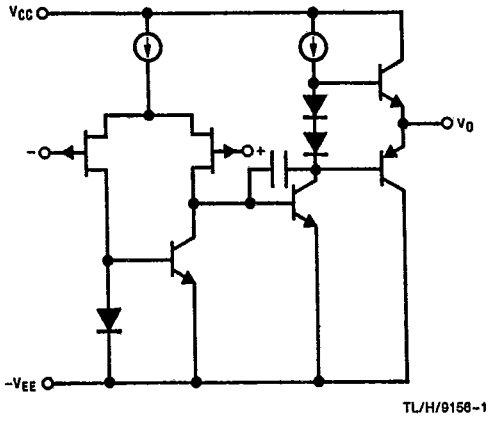
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ ¼ supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Simplified Schematic

¼ Quad



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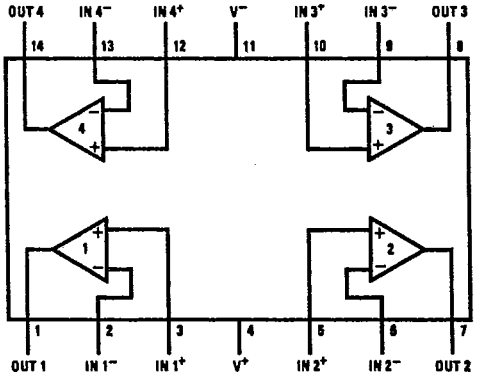
Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



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Top View

Order Number LF444AMD, LF444CD, LF444CJ, LF444CM, LF444CWM, LF444ACN or LF444CN
See NS Package Number D14E, J14A, M14A, M14B or N14A

Ordering Information

LF444XYZ

X Indicates electrical grade

Y Indicates temperature range
"M" for military, "C" for commercial

Z Indicates package type "D", "M" or "N"

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	D Package	N, WM Packages
Power Dissipation (Notes 3 and 9)	900 mW	670 mW
T_J max	150°C	115°C
θ_{JA} (Typical)	100°C/W	85°C/W

	LF444A/LF444 (Note 4)
Operating Temperature Range	
Storage Temperature Range	$-65°C \le T_A \le 150°C$
ESD rating to be determined.	
Soldering Information	
Dual-In-Line Packages (Soldering, 10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10k, T_A = 25°C$			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_J = 25°C$		5	25		5	50	pA
			$T_J = 70°C$			1.5			1.5	nA
			$T_J = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_J = 25°C$		10	50		10	100	pA
			$T_J = 70°C$			3			3	nA
			$T_J = 125°C$			20				nA
R_{IN}	Input Resistance	$T_J = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 10\ k\Omega, T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.8	1.0	mA

AC Electrical Characteristics (Note 5)

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Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1$ kHz		35			35		nV/√Hz
I_n	Equivalent Input Noise Current	$T_A = 25°C$, $f = 1$ kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

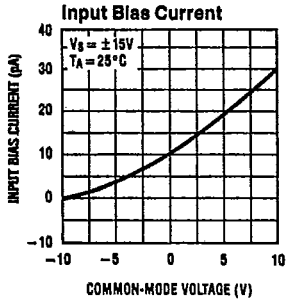
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

Note 8: Refer to RETS444AX for LF444AMD military specifications.

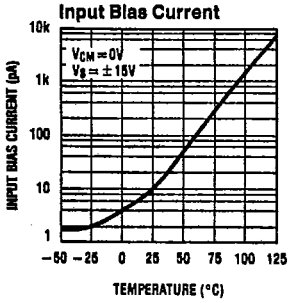
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

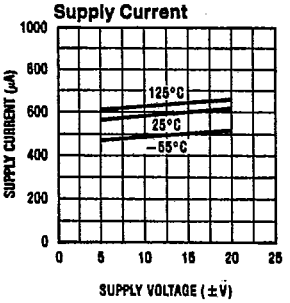
Input Bias Current



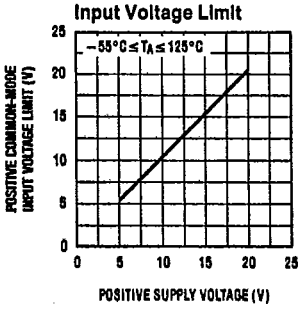
Input Bias Current



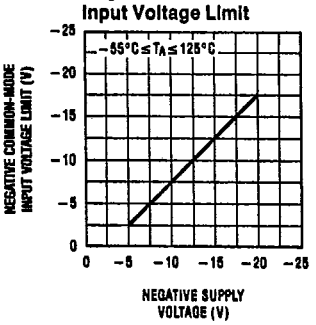
Supply Current



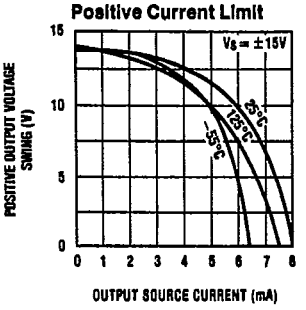
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



Positive Current Limit



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Typical Performance Characteristics (Continued)

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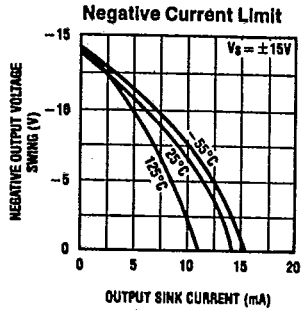
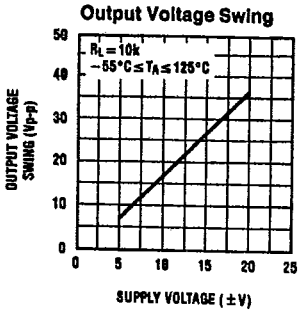
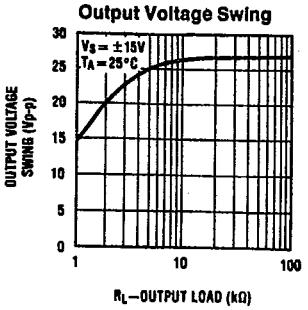
Negative Current Limit



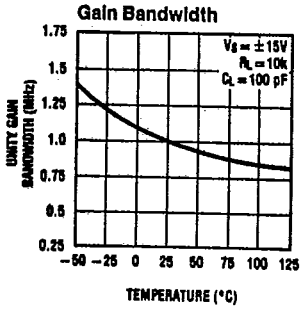
Output Voltage Swing



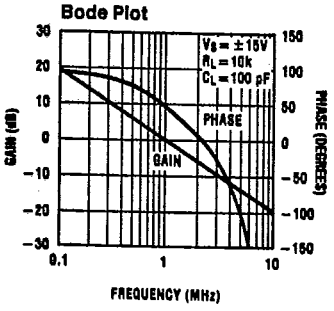
Output Voltage Swing



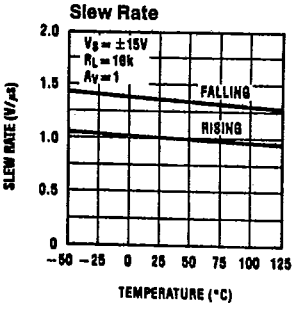
Gain Bandwidth



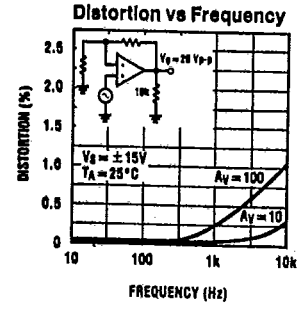
Bode Plot



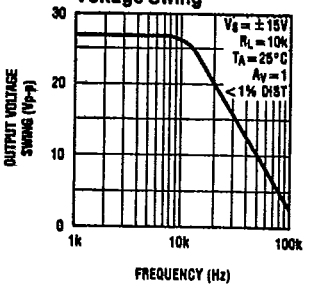
Slew Rate



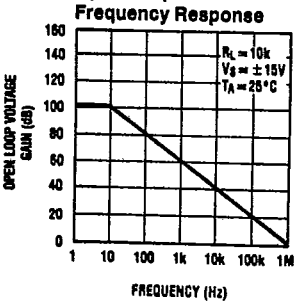
Distortion vs Frequency



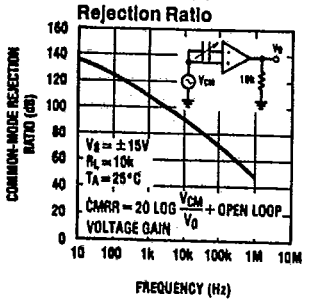
Undistorted Output Voltage Swing



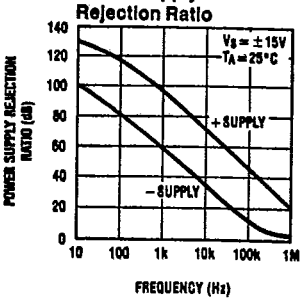
Open Loop Frequency Response



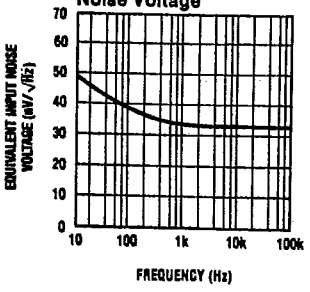
Common-Mode Rejection Ratio



Power Supply Rejection Ratio



Equivalent Input Noise Voltage



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Typical Performance Characteristics (Continued)

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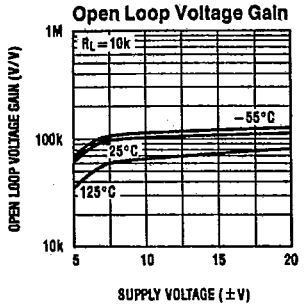
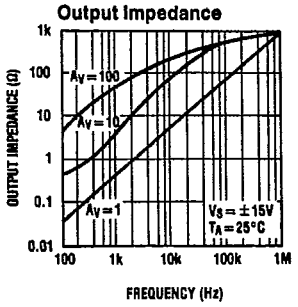
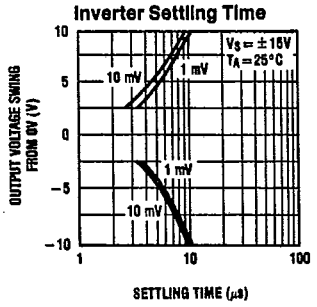
Open Loop Voltage Gain



Output Impedance



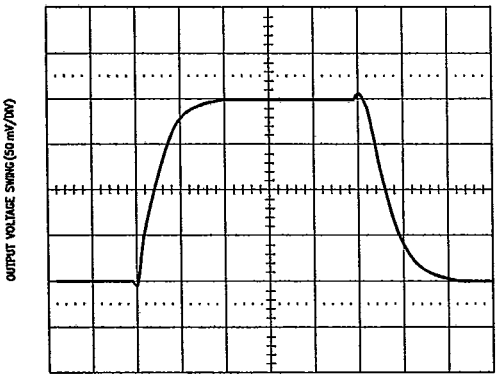
Inverter Settling Time



TL/H/9156-5

Pulse Response $R_L = 10\,k\Omega$, $C_L = 10\,pF$

Small Signal Inverting



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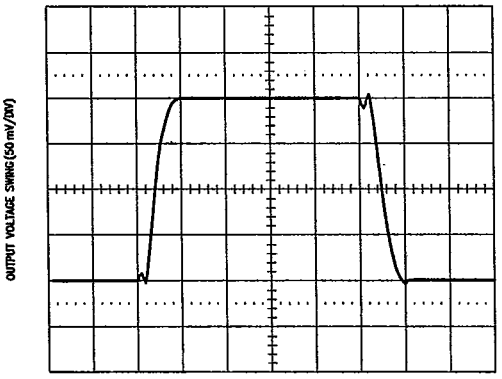
Small Signal Non-Inverting



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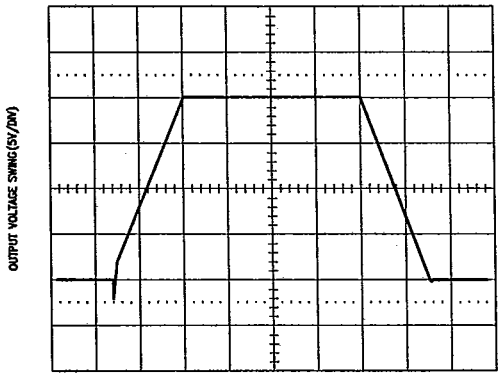
Large Signal Inverting



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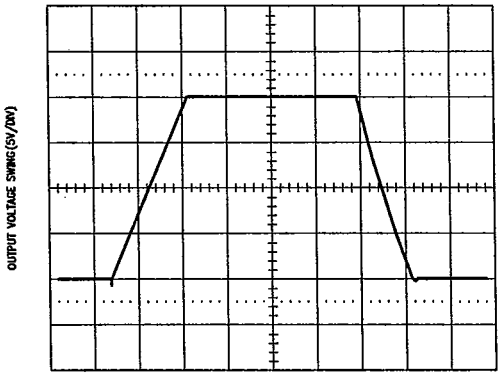
Large Signal Non-Inverting



TL/H/9156-9

Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

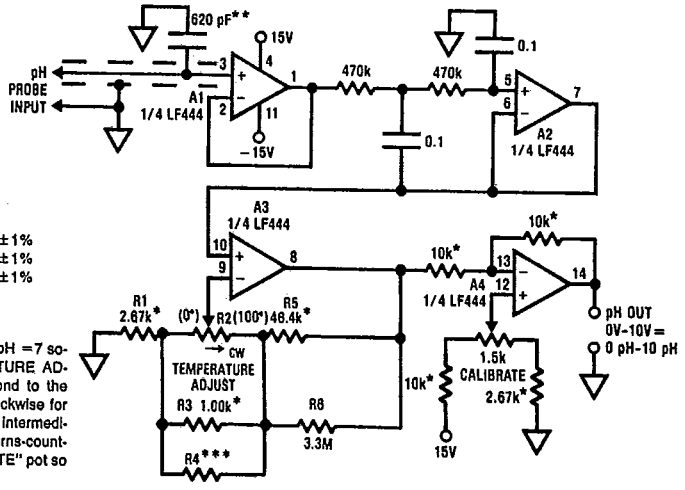
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%

**Polystyrene

*Film resistor type RN60C

To calibrate, insert probe in pH = 7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set "CALIBRATE" pot so output reads 7V.

Typical probe = Ingold Electrodes #465-35

TL/H/9156–10

Detailed Schematic

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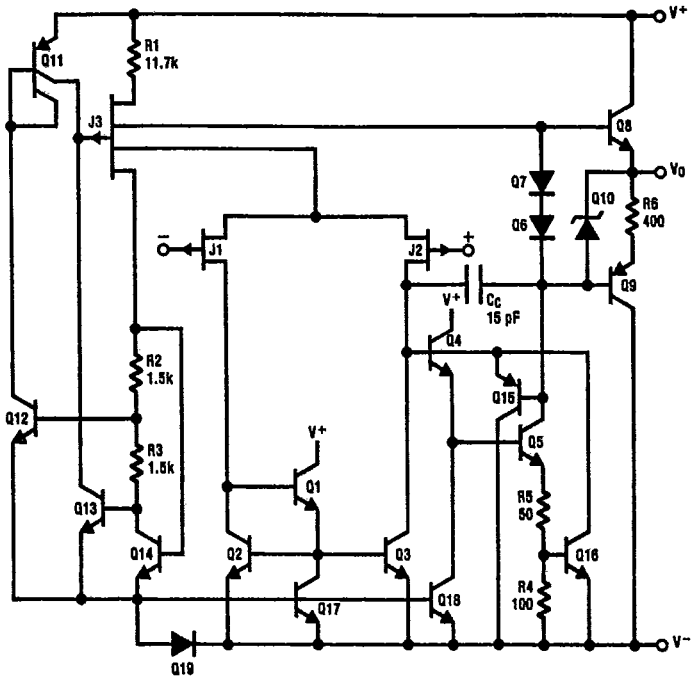
¼ Quad



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