LF48908
Two Dimensional Convolver

FEATURES

- 40 MHz Data and Computation Rate
- Nine Multiplier Array with 8-bit Data and 8-bit Coefficient Inputs
- Separate Cascade Input and Output Ports
- On-board Programmable Row Buffers
- Two Coefficient Mask Registers
- On-board 8-bit ALU
- Two's Complement or Unsigned Operands
- Replaces Harris HSP48908
- DECC SMD No. 5962-93007
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack

DESCRIPTION

The **LF48908** is a high-speed two dimensional convolver that implements a 3 x 3 kernel convolution at real-time video rates. Programmable row buffers are located on-chip, eliminating the need for external data storage. Each row buffer can store up to 1024 pixels. Two internal register banks are provided allowing two separate sets of filter coefficients to be stored simultaneously. Adaptive filter operations are possible when both register banks are used. An on-chip ALU is provided, allowing real-time arithmetic and logical pixel point operations to be performed on the image data. The 3 x 3 convolver comprises nine 8 x 8-bit multipliers, various pipeline registers, and summers. A complete sum-of-products operation is performed every clock cycle. The $\overline{\text{FRAME}}$ signal resets all data registers without affecting the control and coefficient registers.

Pixel and coefficient input data are both 8-bits and can be either signed or unsigned integers. Image data should be in a raster scan non-interlaced format. The LF48908 can internally store images as wide as 1024 pixels for the 3 x 3 convolution. By using external row buffers and multiple LF48908s, longer pixel rows can be used and convolutions with larger kernel sizes can be performed. Output data is 20-bits and this guarantees no overflow for kernel sizes up to 4 x 4. A separate cascade input is used as the data input for summing results from multiple LF48908s. It can also function as the data input path when external line buffers are used.

FIGURE 1. LF48908 BLOCK DIAGRAM

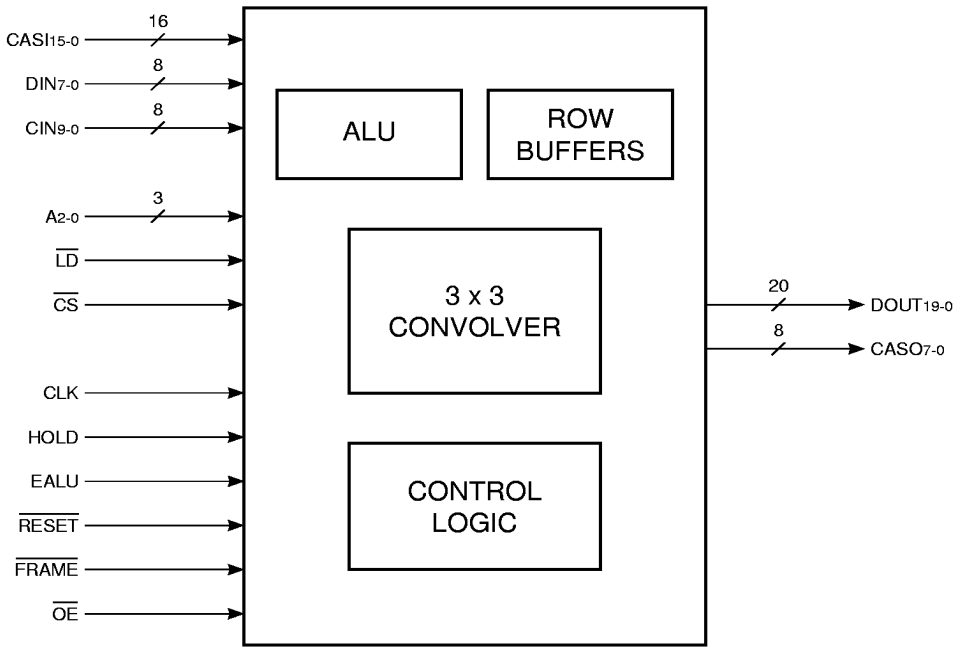

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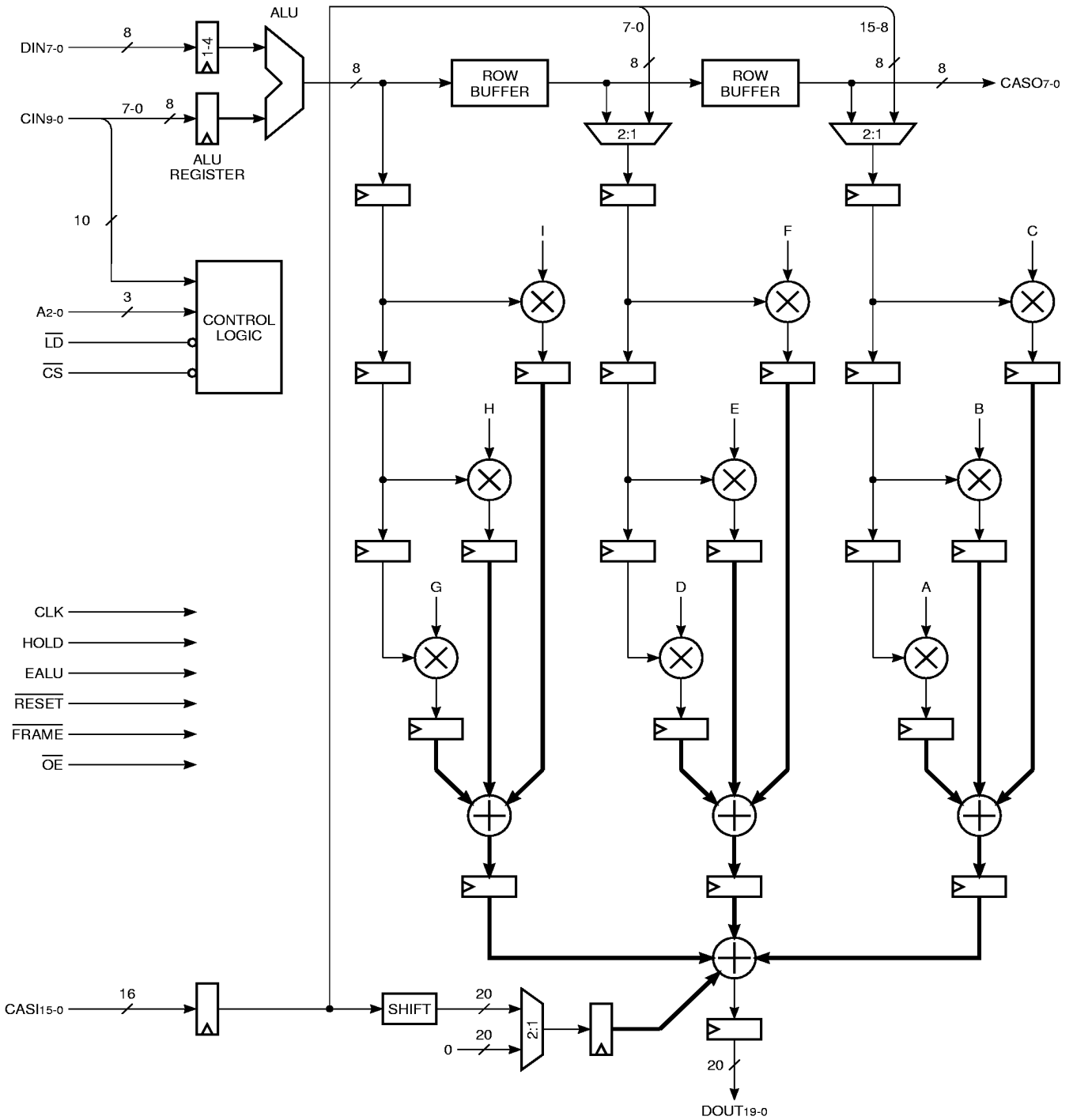
FIGURE 2. LF48908 FUNCTIONAL BLOCK DIAGRAM



NOTE: NUMBERS IN REGISTER INDICATE NUMBER OF PIPELINE DELAYS.

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SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers except for the Control Logic Registers.

Inputs

DIN7-0 — Pixel Data Input

DIN7-0 is the 8-bit registered pixel data input port. Data is latched on the rising edge of CLK.

CIN9-0 — Coefficient and Control Logic Register Input

CIN7-0 is used to load the Coefficient Registers or can be used to provide a second operand input to the ALU. CIN8-0 is used to load the Initialization Register. CIN9-0 is used to load the ALU Microcode and Row Buffer Length Registers. The Control Register Address Lines, A2-0, determine which register will receive the CIN data. The CIN data is loaded into the addressed register by using the $\overline{CS}$ and $\overline{LD}$ control inputs.

CASI15-0 — Cascade Input

The cascade input is used when multiple LF48908s are cascaded together or when external row buffers are needed. This allows convolutions of larger kernels or longer row sizes.

Outputs

DOUT19-0 — Data Output

DOUT19-0 is the 20-bit registered data output port.

CASO7-0 — Cascade Output

The data presented on CASO7-0 is the internal ALU output delayed by twice the programmed internal row buffer length.

Controls

$\overline{RESET}$ — Reset Control

When $\overline{RESET}$ is LOW, all internal circuitry is reset, all outputs are forced LOW, all Control Logic Registers are loaded with their default values (which is 0 for each one except the ALU Microcode Register which has a default value of "0000011000"), and all other internal registers are loaded with a "0".

$\overline{FRAME}$ — New Frame Input Control

When asserted, $\overline{FRAME}$ signals the start of a new frame. When $\overline{FRAME}$ is LOW, all internal circuitry is reset except for the ALU Microcode, Row Length, Initialization, Coefficient, and ALU Registers.

EALU — Enable ALU Register Input

When HIGH, data on CIN7-0 is latched into the ALU Register on the next rising edge of CLK. When LOW, data on CIN7-0 will not be latched into the ALU Register and the register contents will not be changed.

HOLD — Hold Control

The HOLD input is used to disable CLK from all of the internal circuitry. HOLD is latched on the rising edge of CLK and takes effect on the next rising edge of CLK. When HOLD is HIGH, CLK will have no effect on the LF48908 and all internal data will remain unchanged.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, DOUT19-0 is enabled for output. When $\overline{OE}$ is HIGH, DOUT19-0 is placed in a high-impedance state.

A2-0 — Control Logic Address Lines

A2-0 determines which Control Logic Register will receive the CIN9-0 data.

$\overline{CS}$ — Chip Select

When $\overline{CS}$ is LOW, data can be loaded into the Control Logic Registers. When $\overline{CS}$ is HIGH, data can not be loaded and the register contents will not be changed.

$\overline{LD}$ — Load Strobe

If $\overline{CS}$ and $\overline{LD}$ are LOW, the data present on CIN9-0 will be latched into the Control Logic Register addressed by A2-0 on the rising edge of $\overline{LD}$.

FUNCTIONAL DESCRIPTION

The LF48908, a two-dimensional convolver, executes convolutions using internal row buffers to reduce design complexity and board space requirements. 8-bit image data, in raster scan, non-interlace format, is convolved with one of two internal, 3 x 3 user-programable filter kernels. Two 1024 x 8-bit row buffers provide the data delay needed to perform two-dimensional convolutions on a single chip. The result output of 20-bits allows for word growth during the convolution operation.

The input data path (DIN7-0) provides access to an 8-bit ALU. This allows point operations to be performed on the incoming data stream before reaching the row buffers and the convolver. The length of these buffers is programmable for use in various video formats without the need for additional external delay.

This device is configured by loading the coefficent data (filter kernels) and row buffer length through the coefficent data path (CIN7-0). Internal registers are addressed using the A2-0 address lines. Chip Select ($\overline{CS}$) and Load Strobe ($\overline{LD}$) complete the configuration interface which may be controlled by standard microprocessors without additional external logic.

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The filtered image data is output on the Data Output bus (DOUT19-0). This bus is registered with three-state drivers to facilatate use on a standard microprocessor system bus.

Data Input

Image data is input to the 3 x 3 convolver using DIN7-0. Data present on DIN7-0 is latched into a programmable pipeline delay on the rising edge of CLK. The programmable pipeline delay (1 to 4 clock cycles) allows for synchronization of input data when multiple LF48908s are cascaded together to perform larger convolutions. This delay is programed via the Initialization Register (see Table 3). The image data format, unsigned or two's complement, is also controlled by this register.

Coefficient data is input to the 3 x 3 convolver using either of two Coefficient Registers (CREG0 or CREG1). The Coefficient Registers are loaded through CIN7-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. The coefficient data format, unsigned or two's complement, is determined by the Initialization Register.

Arithmetic Logic Unit

The input data path ALU with shifter allows pixel point operations to be performed on the incoming image. These operations include arithmetic functions, logical masking, and left/right shifts. The 10-bit ALU Microcode Register controls the various operations. The three upper bits control the shift amount and direction while the seven lower bits determine the arithmetic or logical operation. The shift operation is performed on the output of the ALU. This shift operation is independent of the arithmetic or logical operation of the ALU.

Tables 1 and 2 show the operations of the ALU Microcode Register. The "A" operand comes from the DIN input data path, while the "B" operand is taken from the ALU Register. The ALU Register is loaded using CIN7-0 and EALU. With EALU HIGH, data from CIN7-0 is loaded into the ALU Register on the rising edge of CLK. With EALU LOW, the data is held in the ALU Register. Since CIN7-0 is also used to load the Control Logic Registers, it is possible to overwrite data in those registers if $\overline{CS}$ and $\overline{LD}$ are active when loading the ALU Register. Therefore, special care must be taken to ensure that $\overline{CS}$ and $\overline{LD}$ are not active when writing to the ALU Register.

Programmable Row Buffers

The two internal row buffers provide the delay needed to perform the two-dimensional convolution. The row buffers function like 8-bit serial shift registers with a user-programmable delay from 1 to 1024 stages (it is possible to select delay stages of 1 or 2, but this leads to meaningless results for a 3 x 3 kernel convolution). The row buffer length is set via the Row Length Register (see Row Length Register Section). The row buffers are connected in series to provide the proper pixel information to the multiplier array. The Cascade Output (CASO7-0) provides a 2X row delay of the input data allowing for cascading of LF48908s to handle larger frames and/or kernel sizes. If more than 1024 delay stages are needed, it is possible to use external row buffers and bypass the internal row buffers. Bit 0 of the Initialization Register determines if internal or external row buffers are used. If Bit 0 is a "0", the internal row buffers are used. If Bit 0 is a "1", the internal row buffers are bypassed and external row buffers may be used.

3 x 3 Multiplier Array

The multiplier array comprises nine 8 x 8-bit multipliers. The active Coefficient Register supplies the coefficents to each of the multipliers, while the pixel data comes from the data input path and row buffers. The array forms a sum-of-products result as defined by the equation listed in Figure 3.

CONTROL LOGIC

Four sets of registers, the ALU Microcode, Row Length, Initialization, and Coefficient, define the Control Logic section. These registers are updated

FIGURE 3. MULTIPLIER ARRAY OUTPUT

PIXEL INPUT DATA

P1	P2	P3
P4	P5	P6
P7	P8	P9

FILTER KERNEL

A	B	C
D	E	F
G	H	I

MULTIPLIER ARRAY OUTPUT = A(P1) + B(P2) + C(P3)
+ D(P4) + E(P5) + F(P6)
+ G(P7) + H(P8) + I(P9)

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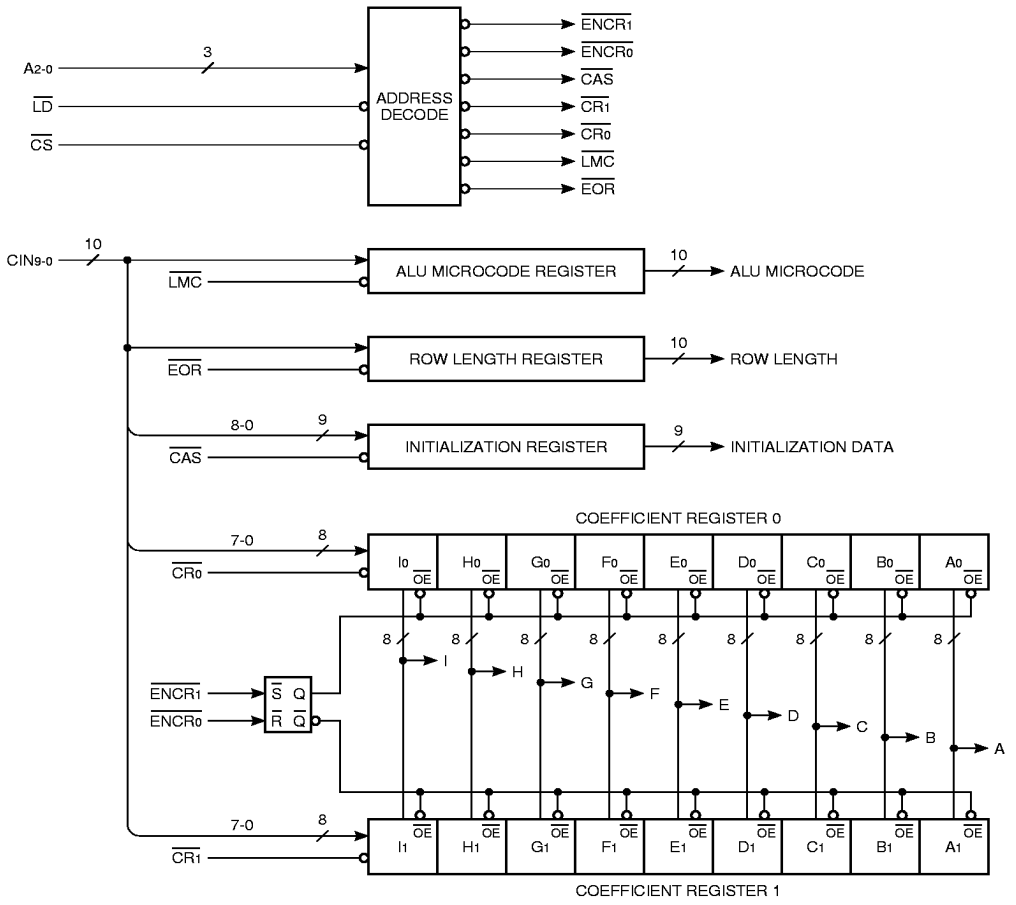
FIGURE 4. LF48908 CONTROL LOGIC BLOCK DIAGRAM



through the CIN bus using A2-0, $\overline{CS}$, and $\overline{LD}$ (see Figure 4). All the Control Logic Registers are set to their default values when $\overline{RESET}$ is active. $\overline{FRAME}$ does not affect the values in these registers.

ALU Microcode Register

Operation of the ALU and shifter are determined by the value stored in the ALU Microcode Register. This 10-bit instruction word is divided into two fields. The lower seven bits define the arithmetic and logical operations of the ALU. The upper three bits specify shift distance and direction. Tables 1 and 2 detail the various instruction words. This register is loaded through CIN9-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. Also see Arithmetic Logic Unit section.

Row Length Register

The value stored in the Row Length Register determines the number of delay stages for each row buffer. The number of delay stages should be set equal to the row length of the input image. The Row Length Register may be loaded with the values 0 through 1023 (0 represents 1024 delay stages). It is possible to program the row buffers to have 1 or 2 delay stages, but this will lead to meaningless results for a 3 x 3 convolution. This register is loaded through CIN9-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. Once the Row Length Register has been loaded, a new value can not be loaded until the LF48908 has been reset. This is done by asserting $\overline{RESET}$. After $\overline{RESET}$ goes HIGH, the Row Length Register must be loaded within 1024 CLK cycles. If the Row Length Register is not loaded within 1024 CLK cycles, the register will automatically be loaded with a "0".

Initialization Register

The Initialization Register configures various functions of the device including: input data delay, input data format, coefficent data format, output rounding, cascade mode, and cascade input shift (see Table 3). This register is loaded through CIN8-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls.

Coefficient Registers - CREG0, CREG1

The Coefficient Registers are used to store the filter coefficients for the multiplier array. Each Coefficient

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TABLE 1. ALU SHIFT OPERATIONS

ALU MICROCODE REGISTER			
REGISTER BIT			
9	8	7	OPERATION
0	0	0	No Shift (Default)
0	0	1	Shift Right 1
0	1	0	Shift Right 2
0	1	1	Shift Right 3
1	0	0	Shift Left 1
1	0	1	Shift Left 2
1	1	0	Shift Left 3
1	1	1	Not Valid

TABLE 2. ALU LOGICAL AND ARITHMETIC OPERATIONS

ALU MICROCODE REGISTER							
REGISTER BIT							
6	5	4	3	2	1	0	OPERATION
0	0	0	0	0	0	0	Logical (00000000)
1	1	1	1	0	0	0	Logical (11111111)
0	0	1	1	0	0	0	Logical (A) (Default)
0	1	0	1	0	0	0	Logical (B)
1	1	0	0	0	0	0	Logical ($\overline{A}$)
1	0	1	0	0	0	0	Logical ($\overline{B}$)
0	1	1	0	0	0	1	Arithmetic (A + B)
1	0	0	1	0	1	0	Arithmetic (A – B)
1	0	0	1	1	0	0	Arithmetic (B – A)
0	0	0	1	0	0	0	Logical (A AND B)
0	0	1	0	0	0	0	Logical (A AND $\overline{B}$)
0	1	0	0	0	0	0	Logical ($\overline{A}$ AND B)
0	1	1	1	0	0	0	Logical (A OR B)
1	0	1	1	0	0	0	Logical (A OR $\overline{B}$)
1	1	0	1	0	0	0	Logical ($\overline{A}$ OR B)
1	1	1	0	0	0	0	Logical (A NAND B)
1	0	0	0	0	0	0	Logical (A NOR B)
0	1	1	0	0	0	0	Logical (A XOR B)
1	0	0	1	0	0	0	Logical (A XNOR B)

Register can hold nine 8-bit values. This allows two different 3 x 3 filter kernels to be stored simultaneously on the LF48908. The outputs of CREG0 and CREG1 are connected to the coefficient inputs of the multiplier array (A through I). The register used to supply the coefficient data is determined by the address written to the Address Decoder. If a "101" is written to the Address Decoder, CREG0 will provide the coefficient data. If a "110" is written to the Address Decoder, CREG1 will be used. It is possible to switch between the two Coefficient Registers in real time. This facilitates adaptive filtering operations. It is important to remember to meet the t_{LCS} timing specification when switching the Coefficient Registers. When a Coefficient Register is selected to supply data to the multiplier array (one of the registers is always selected), all of its outputs are enabled simultaneously. When $\overline{RESET}$ is asserted, CREG0 is the default register selected to supply the coefficient data.

CREG0 and CREG1 are loaded through CIN7-0 using the A2-0, $\overline{CS}$, and $\overline{LD}$ controls. The nine coefficient values are presented on CIN7-0 one by one, in order from A to I. As each value is placed on CIN7-0, it is latched into the selected Coefficient Register using $\overline{CS}$ and $\overline{LD}$. The register to be loaded is determined by the data on A2-0 during the load operation. If CREG0 is to be loaded, "010" must be placed on A2-0 during the load operation. If CREG1 is to be loaded, "011" must be placed on A2-0. If desired, the Coefficient Register that is not being used to send data to the multiplier array can be loaded with coefficient data while the LF48908 is in active operation.

Address Decoder

The Address Decoder is used to load the Control Logic Registers and to determine which Coefficient Register sends data to the multiplier array. To load a Control Logic Register, the address of the register must be placed on A2-0, the data to be written must be placed on the CIN bus, and $\overline{CS}$ and $\overline{LD}$ must be asserted. The data is latched into the addressed register when $\overline{LD}$ goes HIGH. To select a Coefficient Register (CREG0 or CREG1) to send data to the multiplier array, the appropriate address must be placed on A2-0, and $\overline{CS}$ and $\overline{LD}$ must be asserted. When $\overline{LD}$ goes HIGH, the addressed register will begin supplying coefficient data to the multiplier array. Table 4 lists all of the register addresses.

The Control Logic Registers can be modified during active operation of the LF48908. If this is done, it is very important to meet the t_{LCS} timing specification. This is to ensure that the outputs of the Control Logic Registers have enough time to change before the next rising edge of CLK. If t_{LCS} is not met, unexpected results may occur on DOUT19-0 for one clock cycle. There are two situations in which t_{LCS} may

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be ignored. If the LF48908 is not in active operation or if the innactive Coefficient Register is being written to during active operation.

Cascade Operation

The Cascade Input lines (CASI15-0) and Cascade Output lines (CASO7-0) are used to allow convolutions of kernel sizes larger than 3 x 3. The Cascade Input lines are also used to allow convolutions on row lengths longer than 1024 pixels. The Cascade Mode Bit (Bit 0) of the Initialization Register determines the function of the Cascade Input lines. If the Cascade Mode Bit is a "0", then the Cascade Input lines are to be used to cascade multiple LF48908s together to perform convolutions of larger kernel sizes. CASI15-0 will be left shifted (by an amount determined by bits 7 and 8 of the Initialization Register) and then added to DOUT19-0. Cascading is accomplished by connecting CASO7-0 and DOUT19-0 of one LF48908 to DIN7-0 and CASI15-0 respectively of another LF48908. If the Cascade Mode Bit is a "1", then the Cascade Input lines are to be used with external row buffers to allow for longer row lengths. In this mode, the Cascade Input lines are split into two 8-bit data busses (CASI15-8 and CASI7-0) which are fed directly into the multiplier array.

TABLE 3. INITIALIZATION REGISTER

BIT		FUNCTION
0		**CASCADE MODE**
0		Multiplier input from internal row buffers
1		Multiplier input from external buffers
2	**1**	**INPUT DATA DELAY**
0	0	No data delay registers used
0	1	One data delay register used
1	0	Two data delay registers used
1	1	Three data delay registers used
3		**INPUT DATA FORMAT**
0		Unsigned integer format
1		Two's complement format
4		**COEFFICIENT DATA FORMAT**
0		Unsigned integer format
1		Two's complement format
6	**5**	**OUTPUT ROUNDING**
0	0	No rounding
0	1	Round to 16 bits (i.e. DOUT19-4)
1	0	Round to 8 bits (i.e. DOUT19-12)
1	1	Not valid
8	**7**	**CASI15-0 INPUT SHIFT**
0	0	No shift
0	1	Shift CASI15-0 left two
1	0	Shift CASI15-0 left four
1	1	Shift CASI15-0 left eight

TABLE 4. CONTROL LOGIC ADDRESS MAP

A2-0	FUNCTION
000	Load Row Buffer Length Register
001	Load ALU Microcode Register
010	Load Coefficient Register 0
011	Load Coefficient Register 1
100	Load Initialization Register
101	Select Coefficient Register 0 for Internal Processing
110	Select Coefficient Register 1 for Internal Processing
111	No Operation

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MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.8			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			110	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

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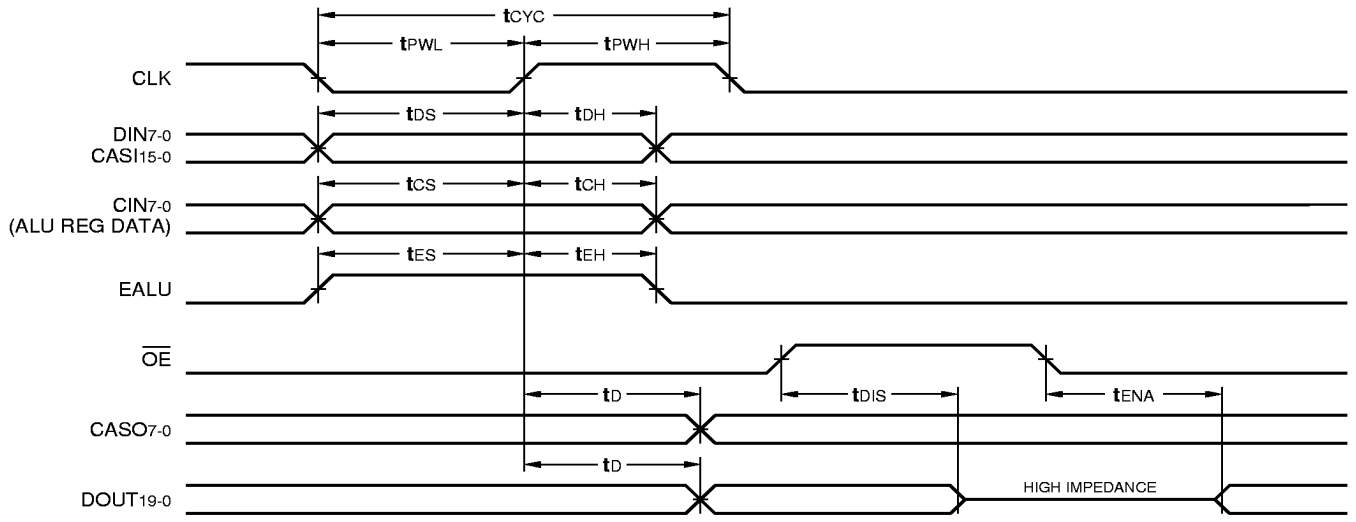
SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48908–					
		50		31		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		31		25	
t_{PWH}	Clock Pulse Width High	20		12		8	
t_{PWL}	Clock Pulse Width Low	20		13		8	
t_{DS}	Data Input Setup Time	14		13		8	
t_{DH}	Data Input Hold Time	0		0		0	
t_{CS}	CIN_{7-0} Setup Time	16		14		10	
t_{CH}	CIN_{7-0} Hold Time	0		0		0	
t_{ES}	EALU Setup Time	14		12		10	
t_{EH}	EALU Hold Time	0		0		0	
t_D	Output Delay		22		16		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		16		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		32		28		8

SWITCHING WAVEFORMS: CONVOLVER DATA I/O



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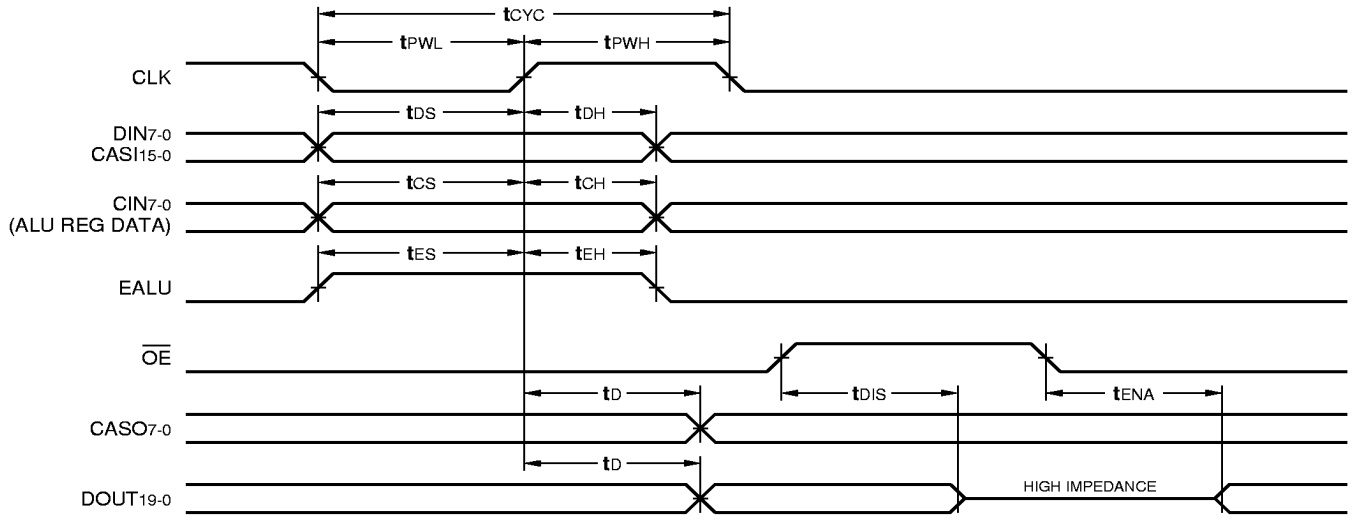
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48908– 50* Min	50* Max	37* Min	37* Max	25* Min	25* Max
t_{CYC}	Cycle Time	50		37		25	
t_{PWH}	Clock Pulse Width High	20		15		8	
t_{PWL}	Clock Pulse Width Low	20		15		8	
t_{DS}	Data Input Setup Time	17		16		8	
t_{DH}	Data Input Hold Time	0		0		0	
t_{CS}	CIN_{7-0} Setup Time	20		17		10	
t_{CH}	CIN_{7-0} Hold Time	0		0		0	
t_{ES}	EALU Setup Time	17		15		10	
t_{EH}	EALU Hold Time	0		0		0	
t_{D}	Output Delay		28		19		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		28		19		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		40		35		8

SWITCHING WAVEFORMS: CONVOLVER DATA I/O



*DISCONTINUED SPEED GRADE

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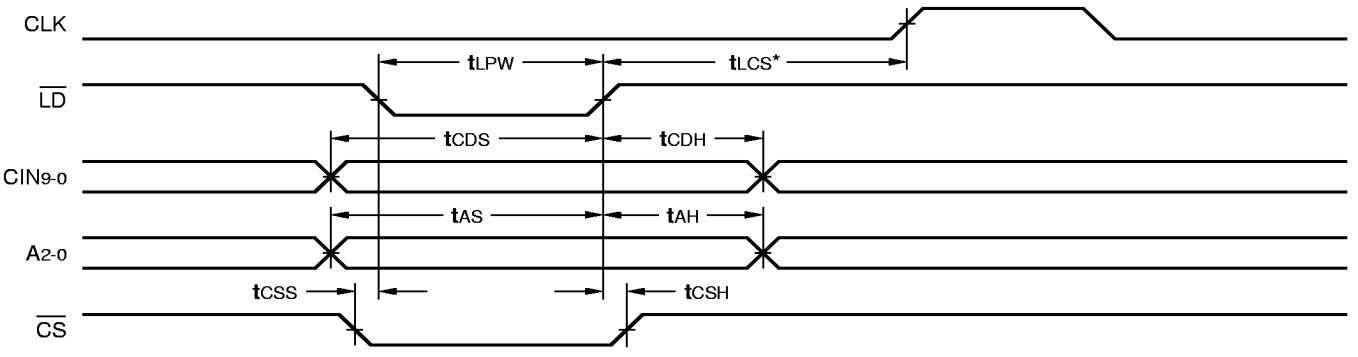
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48908– 50 Min	50 Max	31 Min	31 Max	25 Min	25 Max
t_{LPW}	$\overline{LD}$ Pulse Width	20		12		8	
t_{LCS}	$\overline{LD}$ Setup Time (Applies only during active operation)	30		25		15	
t_{CDS}	Configuration Data Setup Time	16		14		10	
t_{CDH}	Configuration Data Hold Time	0		0		0	
t_{AS}	Address Setup Time	13		13		10	
t_{AH}	Address Hold Time	0		0		0	
t_{CSS}	$\overline{CS}$ Setup Time	0		0		0	
t_{CSH}	$\overline{CS}$ Hold Time	0		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48908– 50* Min	50* Max	37* Min	37* Max	25* Min	25* Max
t_{LPW}	$\overline{LD}$ Pulse Width	20		15		8	
t_{LCS}	$\overline{LD}$ Setup Time (Applies only during active operation)	37		30		15	
t_{CDS}	Configuration Data Setup Time	20		17		10	
t_{CDH}	Configuration Data Hold Time	0		0		0	
t_{AS}	Address Setup Time	15		15		10	
t_{AH}	Address Hold Time	0		0		0	
t_{CSS}	$\overline{CS}$ Setup Time	0		0		0	
t_{CSH}	$\overline{CS}$ Hold Time	0		0		0	

SWITCHING WAVEFORMS: CONFIGURATION DATA



*applies only when the LF48908 is in active operation.

*DISCONTINUED SPEED GRADE

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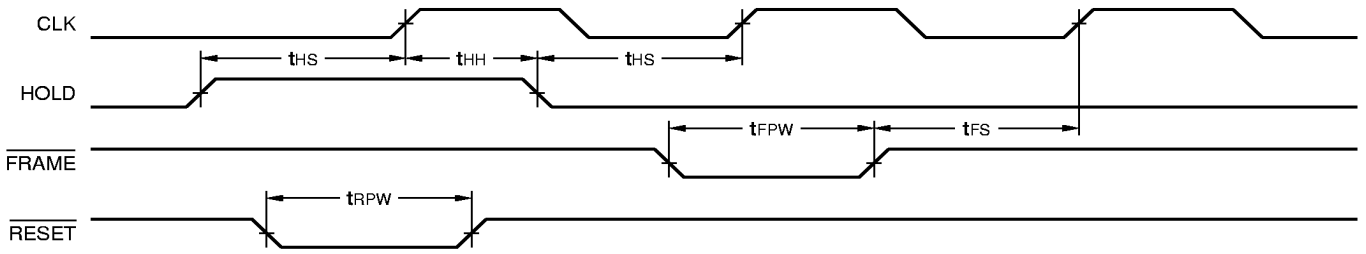
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48908– 50 Min	50 Max	31 Min	31 Max	25 Min	25 Max
t_{HS}	HOLD Setup Time	12		11		9	
t_{HH}	HOLD Hold Time	1		1		0	
t_{FPW}	$\overline{\text{FRAME}}$ Pulse Width	50		31		8	
t_{FS}	$\overline{\text{FRAME}}$ Setup Time	25		21		20	
t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	50		31		8	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF48908– 50* Min	50* Max	37* Min	37* Max	25* Min	25* Max
t_{HS}	HOLD Setup Time	14		13		9	
t_{HH}	HOLD Hold Time	2		2		0	
t_{FPW}	$\overline{\text{FRAME}}$ Pulse Width	50		37		8	
t_{FS}	$\overline{\text{FRAME}}$ Setup Time	30		25		20	
t_{RPW}	$\overline{\text{RESET}}$ Pulse Width	50		37		8	

SWITCHING WAVEFORMS: CONTROL SIGNALS



*DISCONTINUED SPEED GRADE

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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

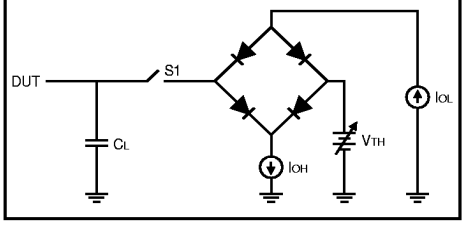
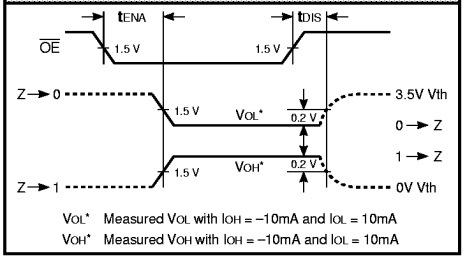


FIGURE B. THRESHOLD LEVELS



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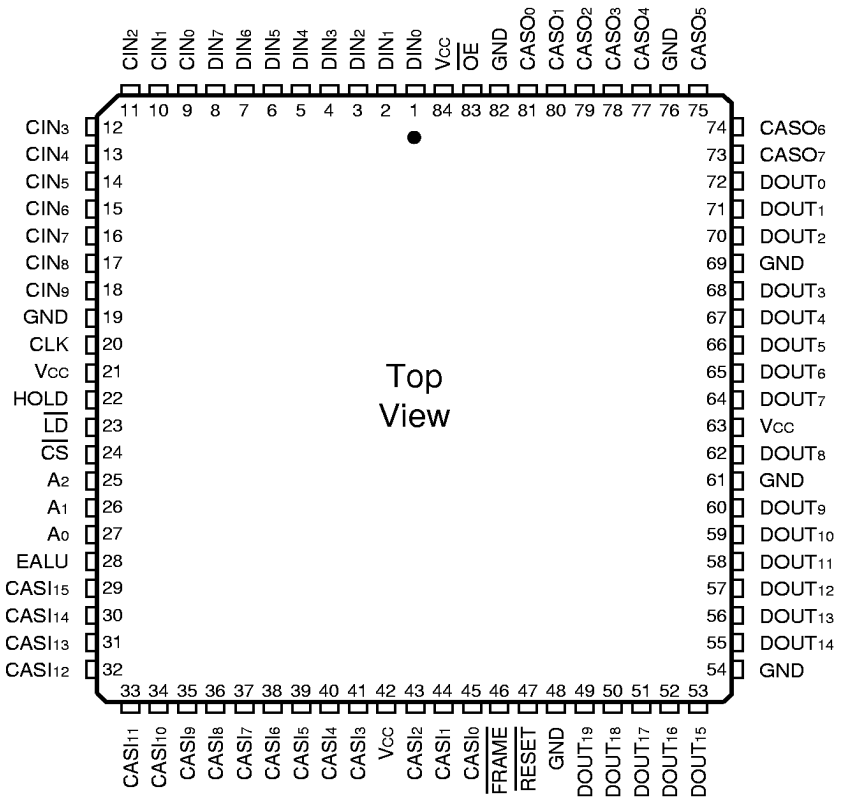
ORDERING INFORMATION

84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — Commercial Screening
50 ns	LF48908JC50
31 ns	LF48908JC31
25 ns	LF48908JC25
	–40°C to +85°C — Commercial Screening
31 ns	LF48908JI31
25 ns	LF48908JI25

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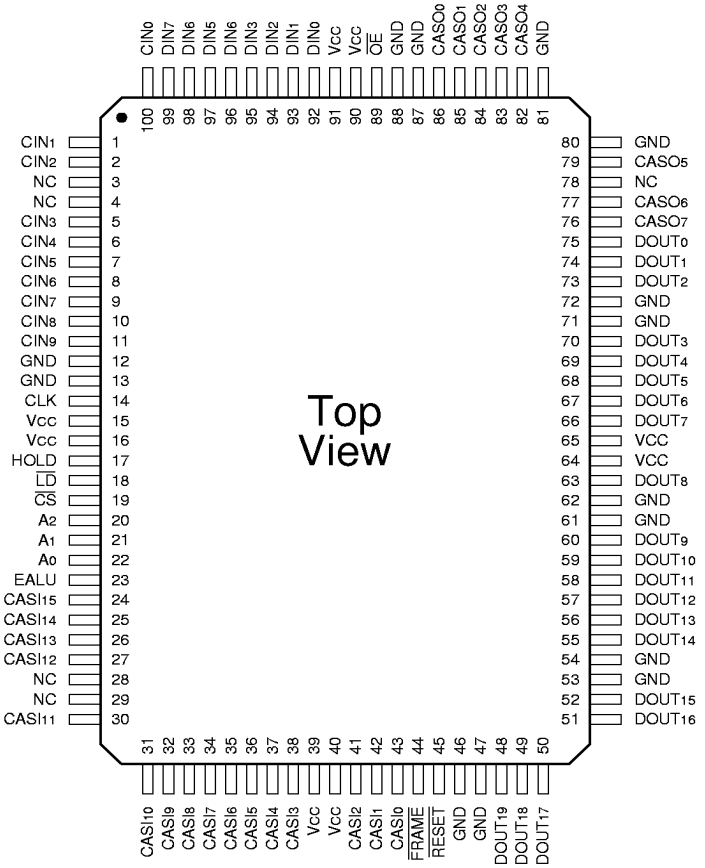
ORDERING INFORMATION

100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — Commercial Screening
31 ns	LF48908QC31
25 ns	LF48908QC25
	–40°C to +85°C — Commercial Screening

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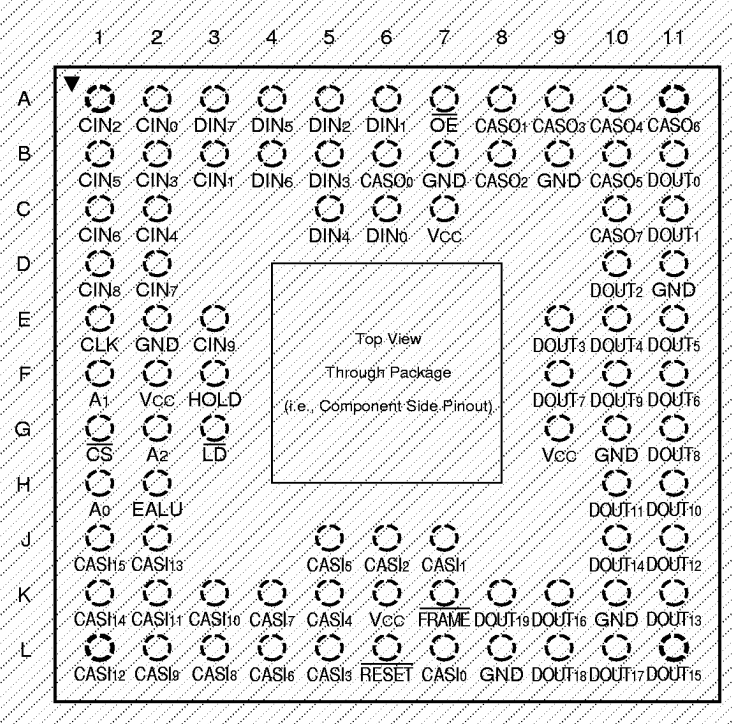
ORDERING INFORMATION

84-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G6)
	0°C to +70°C — Commercial Screening
	–55°C to +125°C — Commercial Screening
	–55°C to +125°C — MIL-STD-883 Compliant

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