Preliminary

D7002A

Single-Chip Speech Compression IC for PC Voice/Telephony Applications

GENERAL DESCRIPTION

The D7002A chipset is a digital speech/signal processing subsystem that implements all the functions of speech compression, telephone line signal processing, memory management and voice data transfer between the HOST and the internal message buffer. Additional features include DIGITAL SPEAKERPHONE™, FLEXISPEECH™ variable-speed playback, and natural-sounding voice prompting for integrated PC applications. The D7002A is fully controlled by the PC through a simple interface protocol. The PC provides activation and control of all chipset functions.

The chipset's programmability enables a full range of PC Voice/Telephony features for the end user. The D7002A is a single-chip, digital signal processor that includes all of the necessary circuitry to interface with an external HOST, memory, and an analog front end.

FEATURES

- High-quality speech compression of 6.8 kbits/second (9.4:1)
- Message buffer provides autonomous operation of PC's powered-down or operating state
- Efficient scheme for transferring voice messages between the message buffer and the host
- Complete set of telephone line monitoring and management with tone detection and generation
- FLEXISPEECH™ – variable-speed playback
- DIGITAL SPEAKERPHONE™ — high-quality hands-free telephone
- Voice/FAX Switchbers for speed dialing
- Suspend mode
- Simple host protocol for fast integration

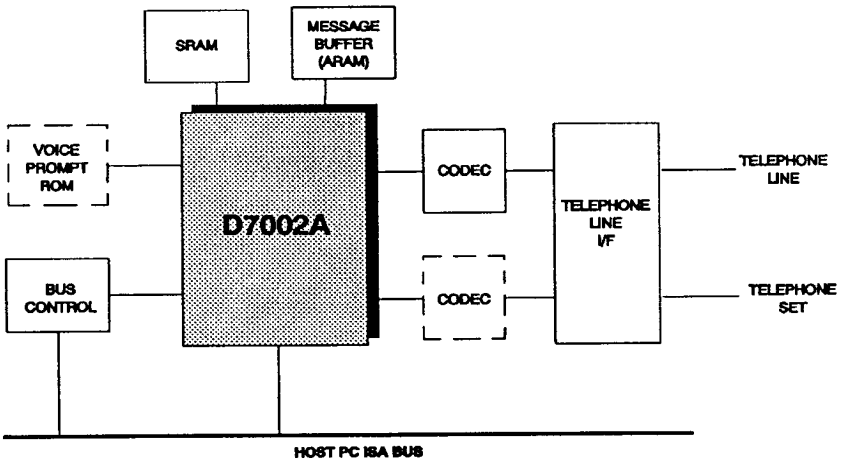

Figure 1. D7002A Block Diagram

All specifications are subject to change without prior notice

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CHIPSET BASIC CONFIGURATION

- D7002A-11 Digital Telephone Answering Device (TAD) Processor (80-pin PQFP)— 1 each
- D0000-29 Analog I/O Interface (16-pin DIP)— 1 each (2 for Speakerphone)
- D0000-34A 4-Mbit ARAM Message Memory (SOJ)— Up to four devices per chipset

Notes:

1. An 8K x 8 SRAM (access time is 100 ns) will be supplied by the customer for basic operation of the D7002A.
2. A minimum of 16K x 8 SRAM is required for activation of FlexiSpeech.
3. For Voice Prompt storage an external EPROM/ROM (access time is 300 ns) is required. Each 8K x 8 block will support 9.5 seconds of voice prompts (up to 64K).
4. SRAM message storage will be supported for an SRAM size of 16K x 8 or more. Each additional 8 Kbytes increases the maximum length of the SRAM message by 9.5 seconds, in addition to the 5 seconds stored in the first 16 Kbytes.

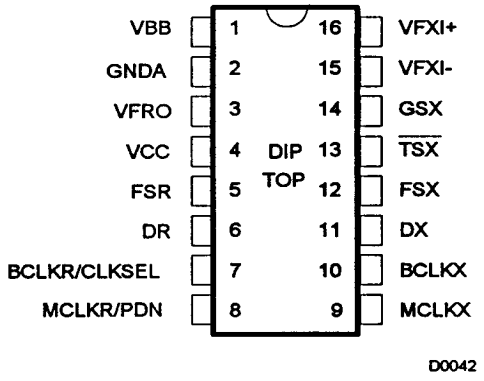

Figure 2. D0000-29

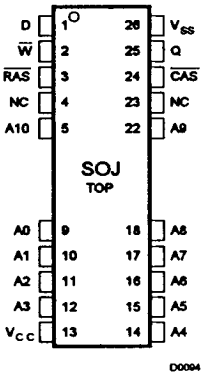

Figure 3. D0000-34A (SOJ)

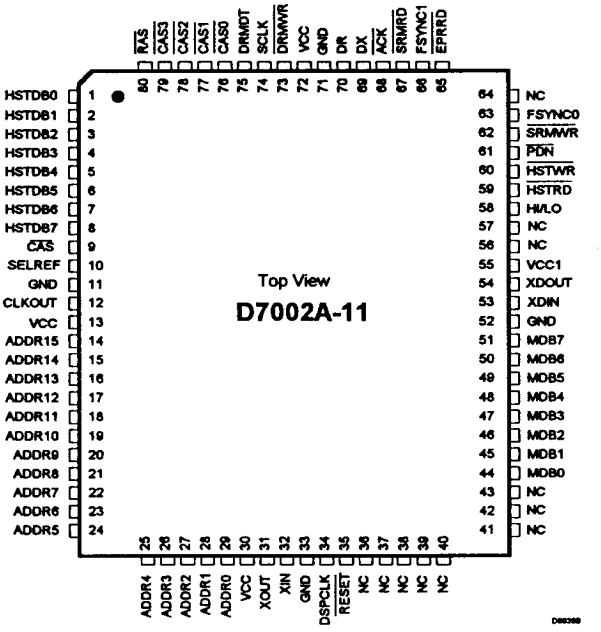

Figure 4. D7002A -11

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PIN DESCRIPTIONS

D7002A-11 (DSP)			
Pin		I/O/Z*	Description
Name	No.		
HSTDB0 (LSB)	1	I/O/Z	HOST DATA BUS. The HOST writes commands and reads status to/from the D6275A via this bus. The HI/LO pin selects between the low byte and the high byte of the command/status. This bus is used for input when HSTWR is low, and for output when HSTRD is low. It has high impedance when HSTWR and HSTRD are high or RESET is low.
HSTDB1	2	I/O/Z	
HSTDB2	3	I/O/Z	
HSTDB3	4	I/O/Z	
HSTDB4	5	I/O/Z	
HSTDB5	6	I/O/Z	
HSTDB6	7	I/O/Z	
HSTDB7 (MSB)	8	I/O/Z	
$\overline{\text{HI/LO}}$	58	I	HIGH/LOW BYTE SELECT. When this signal is low, the HOST can read/write the low byte of the status/command. When high, the high byte is selected.
$\overline{\text{HSTRD}}$	59	I	HOST READ. When low, the HOST reads the low/high byte of the status word.
$\overline{\text{HSTWR}}$	60	I	HOST WRITE. When low the HOST writes commands to the D6275A via HSTDB 0-7.
$\overline{\text{ACK}}$	68	O	HOST ACKNOWLEDGE. This pin goes low when the D6275A sends a status word to the HOST. It goes high when the HOST reads the high byte of the status word.
ADDR0 (LSB)	29	O	EXTERNAL MEMORY ADDRESS BUS
ADDR1	28	O	
ADDR2	27	O	
ADDR3	26	O	
ADDR4	25	O	
ADDR5	24	O	
ADDR6	23	O	
ADDR7	22	O	
ADDR8	21	O	
ADDR9	20	O	
ADDR10	19	O	
ADDR11	18	O	
ADDR12	17	O	
ADDR13	16	O	
ADDR14	15	O	
ADDR15 (MSB)	14	O	
$\overline{\text{SRMRD}}$	67	O	SRAM READ. (active low)
$\overline{\text{SRMWR}}$	62	O	SRAM WRITE. (active low)
$\overline{\text{EPRRD}}$	65	O	Voice prompt ROM/EPROM read (active low)
MDB0 (LSB)	44	I/O/Z	External memory data bus.
MDB1	45	I/O/Z	
MDB2	46	I/O/Z	
MDB3	47	I/O/Z	
MDB4	48	I/O/Z	
MDB5	49	I/O/Z	
MDB6	50	I/O/Z	
MDB7 (MSB)	51	I/O/Z	
DRMDT	75	I/O/Z	ARAM DATA
$\overline{\text{DRMWR}}$	73	O	ARAM WRITE (active low)
$\overline{\text{CAS}}$	9	O	16 MBIT ARAM CAS
$\overline{\text{CAS0}}$	76	O	4 Mbit ARAM CAS (0 for first ARAM, 1 for second ARAM, etc.)
$\overline{\text{CAS1}}$	77	O	
$\overline{\text{CAS2}}$	78	O	

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PIN DESCRIPTIONS (Continued)

D7002A-11 (DSP)			
CAS3	79	O	4 Mbit ARAM CAS (ARAM 4)
RAS	80	O	ARAM RAS
DR	70	I	Serial input for CODEC PCM data
DX	69	O	Serial output for CODEC PCM data
FSYNC0	63	O	Frame synchronization signal for CODEC 0
FSYNC1	66	O	Frame synchronization signal for CODEC 1
SCLK	74	O	Clock output to CODEC
XIN	32	I	Crystal input pin for internal oscillator. The frequency must be 34.992 Mhz in single oscillator mode and 600 KHz +/-20% in dual oscillator mode.
XOUT	31	O	Crystal output pin for internal oscillator.
DSPCLK	34	O	Crystal oscillator frequency output. This pin should be connected to XDIN when the D6275A is operating in single oscillator mode.
XDIN	53	I	Input pin from the crystal to the internal oscillator. When in dual oscillator mode, the crystal must be 34.99Mhz. When in single oscillator mode, this pin should be connected to DSPCLK.
XDOUT	54	O	rystal output pin for internal oscillator when in dual oscillator mode. When in single oscillator mode, this pin should be left unconnected.
CLKOUT	12	O	XDIN frequency divided by 4.
SELREF	10	I	ARAM refresh clock select. This pin should be left open when in single oscillator mode, and connected to GND in dual oscillator mode.
GND	52	PWR	GROUND PIN
GND	33	PWR	GROUND PIN
GND	11	PWR	GROUND PIN
GND	71	PWR	GROUND PIN
V_{CC}	30	PWR	+5V battery backed-up power supply input. This power source should be connected to the ARAMs, SRAM and voice prompt ROM/EPROM.
V_{CC}	13	PWR	
V_{CC}	72	PWR	
V_{CC1}	55	PWR	+5V non-backed-up power supply input.
PDN	61	I	V_{CC1} power fail sensor input. When a low level is detected on this pin, the D6275A enters power-down mode.
RESET	35	I	Reset input (active low)
NC	56	I	These pins should be left unconnected.
NC	57	I	
NC	64	I	
NC	36	I	
NC	37	I	
NC	38	I	
NC	39	I	
NC	40	I	
NC	41	I	
NC	42	I	
NC	43	I	

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PIN DESCRIPTIONS

D0000-29 (Analog I/O Interface)			
Pin		I/O/Z*	Description
Name	No.		
V_{BB}	1	PWR	Negative power supply pin. V_{BB} = –5V
GNDA	2	PWR	Analog ground. All signals are referenced to this pin.
VFR_O	3	O	Analog output of the receive power amplifier.
V_{CC}	4	PWR	Positive power supply pin. VCC = +5V.
FS_R	5	I	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R.
D_R	6	I	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	7	I	Logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. This input should be tied to ground.
$MCLK_R$/ PDN	8	I	Receive master clock. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	9	I	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	10	I	The bit clock which shifts out the PCM data on DX. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	11	O/Z	PCM data output which is enabled by FS_X.
FS_X	12	I	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 KHz pulse train.
TS_X	13	O	Open drain output which pulses low during the encoder time slot.
GS_X	14	O	Analog output of the transmit input amplifier. Used to externally set gain.
VFX_I–	15	I	Inverting input of the transmit input amplifier.
VFX_I+	16	I	Non-inverting input of the transmit input amplifier.

PIN DESCRIPTIONS

D0000-34 (4 MEG ARAM)			
Pin		I/O/Z*	Description
Name	No.		
A0	9	I	Row and column address bits. Row address bits are latched in the chip by the $\overline{RAS}$ signal. Column address bits are latched in by the CAS signal.
A1	10	I	
A2	11	I	
A3	12	I	
A4	14	I	
A5	15	I	
A6	16	I	
A7	17	I	
A8	18	I	
A9	22	I	
A10	5	I	
RAS	3	I	Row address strobe
CAS	24	I	Column address strobe
D	1	I	Data input
Q	25	O	Data output
W	2	I	Write enable input which selects read or write mode
VCC	13	–	+5V supply
VSS	26	–	Ground
TF	4	I	No connection

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FUNCTIONAL DESCRIPTION

HOST Interface

The host interface is an 8-bit parallel data port, used for control and status information transfer. The host controls the operation of the D7002A using a simple command protocol. D7002A status information is updated after each command.

The command and status protocol enables the host to have full control over the functions of the D7002A. The protocol is described in the next section.

Voice Message Storage—Incoming and Outgoing Messages

The D7002A message storage uses a proprietary high-quality speech compression technique at a rate of 6.8 Kbps. The compression technique used is enhanced by an error correction algorithm that enables the use of ARAM memory without degradation in speech quality.

The D7002A chipset supports up to 40.8 minutes of voice storage. Voice messages are stored in 4-Mbit ARAMs up to a maximum of 16 Megabits. Each 4-Mbit ARAM has a storage capacity of 612 seconds. The chipset supports a total of up to 64 variable-length incoming and outgoing messages. Multiple outgoing messages are supported.

A single message can be compressed and stored in the upper part of the external SRAM. The SRAM message can be used as an OGM and, due to the lower power consumption of the SRAM, this message can be backed up for much longer periods. The SRAM message is not supported in an 8 Kbyte configuration. SRAM message recording will be stopped when there is no additional space in the SRAM. No message number will be allocated to the SRAM message; a new SRAM message is recorded over the old one.

During recording, the D7002A performs telephone line monitoring. The HOST can stop recording, and delete the last n*0.9 seconds from the memory using a Record command with Tail Cut factor.

The D7002A is capable of reporting to the HOST the status of the currently available ARAM memory storage space, as well as the overall status of the ARAMs and SRAM, and the number of recorded messages.

Digital Voice-Activated Recording (VOX)

Digital voice activity detection is implemented in the D7002A and activated only in Record mode. Compression and storage of the speech signal starts upon a positive result from the voice activity detector. The voice activity detector output is reported to the HOST via a status bit every 28 ms when in Record mode. The HOST reads this status information and decides whether to stop recording this message.

Message Playback

The D7002A supports random access for playback of any recorded message. If SRAM size is 16 Kbytes or more, three playback speeds can be supported using the FLEXISPEECH technique: normal speed (x1), high speed (x1.3) and slow speed (x0.7). Playback from the beginning of a message or from a predefined offset time may be performed. During playback, the D7002A monitors the telephone line.

Message playback can be stopped by using the Pause command, which is initiated by the HOST. After Pause, playback may be resumed from the same point. Normally, during playback, the status word will contain information about the line and the playback status. If the Read Offset bit (bit 10) was set, the D7002A responds with a time offset, which corresponds to the time elapsed from the beginning of the current message.

Message Deletion

The D7002A enables selective deletion of any prerecorded message from memory. After each deletion the message directory is updated accordingly. To improve memory utilization, the D7002A supports "Garbage Collection," which eliminates empty spaces in the message memory. No deletion of the SRAM message is supported.

Message Time Stamp

The HOST may send a 16-bit time indication to the D7002A, which can be used for time stamping the recorded message. Time stamp for the SRAM message is not supported.

DTMF Detection

DTMF detection is implemented by the D7002A in software. This function may be used for remote operation of the answering device. The identification code of one of 12 detected DTMF signals is transferred to the host for further processing.

Tone Generation

16 DTMF tones and 15 other general-purpose tones can be generated by the D7002A. DTMF signals are generated in accordance with the requirements of EIA RS-470. Voice processing is disabled during tone generation. Each tone may be selected by a host controller command. Thus, the duration of the tone is controlled by the host. The host processor also controls the tone signal level.

Call Progress Tone Detection

The D7002A monitors the line for incoming telephone line signals and detects the presence of call progress tones in a predefined frequency region. The D7002A supports call progress tone detection by utilizing one of two filter/detectors: a wide filter (330-650 Hz) and a narrow one (330-500 Hz). The filter is selected during initialization (Self Test). Indication of the presence of call progress tones is transferred to the HOST, and may be used for terminating recording.

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FAX Calling Tone Detection

The D7002A monitors the line for incoming telephone line signals and detects the presence of a FAX calling tone (CNG—1100Hz). Indication of CNG tone presence is transferred to the host and may be used for Voice-FAX switch implementation.

Ringback Signal Generation

A ringback signal is generated in order to provide audio feedback to the FAX sending party. The ringback signal is a dual tone signal of 440 and 480 Hz to simulate a jingling sound.

Speed Dial Telephone Number Storage

The host may store up to 32 telephone numbers, each with up to 16 digits, in the SRAM.

Self Test and Parameter Initialization

The D7002A supports a self test function which is responsible for testing and mapping of both the ARAMs and the SRAM. The results of each device test are returned to the HOST. The initialization command can set the type of call progress tone filter, ARAM refresh mode and CODEC type.

Voice Prompt Generation

The D7002A implements high-quality Voice Prompt playback, utilizing the built-in speech decoder and an external EPROM/ROM, which stores the vocabulary. The D7002A supports up to a 64-Kbyte EPROM/ROM which allow storage of up to 76 seconds of voice prompts. The vocabulary supports up to 128 phrases or utterances. The D7002A receives the phrase number from the host as part of the Voice Prompt command, and outputs the appropriate speech segment via the CODEC-0 interface. The gap between two consecutive phrases is controlled by the host and can be as low as 0.

During playback of the Voice Prompts, the D7002A monitors the telephone line.

DIGITAL SPEAKERPHONE™

The D7002A implements a host-controllable DIGITAL SPEAKERPHONE™ algorithm. When activated, this algorithm enables enhanced speakerphone operation with programmable parameters such as loop attenuation, VOX sensitivity and switching speed for optimal performance.

Speech Data Retrieval (ARAM to HOST)

The D7002A retrieves compressed speech data from the ARAM and transfers it through the HOST communication interface.

Speech Data Storage (HOST to ARAM)

The D7002A transfers compressed speech data through the HOST communication interface and stores it in the ARAM.

OPERATIONAL DESCRIPTION

INITIAL PROCEDURE

Upon power up, the input $\overline{\text{PDN}}$ signal (pin 61) is set high, followed by the input RESET signal, which should also go high. The D7002A starts the power up procedure according to the memory status. If it is a power up after a power failure, it is likely that a Self Test & Init command has already been issued. The Self Test & Init command writes fixed patterns in several memory locations in the SRAM and ARAM; these patterns remain unchanged during a battery backed-up power failure. After power up, the D7002A checks both the ARAM and SRAM and will respond to one of the following three situations:

1. The SRAM and ARAM status are both OK (Warm start) - the D7002A reads the system parameters from the SRAM and restores the previous conditions. The message directory and all messages are saved.
2. The SRAM status is bad (Cold start) - The D7002A initializes all parameters to their default value, and all messages in the system will be lost.
3. The SRAM status is OK and the ARAM status is bad - The D7002A will restore the system parameters but will delete all ARAM messages in the directory. All ARAM messages will be lost. The SRAM message, however, will be saved and can be played back by the HOST.

After the above system initialization the D7002A will automatically perform "Garbage Collection" in order to remove gaps between messages, in case the power fail occurred before or during Garbage Collection. After completing Garbage Collection, the D7002A will send its status to the HOST and will enter Idle mode. The HOST should read this status by polling the ACK line (pin 68) and, when low, read the status word. From then on, the HOST will send a command and wait for the status word from the D7002A. For each command, a status word is expected within 1 to 28 msec (see table on page 13), except for Self Test & Init and Garbage Collection. In order to perform an appropriate power-up sequence, Host should send Read Memory Status command and determine whether it was "cold" or "warm" start by checking the number of ARAM messages (bits 0-5) and the SRAM status (bit 8).

MODES OF OPERATION

The D7002A is normally in Idle mode. Each time a command other than Idle is issued, the system will enter the new mode.From some of the modes, the system will automatically return to Idle mode after completion of the operation. Other modes (Record, Playback, Tone Generation, Line Monitoring, Voice Prompt Generation, SpeakerPhone, and Speech Data Storage/Retrieval) require Idle command to return to Idle mode.

There are 16 modes of operation. Each of these modes is entered from the monitor program through Idle mode. The 16 modes are as follows:

0. **Idle**—The D7002A performs command polling. It checks the command register in the HOST-D7002A interface and transfers to the requested operating mode.
1. **Record**—The D7002A performs speech compression and records the message to the ARAM or SRAM.*
2. **Playback**—The D7002A performs message playback using compressed speech data stored in the ARAM or SRAM.*
3. **Read Memory Status**—The D7002A returns information on the Memory status to the HOST, e.g., the number of messages stored in ARAM, the availability of memory for recording the next message, ROM checksum status and SRAM status.
4. **Write Telephone Number**—In this mode the D7002A receives a 16-digit telephone number from the HOST and stores it in the telephone number directory.
5. **Read Telephone Number**—The D7002A returns to the HOST a telephone number stored in the telephone directory under the index number given by the HOST.
6. **Tone Generation**—The D7002A generates a selected tone signal – one of 16 DTMF tones or one of 15 other general-purpose tones.*
7. **Line Monitoring**—The D7002A monitors the telephone line for the presence of DTMF signals, call progress tones and a FAX calling (CNG) tone.*
8. **Delete Message**—The D7002A can erase any selected ARAM message entry whose number is specified by the HOST from the messages directory. If the message entry number sent by the HOST is 7FH, the D7002A performs Garbage Collection, removing unused memory space between messages.
9. **Set Current Time**—The HOST sends the D7002A the current time & date stamp to be attached to the next recorded message.
10. **Get Time Stamp**—The D7002A returns to the HOST the time & date stamp asociated with the specific ARAM message.
11. **Get Available Record Time**—The D7002A reports the currently available ARAM record time.
12. **Self Test & Initialize Memory**—The D7002A performs SRAM and ARAM testing and mapping. This command contains the system initialization parameters.
13. **Voice Prompt Generation**—The D7002A implements a TRUESPEECH™ Voice Prompt playback from an external EPROM/ROM.*
14. DIGITAL SPEAKERPHONE—The D7002A implements a DIGITAL SPEAKERPHONE ™algorithm.*
15. **Speech Data Storage/Retrieval** —The D7002A provides the ability to retrieve speech data from the ARAM and transfer it through the HOST communication interface. The D7002A provides as well the ability to transfer compressed speech data through the HOST communication interface and store it in the ARAM.*

*These modes require Idle command to return to Idle mode.

DESCRIPTION OF MODES OF OPERATION

Idle

This is a polling mode in which the D7002A monitors the D7002A-HOST interface for HOST commands. Transition to any other mode must always be done through the Idle mode.

Record

When the HOST sends a record command, after detecting voice activity, the D7002A performs speech compression and stores the message in the ARAM or SRAM. While in this mode, the D7002A monitors the communication port every 28ms for HOST commands. If no new command is detected, the D7002A continues message recording. If an additional Record command is detected, the D7002A returns the VOX status (bit 6), memory status (bit 5), DTMF tone presence (bits 0-3) and call progress tone presence (bit 4) to the HOST. If an Idle command is detected, the D7002A stops recording, updates the message directory and returns to Idle mode. The D7002A reports to the HOST by sending the Idle mode status word. The D7002A assigns the next available message number. The first message will be assigned the number "0," the second message will be assigned the number "1," and so on, up to "63."

Record mode can be terminated by sending a Record command with 'Tail Cut' information. The D7002A stops recording and automatically deletes the last n*0.9 seconds from memory (Tail Cut function). The D7002A then returns to Idle mode.

If the ARAM has become full, the Memory Full bit (bit 5) in the status word is set. The D7002A stops recording, remains in Record mode and continues to perform line monitoring and VOX functions.

A single message can be stored in the SRAM by seting bit 10 in the first RECORD command. The SRAM message storage is not supported in 8K x 8 SRAM configuration. No message number or Day/Time stamp information is allocated to the SRAM message. SRAM message deletion is not supported; a new SRAM message is recorded over the old one.

Playback

In Playback mode, the D7002A performs message playback and line monitoring. Different variations of the Playback command are used during this mode to perform all necessary functions.

The first Playback command is used by the HOST to instruct the D7002A whether to play the message from the SRAM or from the ARAM, which message to play and at what speed (x1, x1.3 or x0.7). If the SRAM bit (bit 10) is "1," the SRAM message will be played and the ARAM message number will be ignored. If bit 10 is "0," the ARAM message that is indicated will be played. The Play Code (bits 8-9) indicates the playback speed. If the Play Code is "00" then the message will be played at normal speed. If it is "01" it will be played 1.3 times faster than recorded. If the Play Code is "10", the message will be played at 0 .7 times the original speed.

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The second Playback command instructs the D7002A at which point in the message to begin playback. This Offset information is measured in units of 1.35 seconds and can indicate a maximum offset of 15 minutes from the begining of the message. If the Offset is "0", the message is played from the begining. Message playback starts immediately after receiving the second Playback command.

After starting playback, the D7002A monitors the HOST command register every 28 ms. The HOST issues additional Playback commands during playback in order to perform line monitoring, change the playback speed, pause playback or read the current offset location. If the Pause bit (bit 11) and Read Offset bit (bit 10) are "0," the D7002A will continue playback at the indicated speed (Play Code) and will return a line status in the status word. If Pause is set, playback will stop until the Pause bit returns to "0." If the Read Offset is set high, the D7002A will return the offset of the current message, i.e., the time elapsed from the beginning of the message, instead of the line status.

The line status word sent in reponse to the Playback command contains information about the tones detected from the line, and and End of Play flag (bit 5), which indicates whether the end of the current message has been reached. When this bit is low, the message is still being played; when it is high, playback has stopped. If a message number does not exist, or if the Offset information is longer than the message length, the D7002A will return a status word with End of Play "1" following the third playback command. The line status information during playback contains the DTMF tone, if detected (bits 0-3), a call progress tone within the predefined bandwidth (in SELF TEST & INIT command) in bit 4 and FAX calling tone (CNG) in bit 6. The host will monitor these tones every 28 ms and will act accordingly. PLAYBACK will be terminated by Idle command and the D6275 will return to Idle mode.

Read Memory Status

In this mode the D7002A returns to the HOST a status word containing the following information:

- — Number of recorded messages
- — Memory Full indication
- — SRAM check status
- — Internal ROM checksum status
- — Existance of SRAM message
- — External ROM checksum status

When 64 messages were recorded OR when there is no available memory space for recording further messages, Memory Full flag (bit 6) is set. Up to 63 messages are reported in the 6 LSB of the status word. When 64 messages were recorded, eight LSB bits of status word are '1'.

SRAM status bit indicates whether an internal memory check was successful. The SRAM check status is used to select between 'cold start' or 'warm start' for power up procedure after RESET. For detailed description see INITIAL PROCEDURE.

After sending the status, the D7002A returns automatically to Idle mode.

Write Telephone Number

In this mode the D7002A receives from the HOST a word containing 4 telephone digits and writes it in the telephone directory under the entry number specified in the command word (the first word). This stored information can be actually used for any other host needs. The D7002A automatically returns to the Idle mode after this command.

Read Telephone Number

In this mode the D7002A returns to the HOST a word containing 4 telephone digits from the telephone directory, or any other information previously stored by the host, using the entry specified in the first command word. The D7002A automatically returns to the Idle mode after this command.

Tone Generation mode

In this mode the D7002A generates a selected DTMF signal or one out of other 15 general purpose tones. The index for the signal/tone to be generated and the required level is sent by the HOST in the command word.

The indices are as follows:

GEN CODE	DTMF CODE	FREQ 1	FREQ 2
0	No Tone		
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	*	941	1209
B	0	941	1336
C	#	941	1477
D		800	
E		1000	
F		1250	
10		950	
11		1100	
12		1400	
13		1500	
14		1600	
15		1800	
16		2100	
17		1300	
18		2450	
19		350	440

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1A		440	480
1B		480	620
1C	A	697	1633
1D	B	770	1633
1E	C	852	1633
1F	D	941	1633

The D7002A checks the host port every 28ms for a new HOST command. Whenever a new tone generation command is sent, the D7002A retrieves the tone index and the level from the command word and starts/continues generating the tone. The length of each tone can be in units of 28 ms. The Tone Level codes are as follows:

TONE LEVEL CODE (HEX)	GAIN
0	0 dB
1	+2 dB
2	+4 dB
3	+6 dB
4	+8 dB
5	+10 dB
6	+12 dB
7	+14 dB
8	0 dB
9	-2 dB
A	-4 dB
B	-6 dB
C	-8 dB
D	-10 dB
E	-12 dB
F	-14 dB

If no new command is sent, the D7002A continues generating the previously generated tone. An Idle command will terminate the tone generation and the D7002A will return to Idle mode.

Line Monitoring mode

In this mode the D7002A monitors the telephone line for the detection of a DTMF signal, FAX calling tone (CNG) or existance of Call Progress tone within the frequency band that was predefined in the SELF TEST & INIT command. The wide filter will detect tones within 330-650 Hz and the narrow filter will detect tones within 330-500 Hz. While in this mode, the D7002A is monitoring the communication port every 28 msec for HOST command. If no new command is detected, the D7002A continues monitoring the line.

The D7002A returns a status word to the HOST containing the CNG tone flag (bit 5), the call progress tone flag (bit 4) and the index of the DTMF signal that has been detected:

INDEX	DTMF CODE
0	No Tone
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
A	*
B	0
C	#

The D7002A will stop monitoring the line and return to Idle mode when an Idle command will be sent.

Delete Message

In this mode the D7002A performs one of the two following functions:

1. If the message number is from 0 to 63, the D7002A removes the message entry from the message directory, shifts all higher message entries one place down in the directory and lower the total number of messages by one. SRAM message deletion is not supported. Deletion of a message will not free up memory space until a Garbage Collection command will be performed. However, if all messages in the ARAM have been deleted, no Garbage Collection is required and all the ARAM space is available for message recording.
2. If the message number is 7FH, the D7002A performs Garbage Collection to get rid of empty spaces in the message memory. When the D7002A completes performing this process, it sends a status word to the HOST.

Note: The D7002A response time to the Garbage Collection command depends on the length of the messages to be relocated in the memory. For each one minute of recording time the process will take 1.3 seconds (approx.). If, for any special need, the host will interrupt the D7002A before Garbage Collection is completed (by issuing an Idle command), the D7002A will keep transferring the current message until its end and will respond with Idle status word. The host should initiate another Garbage Collection later in order to complete the operation and free up the ARAM memory space.

Set Current Time

In this mode the HOST sends to the D7002A the current time & date mark that will be used for time stamping of the next message to be recorded. This time stamp is attached to the message and can be retrieved by Get Time Stamp command. The D7002A automatically returns to the Idle mode after this command.

Get Time Stamp

In this mode the D7002A sends to the HOST the time & date stamp of the message specified in the command word. No time stamp is supported for the SRAM message. The D7002A automatically returns to the Idle mode after this command.

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Get Available Record Time

In this mode, the D7002A sends to the HOST the available ARAM record time in 1.35s units. The D7002A automatically returns to the Idle mode after this command.

Self Test & Initialize Memory

In this mode the D6275 performs memory testing and initialization of hardware & software parameters. There are 3 sub modes in this mode:

1) Normal test mode :

This sub mode used in normal operation of the chip set. After first power up of the system, the host must send this command to the D7002A in order to initialize & map the system memories. The D6275 performs ARAM & SRAM mapping in order to determined the ARAM & SRAM size (can be up to 16M bits ARAM & 8K-64K bytes SRAM). The D7002A reports on the total number of good 1Mbit units in the system and the location of the first bad 1Mbit unit. The SRAM status is reported as pass/fail (bit 3) - this bit is set '1' when the size of the good SRAM found is less then the SRAM SIZE indicated in the host command .

At the end of the memory initialization process, the D7002A writes known patterns to some predefined locations in the SRAM. These patterns will be used for later SRAM status test.

This sub mode is also used for setup of the system's hardware configuration and the selection of the call progress tone filter bandwidth. When CODEC MODE bit is '0' - the hardware setup is for a fixed data rate CODEC, when '1'- will set it for variable data rate CODEC. When REFRESH MODE bit is '0'- the hardware setup to RAS only refresh mode during power down, when '1'- will set the hardware to CAS before RAS refresh mode during power down. When CPTF bit is '0'- Narrow band (330-500 Hz) filter is selected, when '1' wide band (330-650Hz) filter is selected for call progress tone detection. INI bit give to the host ability to change hardware setup & filter selection without the memory initialization - this done by setting INI bit to '1'.

If the memories were not initialized after first power-up, the D7002A assumes that the system has 16 Mbit ARAM, 8 Kbyte SRAM, fixed rate CODEC, refresh with RAS only in power down, and narrow band filter for call progress tones.

2)Short ARAM Test:

This sub mode can be useful for production line testing - It gives fast indication on existence of ARAMs in the system.

3)SRAM & Voice Prompt EPROM Test:

This sub mode can be useful for production line testing - It performs Voice Prompts EPROM pass/fail test and reports the size of the SRAM in the system . The D7002A automatically returns to the Idle mode after this command.

Voice Prompt Generation

In this mode the D7002A playback a speech segment, that was previously stored in an external ROM/EPROM, using the speech decompression algorithm. The host is indicating the D7002A the phrase number to play (0-127) in bits 0-6 in the command word. The D7002A will load the phrase, start play it and send status word to the host containing line status and playback status. The line status part will contain information about DTMF, call progress tones and CNG tone in the same way as for LINE MONITOR command. The second part of the status word contains two flags: END OF PLAY and READY. The host can continiously monitor the status by issuing VOICE PROMPT command (every 28 ms) and act according to the returned flags.

READY - this bit (9) is set to "1" by the D7002A two frames (frame = 28 ms) before the end of the phrase playback. It indicates that the D7002A is ready to load a new phrase. If the HOST will send LOAD command immediately after reading this status, there will be no silence gap between the two phrases. The host can delay the LOAD command for few frames and create gap between two phrases in units of 28 ms. The host will load the new phrase by seting LOAD bit (bit 11) to '1' in the next command and indicating the new phrase number in bits 0-6. Sending LOAD command while ready bit is '0' will not load the new phrase.

END OF PLAY - This bit (10) is set one frame after the READY bit and it indicates that the D7002A have finished playback of the phrase. The D7002A will transmit silence to the codec but will stay in VOICE PROMPT mode.

The VOICE PROMPT mode is terminated by sending Idle command.

Notes:

1) The D7002A ignores the LOAD bit in the first VOICE PROMPT command, and loads anyway.
2) If the phrase number is higher than the last phrase recorded in the ROM/EPROM, the status word will return END OF PLAY and READY bits high and no playback will be performed.
3) The amount of recording time for voice prompts depends on the ROM/EPROM size and it is 9.5 seconds for each 8Kbytes of memory space.

Speakerphone

In this mode the D7002A implements a host controllable Digital SpeakerPhone algorithm. When activated, this algorithm enables enhanced speakerphone operation with programmable parameters.

The speakerphone command is comprised of two commands. The first command defines the speakerphone parameters. The second command is needed only for generating DTMF tones while in speakerphone mode.

Default Priority Control. This parameter controls the algorithm's default priority setup. If D bit (bit 11) is set to '1', the line side (far) will have priority over the microphone side (near) and whenever

both sides are quiet, the far side will control the line and the microphone will be attenuated. If D bit is '0', the control of the conversation will alternate between the two sides and will stay at the latest side in the case of quiet from both sides.

Echo Suppression Loop Gain. This parameter defines the suppression loop gain. The parameter affects the trade-off between the natural likeness of the conversation and the echo immunity robustness.

The user can choose a suppression level ranging from 12 dB to 40 dB with 4 dB resolution:

ECHO SUPPRESSION GAIN	SUPPRESSION LEVEL
0	12 dB
1	16 dB
2	20 dB
3	24 dB
4	28 dB
5	32 dB
6	36 dB
7	40 dB

MIC and LINE Voxes Input Gain. These two parameters affect the echo suppressor switching behavior. The bigger the input gain, the easier it is for the speaker at the appropriate side to dominate the conversation.

The host can independently choose the input levels to the MIC and LINE voxes, ranging from -8 dB to +7 dB with 2 dB resolution.

MIC/LINE Gain	MIC\LINE Vox/Input Level Ratios
0	+7 dB
1	+4 dB
2	+2 dB
3	0 dB
4	-2 dB
5	-4 dB
6	-6 dB
7	-8 dB

Vox Decay. This parameter affects the echo suppressor switching time. Too fast a switching time can cause a switching resonance effect, especially if the speaker volume is high.

Set-up Optimization. The parameterized speakerphone function allows the user to optimize the function behavior to suit his needs. The recommended parameter tuning procedure is as follows:

1. Choose the echo suppression loop GAIN that eliminates the echo effect. Remember, that the lower the gain, the better the conversation will sound.
2. Start with both MIC and LINE vox input gains set to 0 dB. Adjust the vox input gains to get the most satisfying switching behavior. If one side fails to switch-in properly, increase its vox input gain.
3. Use the VOX Decay parameter to further optimize the switching behavior achieved in the previous steps.

Speech Data Retrieval (ARAM to HOST)

In this mode the D7002A retrieves speech data, previously compressed and stored in the message buffer (ARAM), and transfers it through the HOST communication interface.

The first command of this mode specifies in bits 0-6 the number of the message to be retrieved. Status of this command contains END of MESSAGE bit (bit 8). If the specified message doesn't exist, the DSP returns the status with END of MESSAGE bit set to "1" and the D7002A goes to IDLE mode. If the specified message exists the D7002A returns status word with echo of the message number in bits 0-6 and the bit 8 cleared to"0".

The second and subsequent commands instruct D7002A to transfer the compressed speech data one byte at a time. The low byte of the status of this command contains byte of compressed speech data. The status also contains END of MESSAGE bit (bit 8) which points the last byte of the message. If this bit is set "1", the current byte is the last byte of the message. After the end of the message D7002A stops retrieving data and goes to Idle mode. The message transferred to the HOST remains in the ARAM.

The maximum data transfer rate is 33Kbyte of compressed speech per second.

The message length is always multiples of 128 bytes.

Speech Data Storage (HOST to ARAM)

In this mode the D7002A transfers compressed speech data through the HOST communication interface and stores this data in the message buffer (ARAM) one byte at a time.

The low byte of the Data Storage command contains the byte of compressed speech data to be stored. The D7002A echoes the data in the low byte of the status word. If an Idle command is detected, the D7002A assigns the next available message number to newly stored data, updates the message directory, and goes to Idle mode.

The maximum data transfer rate is 115Kbyte of compressed speech per second.

If ARAM has become full in Data Storage mode the D7002A sets the Memory Full bit (bit 8) "1", stops storing data, and stays in the Data Storage mode. The HOST should send Idle command and the D7002A will assign the next available message number to newly stored data, update the message directory, and go to Idle mode.

The D7002A stores data in full segments of 128 bytes. If the last segment of the message is not full, this segment will be lost.

HOST INTERFACE PERFORMANCE

The D7002A maximum response times of the D7002A to host commands are as follows:

COMMAND	MAX STAT US RESPONSE TIME
Idle	28 msec
Record	28 msec
First Playback	1 msec
Second Playback (offset)	1 msec
Next Playback (Continue)	28 msec
Line Monitor	28 msec
Delete Message without Garbage Collection	1 msec
Delete Message with Garbage Collection	30 sec*
Set Current Time	1 msec
Get Time	1 msec
Get Available Record Time	1 msec
Read ARAM Status	1 msec
Write Telephone Number	1 msec
Read Telephone Number	1 msec
DTMF Generation	28 msec
First Speakerphone	1 msec
Second Speakerphone	28 msec
Voice Prompt Generator	28 msec
Self Test	58 sec*
Speech Data Retrieve	1 msec
Speech Data Storage	4 msec

* execution time for D7002A system with 8 Mbit ARAM.

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Power Down Operation

The D7002A needs two sources of power:

VCC– Battery backed 5VDC supply, connected continuously to the D7002A-11, SRAM, ARAM and EPROM.

VCC1– 5VDC that supplies power only during power on, connected to the D7002A-11 and the CODECs.

Power fail indication signal is supplied to the D7002A through $\overline{PDN}$ pin (pin 61). A RESET input signal is also connected to the D7002A (pin 35). In power up sequence, the $\overline{PDN}$ signal should go high as soon as VCC1 is supplied and $\overline{RESET}$ should go high after VCC1 is valid but not before $\overline{PDN}$ is high.

For dual oscillator configuration the $\overline{RESET}$ should go high with a minimum delay of 10 msec after VCC1 is valid.

When power failure happens, the $\overline{PDN}$ signal goes low and the D7002A will perform several operations before entering Power Down mode. While in power down mode the D7002A is not operating and will not respond to external signals. A RESET signal should go low at least 2 mseconds after $\overline{PDN}$ is low.

The refresh mode during power down can be selected by software parameter during SELF TEST & INIT command and it can be one of the following:

— 0 - RAS Only refresh mode
— 1 - CAS before RAS refresh mode.

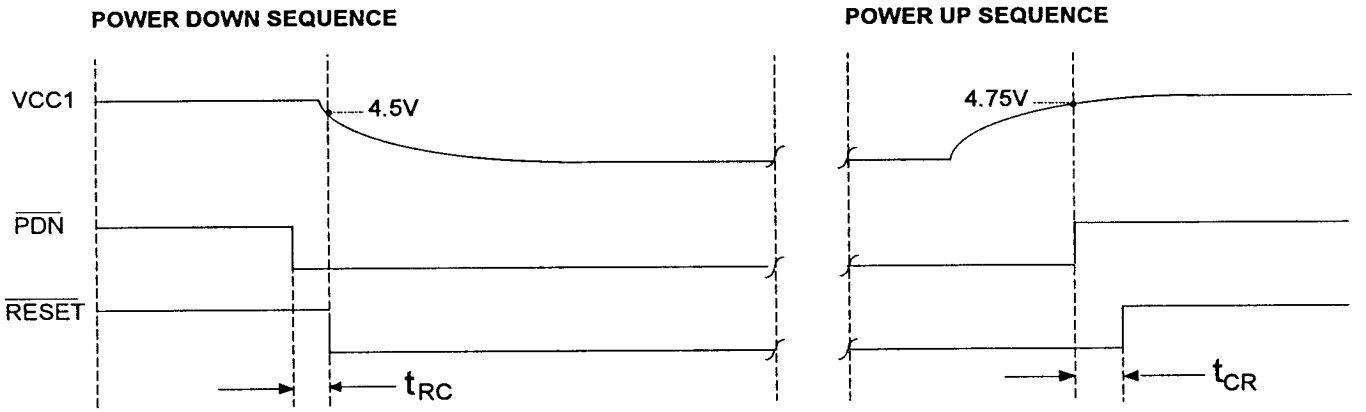

Figure 5. Timing data for the Power Down/Up Sequence

$t_{RC} > 2msec$
$t_{CR} > 0$

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D7002A COMMAND SET

0. IDLE

Command:

0000	000000000000
(15 - 12)	(11 - 0)

Status:

0000	000000000000
(15 - 12)	(11 - 0)

1. RECORD

Command:

0001	0	SRAM	0000000000
(15 - 12)	(11)	(10)	(9 - 0)

SRAM: 0 - Record in ARAM area
1 - Record in SRAM area

Status:

0001	0	SRAM	000	VOX	MEMORY FULL	TONE	DTMF CODE
(15 - 12)	(11)	(10)	(9 - 7)	(6)	(5)	(4)	(3 - 0)

Command (Last):

0001	1	0	0000	TAIL CUT FACTOR
(15 - 12)	(11)	(10)	(9 - 6)	(5 - 0)

Status:

0001	1	0	0000	TAIL CUT FACTOR
(15 - 12)	(11)	(10)	(9 - 6)	(5 - 0)

TAIL CUT FACTOR: Message tail is cut in units of 0.9 seconds
When 000000, message tail is not cut

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2. PLAYBACK

Command (First):

0010	0	SRAM	PLAY CODE	0	ARAM MESSAGE NUMBER
(15 - 12)	(11)	(10)	(9 - 8)	(7)	(6 - 0)

SRAM = 0: Play from ARAM
1: Play from SRAM

PLAY CODE:
00 - Normal
01 - Fast FLEXI rate (1.3)
10 - Slow FLEXI rate (0.7)
11 - Reserved

Note: D6275A supports up to 64 messages (bit 6 must be 0)

Status:

0010	0	SRAM	PLAY CODE	0	ARAM MESSAGE NUMBER
(15 - 12)	(11)	(10)	(9 - 8)	(7)	(6 - 0)

Command (Second):

0010	00	OFFSET
(15 - 12)	(11 - 10)	(9 - 0)

OFFSET: Offset is measured from the beginning of the message, in units of 1.35 seconds. The maximum offset supported is 10,1010,1010 (approximately 920 seconds, or 15 minutes).

Status:

0010	00	OFFSET
(15 - 12)	(11 - 10)	(9 - 0)

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Command (Third, and on, used for monitoring the input and END of message):

0010	PAUSE	READ OFFSET	PLAY CODE	00000000
(15 - 12)	(11)	(10)	(9 - 8)	(7 - 0)

PAUSE: 1 - Stop Playback (Pause)
0 - Continue Playback

PLAY CODE: Changes Playback speed

00 - Normal
01 - Fast FLEXI
10 - Slow FLEXI
11 - Reserved

If READ OFFSET bit = 1, then the current offset is reported, as measured from the beginning of the message, in units of 1.35 seconds. The maximal value is 1010101010.

Status:

0010	PAUSE	1	OFFSET
(15 - 12)	(11)	(10)	(9 - 0)

If READ OFFSET bit - 0, then:

Status:

0010	PAUSE	0	PLAY CODE	0	CNG	END OF PLAY	TONE	DTMF
(15 - 12)	(11)	(10)	(9 - 8)	(7)	(6)	(5)	(4)	(3 - 0)

DTMF: Code of DTMF signal detected

TONE: 1 - Call Progress Tone detected

END OF PLAY: 1 - End of message reached

CNG: 1 - CNG tone detect

PLAY CODE: Same as in the command

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3. READ MEMORY STATUS

Command:

0011	*0000000000*
(15 - 12)	*(11 - 0)*

Status:

0011	EPROM CHECKSUM STATUS	SRAM MSG	ROM CHECKSUM STATUS	SRAM STATUS	PAGE	MEMORY FULL	# OF ARAM MSGES
(15 - 12)	(11)	(10)	(9)	(8)	(7)	(6)	(5 - 0)

MEMORY FULL:	1 - Message memory full, or directory full (64)
PAGE:	0 - For number of messages below 64 1 - For 64 messages
SRAM STATUS:	0 - SRAM StatusTest OK
EPROM CHECKSUM STATUS:	0 -Synthesizer EPROM ChecksumTest OK
ROM CHECKSUM STATUS:	0 - ROM Checksum Test OK
SRAM MESSAGE:	1 - Message is stored in SRAM area

NOTE: If 64 messages are recorded, all 8 LSB status words will be set to '1'.

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4. WRITE TELEPHONE NUMBER

Command (First):

0100	00000	DIRECTORY INDEX	WORD INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

DIRECTORY INDEX: Telephone number index
WORD INDEX: 4 digit group index

Status:

0100	00000	DIRECTORY INDEX	WORD INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

Command (Second):

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

Status:

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

5. READ TELEPHONE NUMBER

Command:

0101	00000	DIRECTORY INDEX	WORD INDEX
(15 - 12)	(11 - 7)	(6 - 2)	(1 - 0)

Status:

DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4
(15 - 12)	(11 - 8)	(7 - 4)	(3 - 0)

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6. TONE GENERATOR

Command:

0110	000	TONE LEVEL	TONE CODE
(15 - 12)	(11 - 9)	(8 - 5)	(4 - 0)

TONE CODE: 0 - No tone
1 - 31 - Tone code

TONE LEVEL: 0000, 1000 Normal (0 dB = -12 dBm per tone)
0001 - 0111 Gain level (+2 dB steps)
1001 - 1111 Attenuation level (-2 dB steps)

Notes: 1) DTMF levels are -13 dBm for DTMFLO and -11dBm for DTMFHI (Twist)
2) +14dB gain is not supported for dual tones

Status:

0110	000	TONE LEVEL	TONE CODE
(15 - 12)	(11 - 9)	(8 - 5)	(4 - 0)

7. LINE MONITOR

Command:

0111	000000000000
(15 - 12)	(11 - 0)

Status:

0111	000000	CNG	TONE	DTMF
(15 - 12)	(11 - 6)	(5)	(4)	(3 - 0)

DTMF: Code of DTMF signal detected
TONE: 1 - Call progress tone detected
CNG: 1- CNG tone detected

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8. DELETE MESSAGE

Command:

1000	00000	MESSAGE NUMBER
(15 - 12)	(11 - 7)	(6 - 0)

MESSAGE NUMBER = 0 - 63: Delete message
64 - 126: Reserved
127: Garbage collection

Status:

1000	000	STATUS	MESSAGE NUMBER
(15 - 12)	(11 - 9)	(8 - 7)	(6 - 0)

STATUS: = 00: OK
01: Attempt to delete an empty message
10: Garbage collection performed
11: Reserved

Note: No need for Garbage collection after deleting all messages in directory.

9. SET CURRENT TIME

Command (First):

1001	000000000000
(15 - 12)	(11 - 0)

Status:

1001	000000000000
(15 - 12)	(11 - 0)

Command (Second):

TIME STAMP
(15 - 0)

Status:

TIME STAMP
(15 - 0)

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10. GET TIME STAMP

Command:

1010	00000	MESSAGE NUMBER
(15 - 12)	(11 - 7)	(6 - 0)

Status:

TIME STAMP
(15 - 0)

11. GET AVAILABLE RECORD TIME

Command:

1011	000000000000
(15 - 12)	(11 - 0)

Status:

1011	0	AVAILABLE TIME
(15 - 12)	(11)	(10 - 0)

AVAILABLE TIME: Available time in units of 1.35 seconds.

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12. SELF TEST AND INITIALIZATION

If TEST MODE (bits 9-11) = 000 (Normal test mode)

Command:

1100	0 0 0	00	REFRESH MODE	SRAM SIZE	INI	CODEC MODE	CPTF
(15 - 12)	(11 - 9)	(8 - 7)	(6)	(5 - 3)	(2)	(1)	(0)

CPTF: 0 - Select narrow band filter for Call Progress Tone Detector (330 - 500)
1 - Select wide band filter for call Progress Tone Detector (330 - 650)

CODEC MODE: 0 - Select fixed mode codec interface (D0000-29)
1 - Select variable mode codec interface

INI: 0 - Test and initialize memory
1 - Do not test and initialize memory (SRAM, ARAM)

SRAM SIZE: 000 - Report failure in lower 8 Kbyte space
001 - Report failure in lower 16 Kbyte space
010 - Report failure in lower 24 Kbyte space
011 - Report failure in lower 32 Kbyte space
100 - Report failure in lower 40 Kbyte space
101 - Report failure in lower 48 Kbyte space
110 - Report failure in lower 56 Kbyte space
111 - Report failure in lower 64 Kbyte space

REFRESH MODE: 0 - RAS only refresh in Power Down Mode
1 - CAS before RAS refresh in Power Down Mode

TEST MODE: 000 - Normal test and initalization MODE (Should be run first time after first power on or for change wide of Call Progress Detector filters)
001 - Short ARAM test (Existance of ARAM)
010 - Short SRAM and EPROM test

Status:

1100	INDEX OF FIRST BAD ARAM	NUMBER OF GOOD ARAMS	SRAM STATUS	INI	CODEC MOD	CPTF
(15 - 12)	(11 - 8)	(7 - 4)	(3)	(2)	(1)	(0)

INDEX OF FIRST BAD ARAM: Index of first bad 1 Mbit ARAM found in the test.

NUMBER OF GOOD ARAMS: Number of good 1 Mbit ARAMS found in the test. When 16 Mbit were found good, the value is 0000 and INDEX of FIRST BAD ARAM is 0001.

SRAM STATUS: Result depends on SRAM size bits:
0 - Good SRAM
1 - SRAM failure test

INI, CODEC MODE & CPTF: Same as in the command

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If TEST MODE (bits 9-11) = 001 (Short ARAM Test):

Command:

1100	*001*	*000000000*
(15 - 12)	*(11 - 9)*	*(8 - 0)*

Status:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

AX: 0 - No ARAM in location X exist
1- ARAM in location X exist

X - in unit of 1 Mbit

If TEST MODE (bits 9-11) = 010 (SRAM & Voice Prompt EPROM/ROM Test)

Command:

1100	*010*	*000000000*
(15 - 12)	*(11 - 9)*	*(8 - 0)*

Status:

1100	010	EPROM CHECKSUM TEST	0000	SRAM SIZE
(15 - 12)	(11 - 9)	(8)	(7 - 4)	(3 - 0)

SRAM SIZE - Amount of good SRAM in units of 8K bytes

EPROM CHECKSUM TEST 0 - Checksum is OK
1 - Checksum failed

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13. VOICE PROMPT GENERATION

Command:

1101	*LOAD*	*0 0 0 0*	*PHRASE NUMBER*
(15 - 12)	*(11)*	*(10 - 7)*	*(6 - 0)*

LOAD: 1 - Load new phrase number for playback
0 - Monitor Status

Status:

1101	LOAD	END OF PLAY	READY	0 0 0	CNG	TONE	DTMF
(15 - 12)	(11)	(10)	(9)	(8 - 6)	(5)	(4)	(3 - 0)

DTMF: Code of DTMF signal detected

TONE: 1 - Call Progress Tone detected

CNG: CNG tone detect

READY: 1 - Ready for loading a new phrase for Playback

END OF PLAY: End of phrase reached

LOAD: 1 - Load phrase command was accepted

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14. SPEAKERPHONE

Command (First):

1110	D	ATTENUATION LEVEL	MIC. VOX GAIN	LINE VOX GAIN	SWITCH SPEED
(15 - 12)	(11)	(10 - 8)	(7 - 5)	(4 - 2)	(1 - 0)

ATTENTUATION LEVEL: Echo suppression loop gain =
000 - 12 dB
001 - 16 dB
010 - 20 dB
011 - 24 dB
100 - 28 dB
101 - 32 dB
110 - 36 dB
111 - 40 dB

SWITCH SPEED:
00 - slow
01 -
10 -
11 - fast

D (Default control):
1 - Line side priority
0 - No priority

MIC VOX GAIN, LINE VOX GAIN:
000 - +7 dB
001 - +4 dB
010 - +2 dB
011 - +0 dB
100 - -2 dB
101 - -4 dB
110 - -6 dB
111 - -8 dB

Status:

1110	D	ATTENUATION LEVEL	MIC. VOX SENSITIVITY	LINE VOX SENSITIVITY	SWITCH SPEED
(15 - 12)	(11)	(10 - 8)	(7 - 5)	(4 - 2)	(1 - 0)

Command (Second):

1110	0 0 0	TONE LEVEL	TONE CODE
(15 - 12)	(11 - 9)	(8 - 5)	(4 - 0)

TONE LEVEL:
0000, 1000 Normal (0 dB = -12 dBm per tone)
0001 - 0111 Gain level (+2 dB steps)
1001 - 1111 Attenuation level (-2 dB steps)

TONE CODE:
0 - No tone
1 - 31 - Tone code

Status (Second):

1110	0 0 0	TONE LEVEL	TONE CODE
(15 - 12)	(11 - 9)	(8 - 5)	(4 - 0)

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15. SPEECH DATA STORAGE/RETRIEVAL DATA STORAGE (HOST TO ARAM)

Command:

1111	0	000	DATA
(15 - 12)	(11)	(10 - 8)	(7 - 0)

Status:

1111	0	00	MEMORY FULL	DATA
(15 - 12)	(11)	(10 - 9)	(8)	(7 - 0)

SPEECH DATA RETRIEVAL (ARAM TO HOST)

Command (First):

1111	1	00	MESSAGE NUMBER
(15 - 12)	(11)	(10 - 7)	(6 - 0)

Status (First):

1111	1	00	END OF MESSAGE	0	MESSAGE NUMBER
(15 - 12)	(11)	(10 - 9)	(8)	(7)	(6 - 0)

If a message does not exist, END OF MESSAGE = 1 and MESSAGE NUMBER = 0000000. The DSP will go to IDLE Mode.

If a message exists, END OF MESSAGE = 0 and MESSAGE NUMBER echos the MESSAGE NUMBER of the command. The DSP will wait for the second command.

Command (Second and on):

1111	1	000	00000000
(15 - 12)	(11)	(10 - 8)	(7 - 0)

Status (Second and on):

1111	1	00	END OF MESSAGE	DATA
(15 - 12)	(11)	(10 - 9)	(8)	(7 - 0)

END OF MESSAGE = 1: No more data available in the message.

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FUNCTIONAL BLOCKS

The block diagram in Figure 6 shows the D7002A functional blocks and interface.

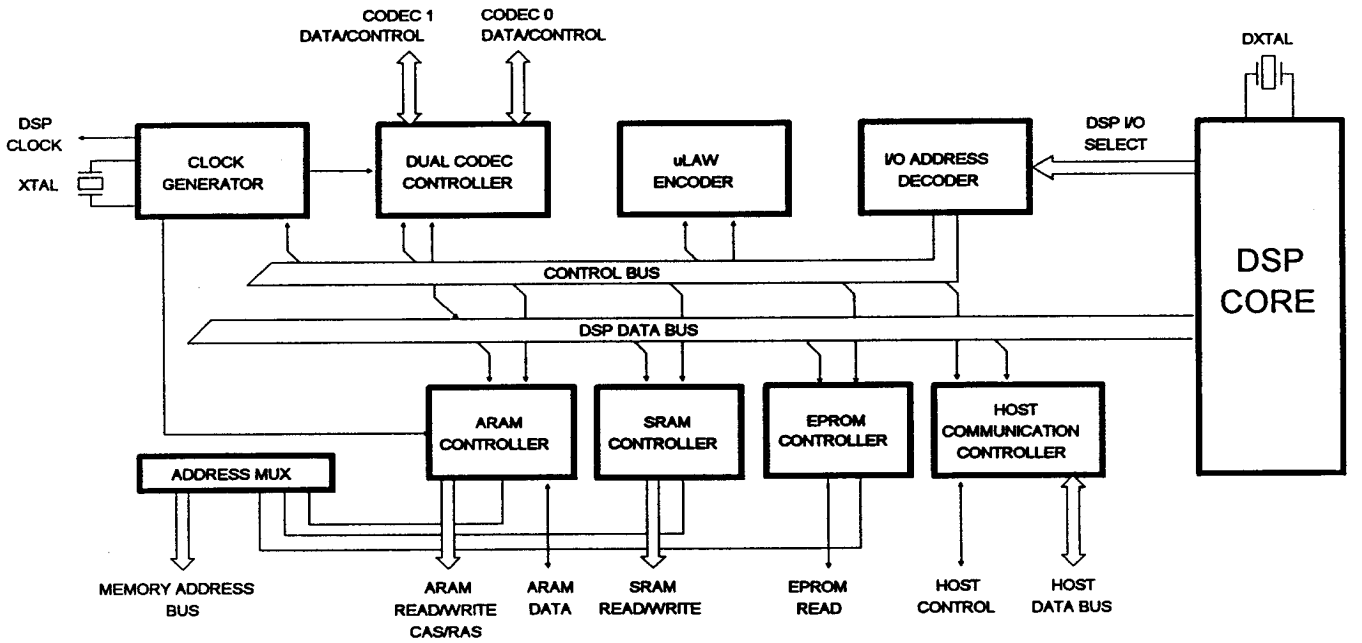

Figure 6. D7002A-11 Block Diagram

D0091

DSP CORE

At the heart of the chipset is the DSP Core. All of the software algorithms such as compression, decompression, tone detection, tone generation, and echo cancellation run on that processor. The DSP Core controls the system, memory and message management. The DSP program ROM is masked internally. The DSP is connected via an internal bus, to most of the other modules within the D7002A-11 COMBO chips. The DSP Core shuts down during power-down mode.

ADDRESS MUX

Address MUX controls external memory select signals and memory address bus.

ARAM INTERFACE

The ARAM interface offers up to 16 Mbits of ARAM storage for message storage. This interface can support up to four 4Mbit x 1 ARAMS without external logic.

This block consists of two parts:

1. ARAM read/write logic
2. Refresh logic

In power down mode the refresh logic will select as its clock source either the high DSP DXTAL signal or the optional low-frequency resonator, according to the SELREF pin (pin 10) status.

The 12 address lines shared with address lines of SRAM. When accessing SRAM, refresh is disabled and the address bus is switched to SRAM address via the Address MUX.

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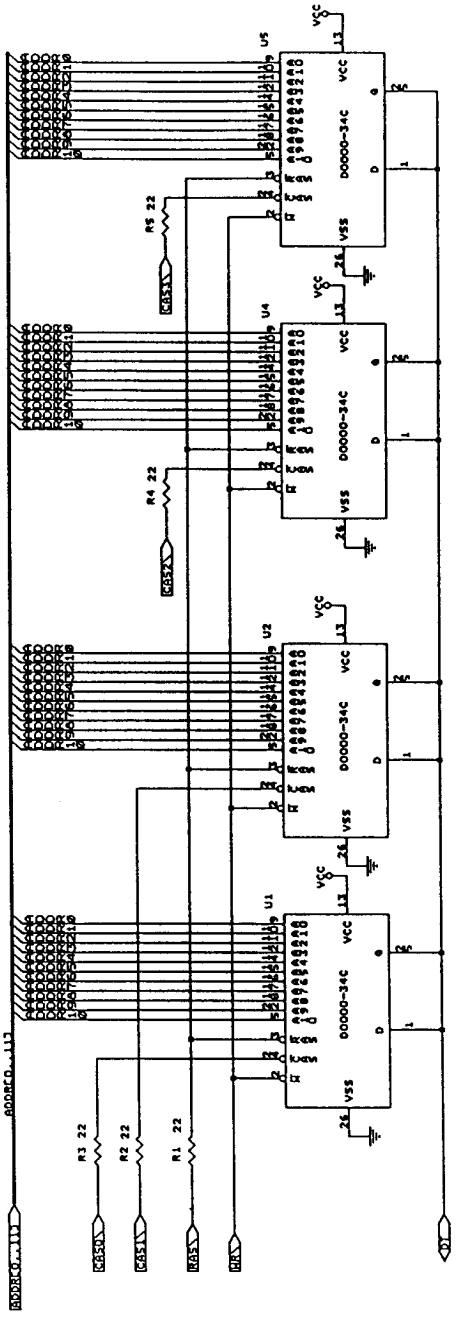

Figure 7. ARAM Block - 4 Meg Devices (D0000-34)

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SRAM INTERFACE

The D7002A reads/writes from/to the SRAM using the 8 bits data bus. Each 16 bit wide access is transformed by the D7002A into two consecutive 8 bit accesses. The D7002A sets the initial address, then consecutive reads/writes from/to the SRAM may be done using the address counter located in the internal logic. The maximum access rate to the SRAM is one word for each four CLKOUT periods.

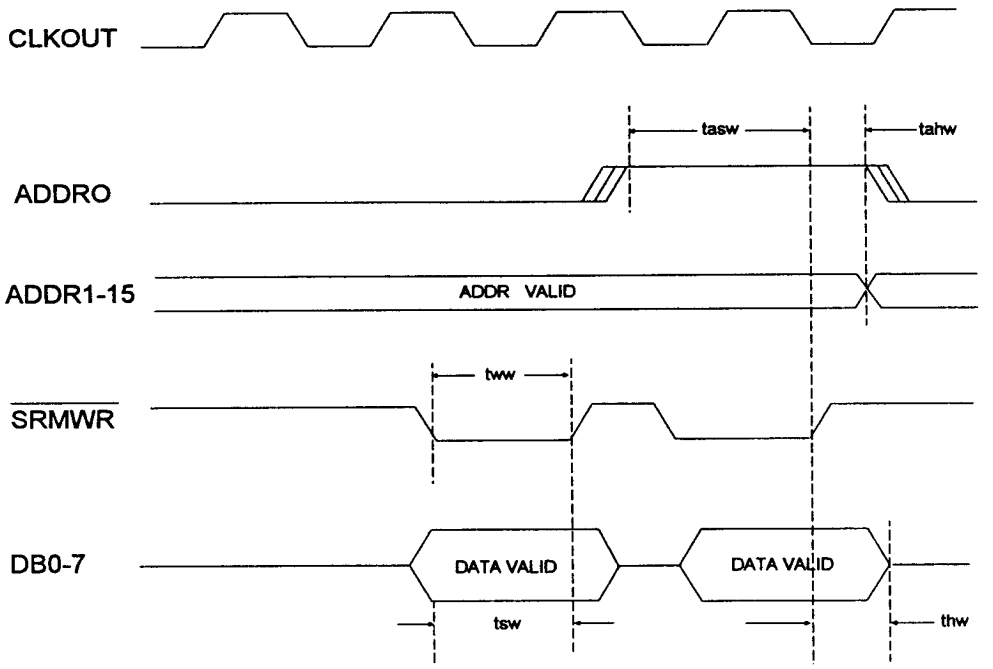

Figure 8. SRAM Write Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
tasw	Address valid setup time	120	168.4		ns
tahw	Address valid hold time	3			ns
tww	Write pulse width	90	114.3		ns
tsw	Data valid setup time	90			ns
thw	Data valid hold time	3			ns

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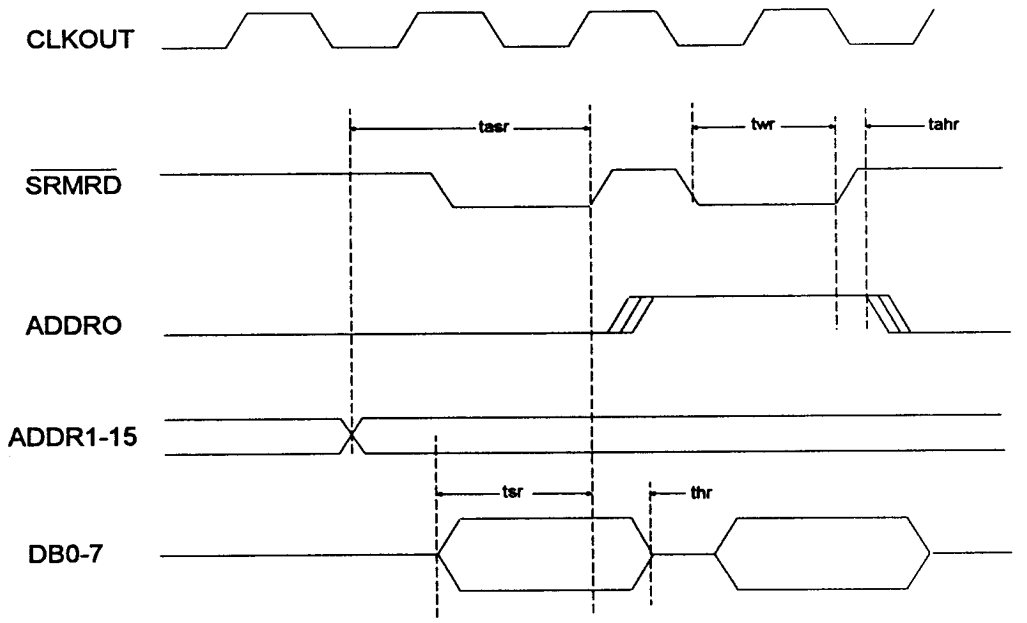

Figure 9. SRAM Read Timing

PARMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
tasr	Address setup time	125	168.4		ns
tahr	Address hold time	3			ns
tsr	Data setup time	10			ns
thr	Data hold time	0			ns
twr	Read pulse width		114.3		ns

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VOICE PROMPT EPROM INTERFACE

The D7002A will read from the EPROM using 8 bits of the memory-data bus (MDB[0-7]). Each 16 bit wide access is transformed by the D7002A into two consecutive 8 bit accesses. The D7002A sets the initial address, then consecutive reads from the EPROM may be done using the address counter located in the internal logic. The maximum access rate to the EPROM is one word for each 7 CLKOUT periods.

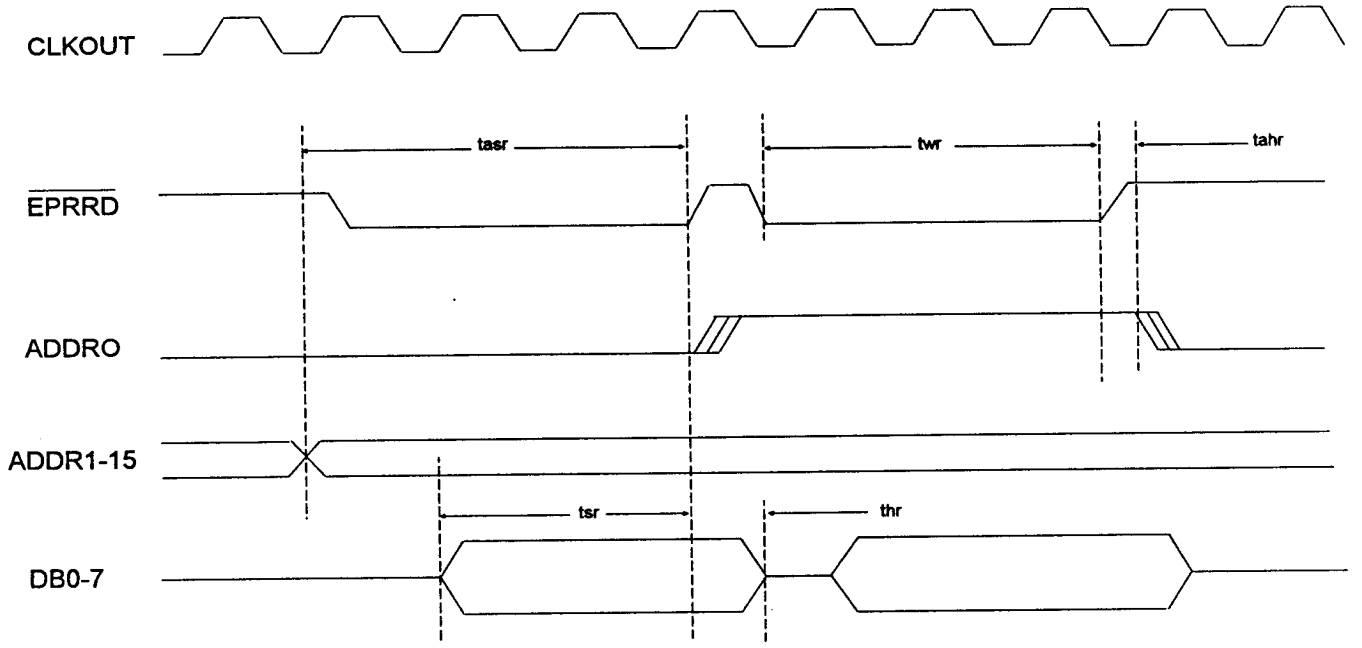

Figure 10. EPROM/ROM Read Timing

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
tasr	Address setup time	354.0	397.0		ns
tahr	Address hold time	3			ns
tsr	Data setup time	10			ns
thr	Data hold time	0			ns
twr	Read pulse width		342.9		ns

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µLAW ENCODER

This is an interface implemented in the D7002A-11 to convert linear code (14-bit) to 8-bit µlaw PCM code. It works by writing 14-bit linear data to this interface. Reading from this port will produce 8-bit PCM data.

ANALOG I/O CONTROLLER

The Analog I/O controller implements the data transfer and synchronization functions required to interface the DSP with the Analog I/O Interface (codec) chips. The data transfer to/from the codecs is serial, while shift registers enable an 8-bit parallel link with the DSP. The INT interrupt signal informs the DSP that a data byte has been received or has to be transmitted. The analog I/O controller can support fixed rate CODECs as well as variable rate CODECS. The bit 1 of the Self Test & Init command selects between the two types.

CLOCK GENERATOR

The D7002A can be connected to the CLOCK source in two different ways:

1. Single, high-frequency crystal oscillator for both operation and power down modes. A 34.992 MHz crystal is connected to XOUT and XIN (pins 21-21). The SELREF pin (pin 10) should be open and DSPCLK (pin 34) should be connected to XDIN (pin 53). See Figure 14.
2. Dual, high and low frequency crystal oscillators to support low power consumption during power down mode. A 34.992 MHz crystal is connected to XDIN and XDOUT (pins 53-54) and a 600 KHz resonator is connected to XOUT and XIN (pins 31-32). The SELREF pin (pin 10) should be connected to GND. See Figure 15.

The SELREF input signal selects between the two modes. The second configuration, with two separate clock sources significantly improves the power consumption during power-down mode.

I/O ADDRESS DECODER

The I/O Address Decoder generates the required I/O read and write pulses for the internal DSP peripheral devices.

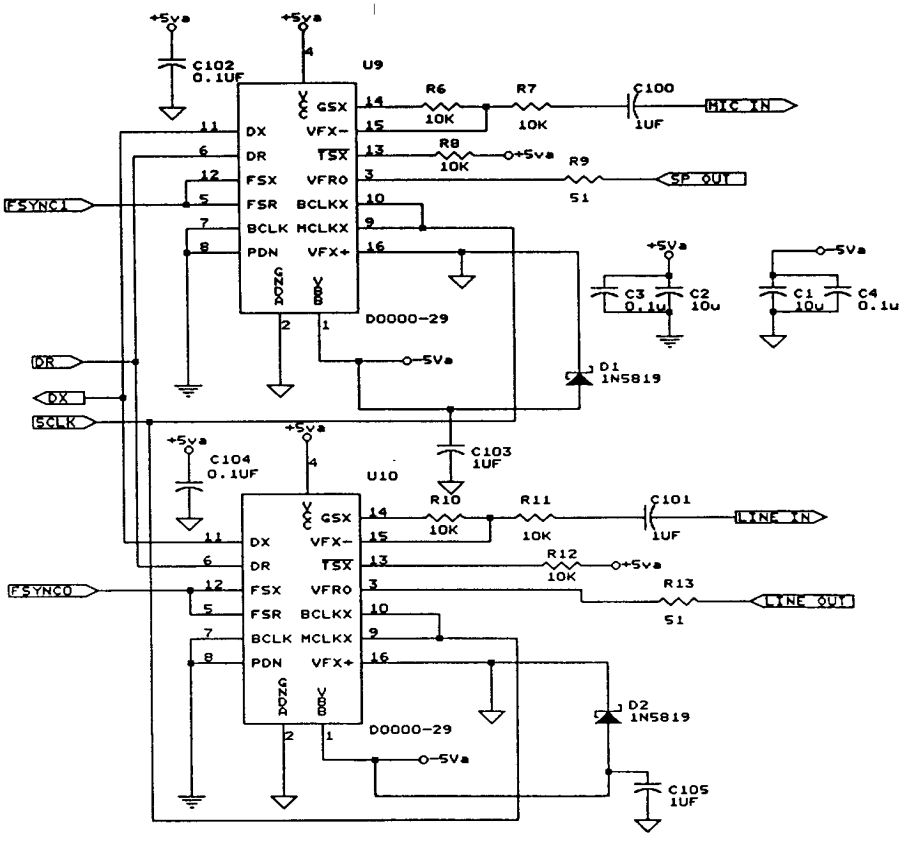

Figure 11. D0000-29 CODEC Interconnection Diagram

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HOST—D7002A COMMUNICATION INTERFACE

The host communication port is a 16-bit bidirectional register. The D7002A will access this register internally by one 16-bit wide access. The HOST accesses this register via the 8-bit bus in two accesses: first low byte then a high byte.

After the HOST writes command to the High byte of this register the D7002A accepts this command.

When the D7002A reads the communication register, this flag is reset. When the D7002A writes a status word to the communication register it sets the ACK pin low (external pin) which is connected to the HOST for indication. The host can use this pin as an interrupt or poll this signal periodically. When the HOST reads the high byte of this register it sets the ACK bit high. The choice of high/low byte for the host will be made by the HI/LO pin. The host should read the low byte of the status word first, then the high byte.

The D7002A will send a status word only in response to a host command

Figure 12 shows the host interface for the D7002A—PC. Figure 13 shows timing data for the D7002A Communication Interface.

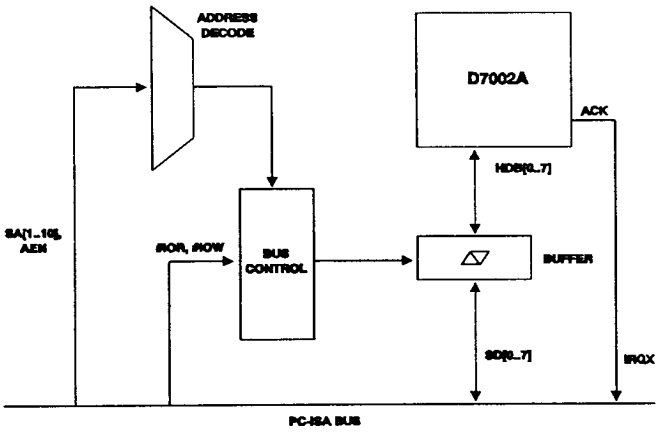

Figure 12. PC Interface

Table 1. Communication Interface Signals

Pin Name	Type(*)	Description
HSTDB[0..7]	Input/Output	HOST 8-bit data bus
HSTRD	Input	HOST READ line from register
HSTWR	Input	HOST WRITE line into register
ACK	Output	Flag to HOST–status byte ready in register
HI/LO	Input	High or Low byte select

*Input and Output are referenced to the D7002A-11.

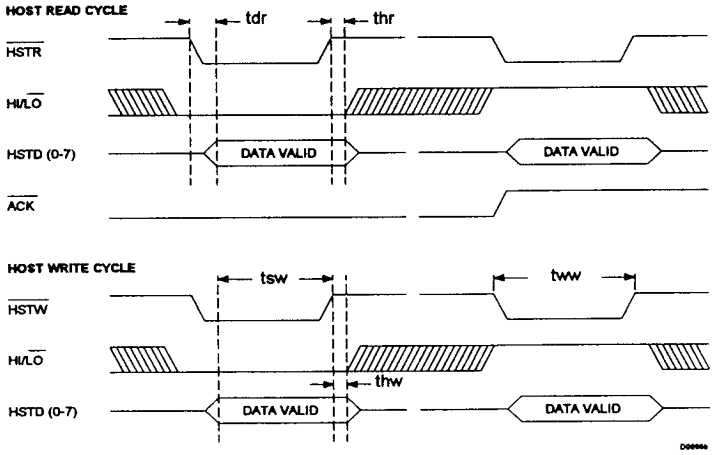

Figure 13. D6275A - Host Interface Timing Data

thr:	= 5ns min
tdr:	=20ns max
thw:	= 5ns min
tsw:	= 20ns min
tww:	= 20ns min

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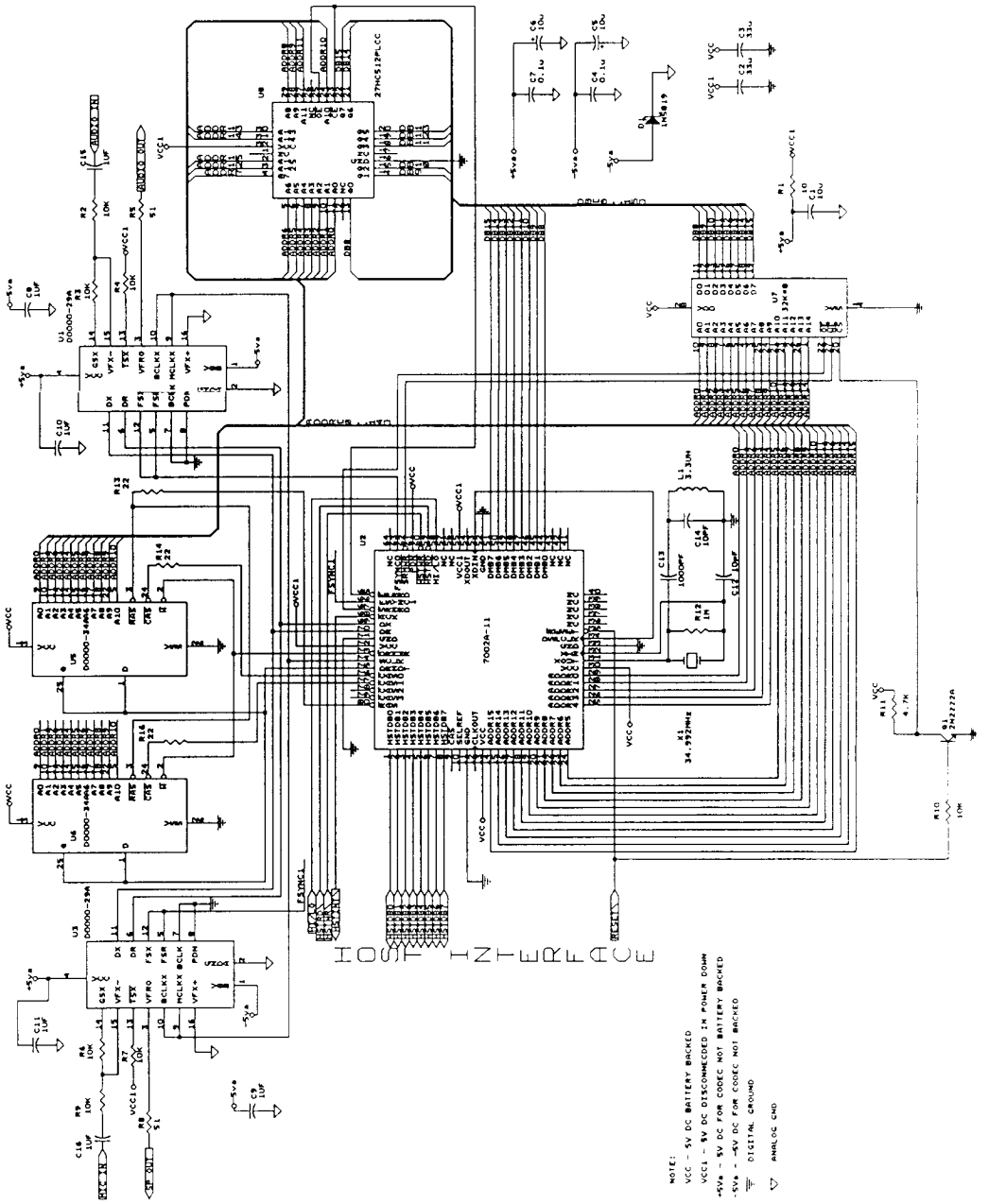

Figure 14. Chipset Interconnection Diagram with One Crystal

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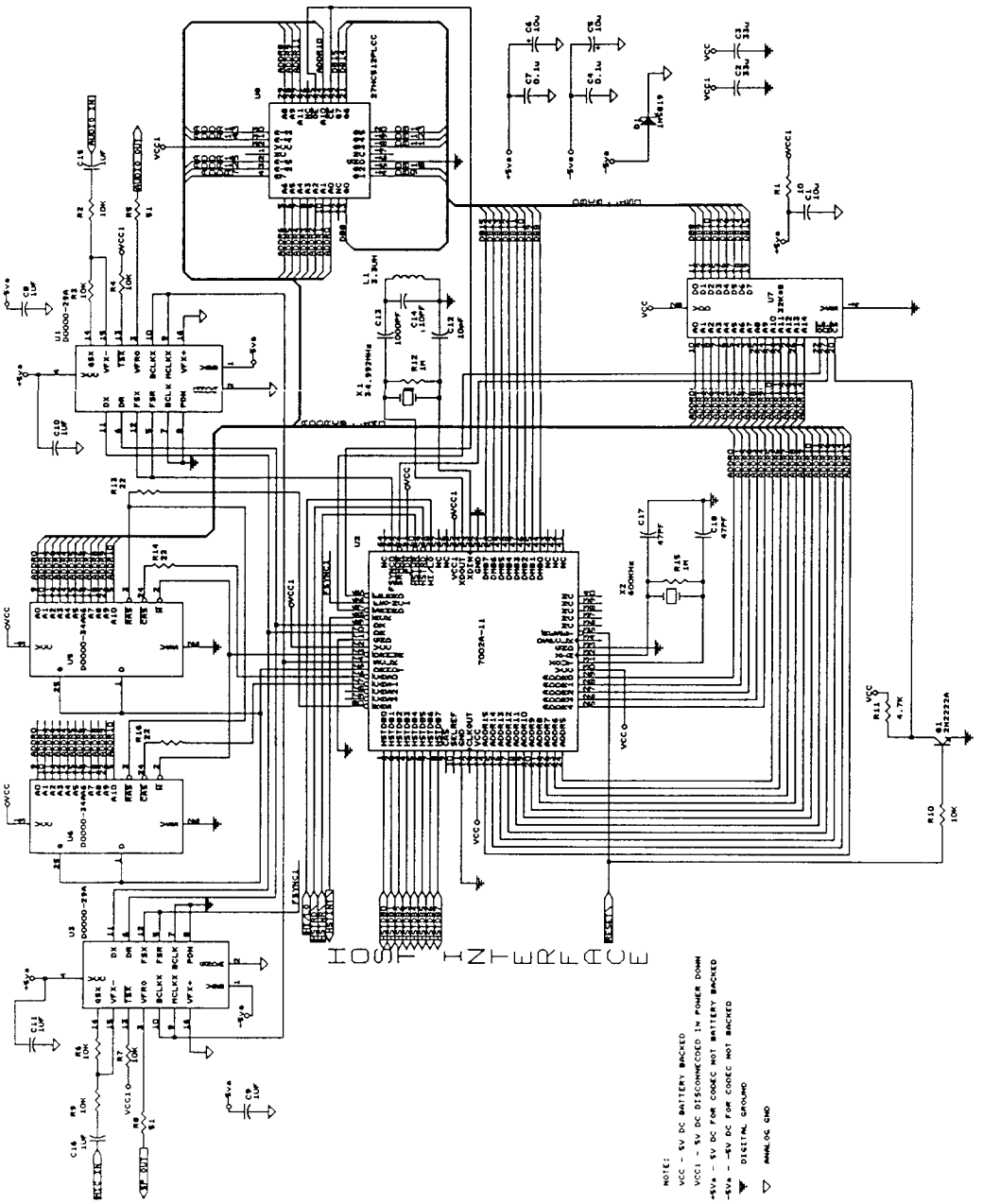

Figure 15. Chipset Interconnection Diagram with Two Oscillators

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APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high audio quality. To achieve this, the designer has to be conscious of noise both in the D7002A chipset and the front-end analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through. Other causes of concerns are ground loops and digital feedthrough.

Layout Hints

Ensure that the layout for printed circuit board has digital and analog signal lines separated as much as possible. Take care not to run any digital track along side an analog signal. Guard the analog input with GNDA. Establish a single point analog ground separate from the digital ground. Low impedance analog and digital power supply common returns are essential to low noise operation.

Power Supply Considerations

Since the D7002A is a chipset with analog input and output, its performance (especially the analog front-end) may be adversely affected by the noise of the power supply. In order to prevent mixing of noise, observe the following cautions:

- Separate the power supply to the digital parts and analog parts.
- GNDs of two power supplies should be connected at only one point. Furthermore, that connecting point should be close to the supplies. This will minimize the effect of noise from the digital power supply to the analog power supply.

The power supply should have the least ripple possible, and a series regulator power supply is recommended for best condition.

Good engineering practice calls for proper supply decoupling between the various components. This may be achieved by running separate Vcc and ground return lines to the D7002A and ARAMS and placing 0.1 µF ceramic decoupling capacitors near each Vcc supply pin.

Microphone and Speaker Considerations

An often overlooked fact is that the sound quality produced by D7002A chipset is directly related to the quality of the microphone and speaker connected to them. Use a good quality microphone and speaker with good frequency response. Design carefully the microphone preamplifier circuit. The physical location of the microphone, along with the characteristics of the microphone, play a large role in the playback sound quality.

Codec Input/Output Gain

There is difference in input and output gain of the two codecs D0000-26 and D0000-29 that can be used in the D7002A chipset. The gain of transmit and receive path is measured at 1020 Hz with 600 ohm load. For the D0000-29 the nominal gain for both paths is 4 dBm. The D0000-26 has 2.76 dBm gain in the transmit path and 5.76 dBm gain in the receive path. This causes that the D0000-26 has 3 dB gain when in loopback mode while the D0000-29 gain is 0 dB. To get completely identical gains in the both paths we recommend to the following modifications in the D7002A chipset with D0000-29 codec:

1. Increase the value of resistor R3 from 10K to 11.2K to compensate for the higher gain of the transmit path . The difference is 1.24 dBm (1.153).
2. Add additional external gain to the analog output to compensate for the lower gain of the receive path. The difference is 1.76 dBm (1.224).

Battery Backup

While the D7002A is in power down mode, power is supplied to the D7002A-11, SRAM , ARAMs and EPROM. In this mode the D7002A-11 generates the necessary refresh cycles for the ARAMs. The SRAM and EPROM are not active. The typical power dissipation of the D7002A-11 is 6 mA. The typical power dissipation of D0000-34 is 3 mA. Following is analysis for several chipset configurations and available backup time.

Battery Type	Configuration	Recording time	Battery Backup
1 x 9V (500 mAH)	1 x D0000-34	10 minutes	55 hours
4 x AAA (850 mAH)	1 x D0000-34	10 minutes	94 hours
4 x AA (1700 mAH)	2 x D0000-34	20 minutes	141 hours
NiCd 4 x AA(500 mAH)	1 x D0000-34	10 minutes	55 hours

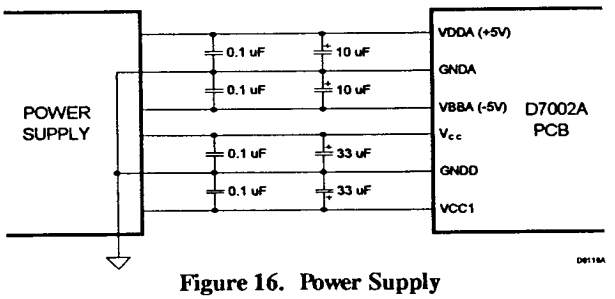

Figure 16. Power Supply

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ELECTRICAL CHARACTERISTICS

D7002A-11

Absolute maximum ratings over specified temperature range

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input voltage range	-0.5 V to (Vcc + 0.5 V)
Output voltage range	-0.5 V to (Vcc + 0.5 V)
Continuous output current	±25 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{SS} Supply voltage			0		V
V_{IH} High-level input voltage	All inputs except PDN and RESET	2			V
V_{IL} Low-level input voltage	PDN and RESET			0.8	V
VT+ Positive-going RESET and PDN threshold voltage			3.35		V
VT- Negative-going RESET and PDN threshold voltage			1.65		V
I_{OH} High-level output current				-4	mA
I_{OL} Low-level output current				4	mA
Crystal oscillator (100 ppm)			34.992		MHz
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage		I_{OH} = MAX	3.7	3		V
		I_{OH} = -20 µA		VCC -0.1		
V_{OL} Low-level output voltage		I_{OL} = MAX		0.3	0.5	V
I_{oz} Off-state output current		V_O = V_{CC} or 0 V			±5	µA
I_I Input current		V_I = V_{CC} or 0 V			±1	µA
ICC Supply current	Operating Mode	f = 35 MHz, VCC = 5.5 V		32.4		mA
	Suspend Mode	34.992 MHz single crystal configuration		6		mA
		Dual oscillator configuration (34.992 MHz and 600 KHz)		5		mA
CI Input capacitance	Data bus	f = 1 MHz, All other pins 0 V		10		pF
	All others			5		
CO Output capacitance	Data bus	f = 1 MHz, All other pins 0 V		25		pF
	All others			20		

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ADDR 0–11					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP***	**MAX**	**UNIT**
V_{OH} High-level output voltage	I_{OH} = –8 mA	3.7			V
	I_{OH} = –20 µA		V_{CC}–0.1		
V_{OL} Low-level output voltage	I_{OL} = 8 mA		0.2	0.4	V
	I_{OL} = 20 µA		0.05	0.1	
ACK, ADDR 12–15					
V_{OH} High-level output voltage	I_{OH} = –4 mA	3.7			V
	I_{OH} = –20 µA	V_{CC}–0.1			
Icc Supply Current	Active Power Down		20 6		mA
V_{OL} Low-level output voltage	I_{OL} = 4 mA		0.2	0.5	V
	I_{OL} = 20 µA		0.05	0.1	
HSTDB0-7, DB8-DB15					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP***	**MAX**	**UNIT**
V_{OH} High-level output voltage	I_{OH} = –4 mA	3.7			V
	I_{OH} = –20 µA	V_{CC}–0.1			
V_{OL} Low-level output voltage	I_{OL} = 4 mA			0.5	V
	I_{OL} = 20 µA			0.1	V
I_{OZ} Off-state output current	V_O = V_{CC}			±10	µA
	V_O = 0		–70		µA
HSTRD, HSTWR, HI/LO					
I_I Input current	V_I = V_{CC}			±1	µA
	VI = 0		–70		
RESET					
VT+ Positive-going threshold level			3.35	3.85	V
VT– Negative-going threshold level		0.9	1.65		V

*Typical values are at V_{CC} = 5 V, T_A = 25°C.

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D0000-29 (Analog I/O interface)

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	–0.3 V to 7 V
Output voltage, V_O	–0.3 V to 7 V
Input voltage, V_I	–0.3 V to 7 V
Digital ground voltage	–0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

Recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		4.75	5	5.25	V
V_{BB} Supply voltage		–4.75	–5	–5.25	V
V_{IH} High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL} Low-level input voltage, all inputs except CLKSEL				0.6	V
R_L Load resistance	No change transmit	10			kΩ
	At VFR0 Receive	600			Ω
C_L Load capacitance	At GSX			50	pF
	At VFR0			500	
T_A Operating free-air temperature		0		70	°C

Electrical characteristics over recommended ranges of supply voltage and operating free-air temperature supply current, f_{DCLK} 2.048 MHz, outputs not loaded

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
I_{CC} Supply current from V_{CC}	Operating		6	9	mA
	Power-down		0.5	1.5	
I_{BB} Supply Current from V_{BB}	Operating		–6	–9	mA
	Power-down		–0.5	–1.5	
Power dissipation	Operating		60	90	mW
	Power-down		5	15	

Transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±200	nA
Input offset voltage at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V			±20	mV
Common-mode rejection at ANLG IN+, ANLG IN –	V_I = –2.17 V to 2.17 V	60			dB
Open-loop voltage amplification at GSX		5000			V/V
Open-loop unity-gain bandwidth at GSX			2		MHz
Input resistance at ANLG IN+, ANLG IN –		10			MΩ

Receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage PWRO+, PWRO – (single-ended)	Relative to ANLG GND	–200		200	mV
Output resistance at PWRO+, PWRO –			1		Ω

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D0000-34A (4 Mbit ARAM)

Absolute maximum ratings over operating temperature range

Voltage range on any pin	–1 V to 5.50 V
Voltage range on V_{CC}	–1 V to 5.50 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

Recommended operating conditions

	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2.4		5.25	V
V_{IL} Low-level input voltage	–0.5		0.4	V
V_{OH} High-level output voltage	2.4			V
V_{OL} Low-level output voltage			0.4	V
T_A Operating free-air temperature range	0		70	°C

Electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
V_{OH} High level output voltage	I_{OH} = –mA	2.4		V
V_{OL} Low-level output voltage	I_{OL} = 3.0 mA		0.4	V
I_I Input current (leakage)	V_I = 0 V to 5.5 V, V_{CC} = 5.25 V, all other pins = 0 V to V_{CC}		±20	µA
I_O Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V, CAS high		±20	µA
I_{CC1} Read or write cycle current	Minimum cycle, V_{CC} = 5.25 V		80	mA
I_{CC2} Standby cycle	After 1 memory cycle, RAS and CAS high, V_{IH} = 2.2 V		5	mA
I_{CC3} Average refresh current	Minimum cycle, V_{CC} = 5.25 V RAS cycling, CAS high		70	mA
I_{CC4} Average page (word) current	$t_{C(P)}$ = minimum, V_{CC} = 5.25 V RAS low, CAS cycling		35	mA

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DTMF & VOX Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
DTMF Signal level for detection *	–35		0	dB
DTMF Twist (High/Low Tone)			6	dB
DTMF Frequency Detect Band width	±(1.5% + 2Hz)		4.1%	%fc
DTMF Noise tolerance**			–12	dB
DTMF tone duration accept	40			ms
DTMF tone duration reject			20	ms
DTMF interdigit pause accept	40			ms
DTMF interdigit pause reject			20	ms
VOX detection	–43		0	dB
Tone generator frequency accuracy	-1		+1	%fc
Tone generator 0 dB definition***		+12		dBm
Tone generator level accuracy	-1		+1	dB

*1 V RMS is defined as 0 dB

**BW limited (0–3.4KHz) Gaussian noise

***DTMF generation 0 dB definition is +13 dBm for high tone and +11 dBm for low tone

CALL PROGRESS TONE DETECTOR PERFORMANCE

Narrow band detection level: minimum -35dB
Narrow band rejection level: less than -40dB
Narrow band rejection frequency range: less than 250Hz or greater than 600Hz
Narrow band frequency range: between 330Hz and 500Hz
Wide band detection level: minimum -35dB
Wide band rejection level: less than -40dB
Wide band rejection frequency range: less than 250Hz or greater than 750Hz
Wide band detection frequency range: between 330Hz and 650Hz
1.4V RMS is defined as 0 dB for single tone input.
Noise tolerance -12 dB*

CNG DETECTOR PERFORMANCE

Detection level: minimum -38dB
Rejection level: less than -45dB
Detection frequency range: between 1062 and 1138
Rejection frequency range: less than 1000 Hz and more than 1200 Hz
1.4V RMS is defined as 0 dB
Noise tolerance -12 dB*

*BW limited (0-3.4 KHz) Gaussian noise

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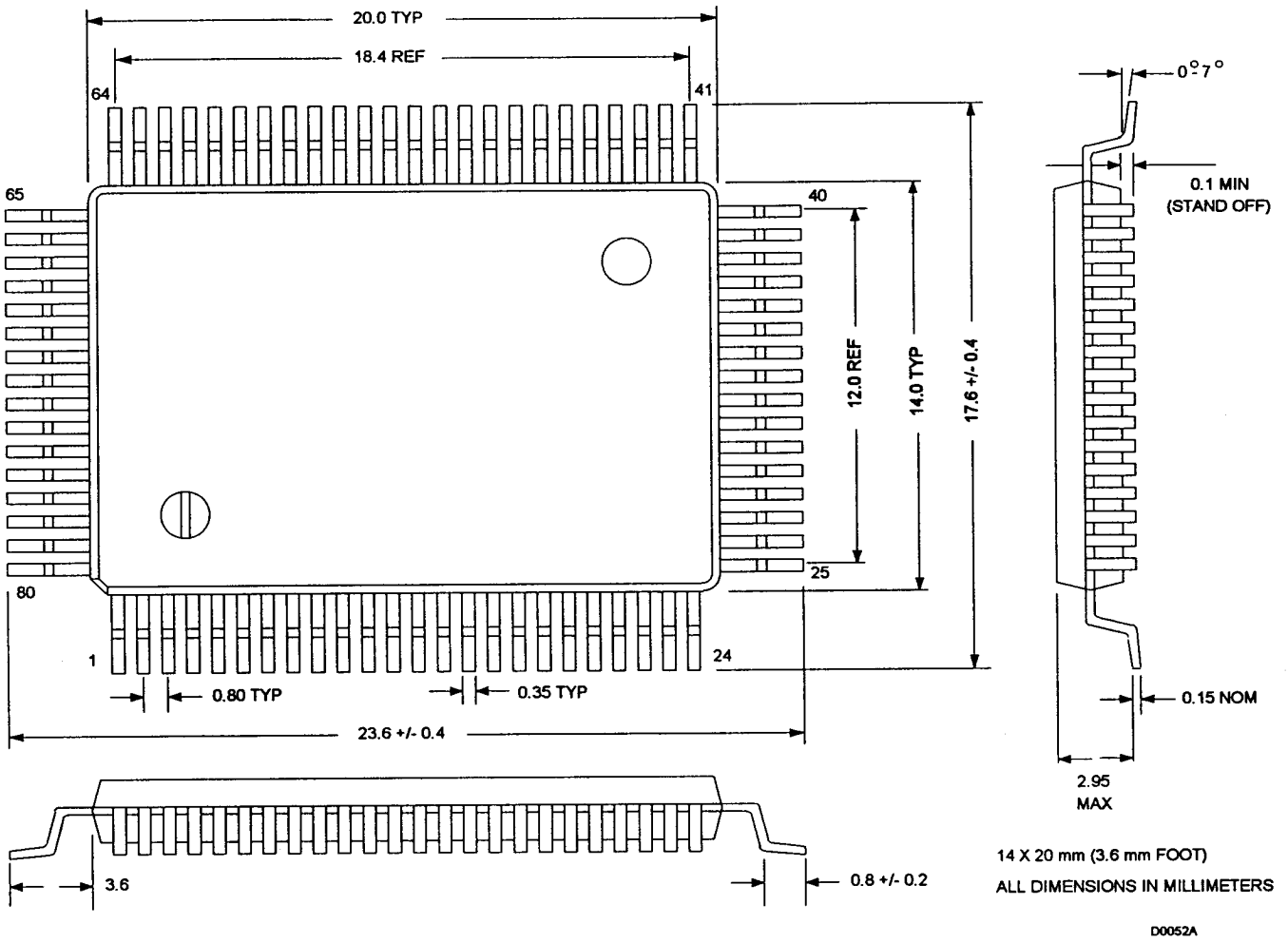

Figure 17. D7002A-11 Mechanical Data

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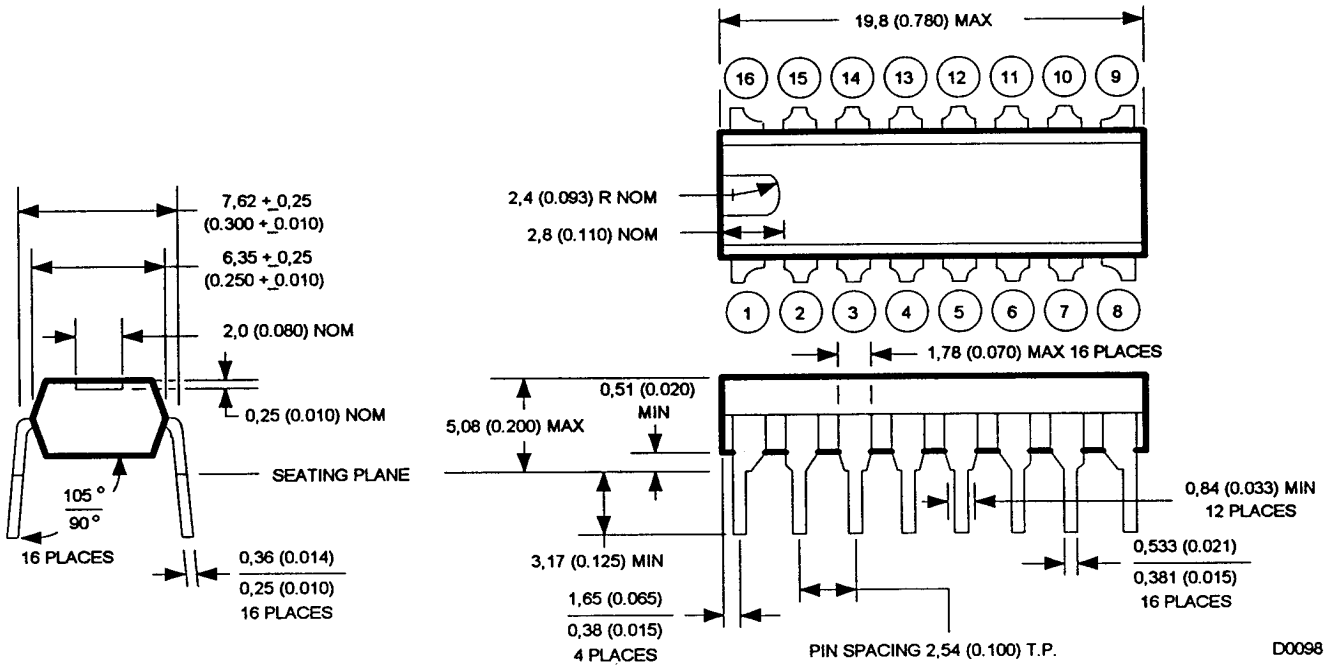

Figure 18. D0000-29 Codec Mechanical Data

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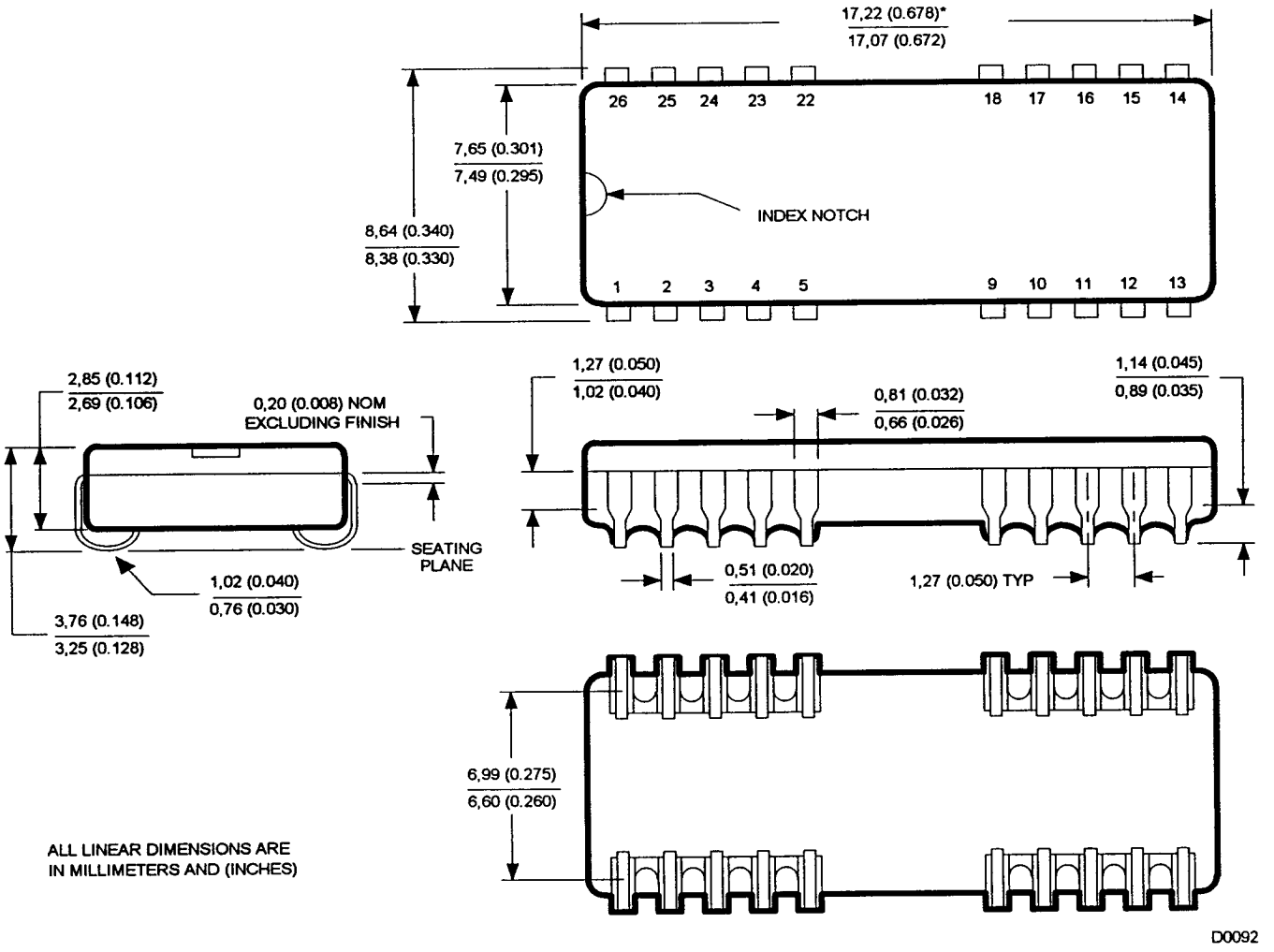

Figure 19. D0000-34 ARAM SOJ Mechanical Data

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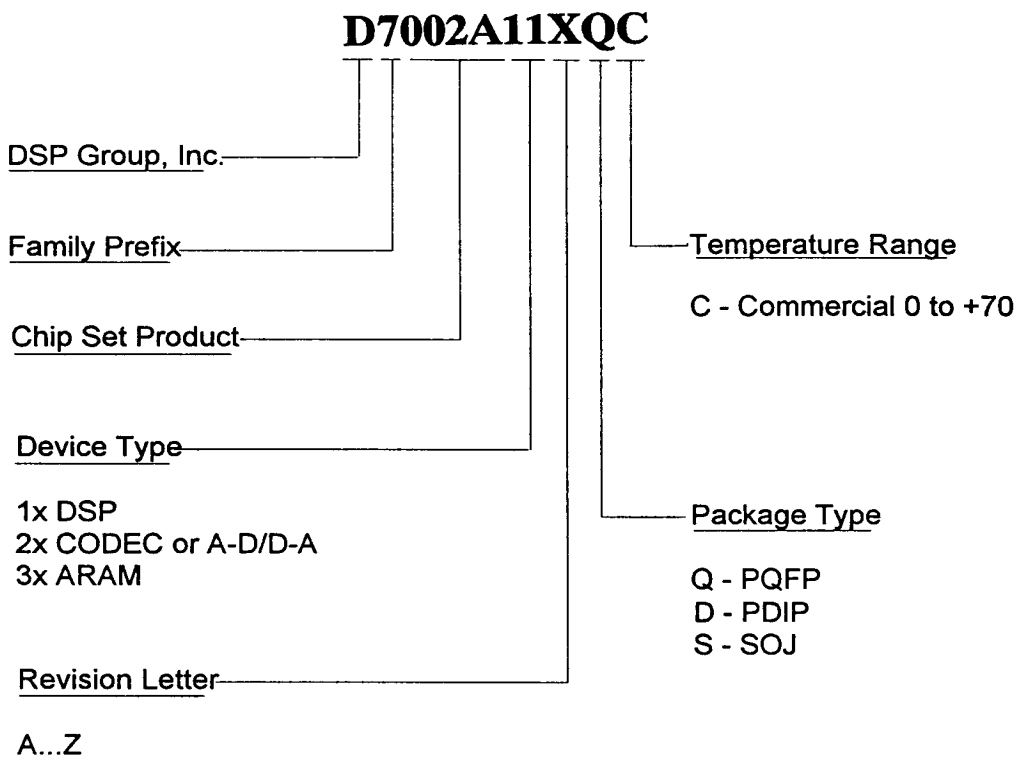
DSPG CHIP SET PART NUMBER SYSTEM



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