19-2339; Rev 0; 1/02

EVALUATION KIT AVAILABLE

Upstream CATV Amplifier

General Description

The MAX3503 programmable power amplifier is designed for use in CATV upstream applications. The MAX3503 drives 61dBmV (QPSK) into a 75Ω load when driven with a 34dBmV nominal input signal. Both input and output ports are differential, requiring that an external balun be used at the output port. The variable gain feature provides greater than 56dB of dynamic range, which is controlled by an SPI™ 3-wire interface. Gain control is available in 0.5dB steps. The device operates over a frequency range of 5MHz to 65MHz. The MAX3503 is internally matched for use with a 1:1 balun.

This device operates from a single 3.3VDC supply and draws 235mA during transmit (100% duty cycle, 61dBmV out). The bias current is automatically adjusted, based on the output level to increase efficiency. Additionally, the device can be disabled between bursts to minimize noise and save power while maintaining a match at the output port. In addition, a shutdown mode is available to disable all circuitry and reduce current consumption to 5µA (typ).

The MAX3503 is available in a 20-pin QFN package. The device operates in the extended industrial temperature range (-40°C to +85°C).

Applications

DOCSIS™/EuroDOCSIS™ and DVB Cable Modems

OpenCable™ Set-Top Box

Telephony Over Cable

CATV Status Monitor

Typical Operating Circuit appears at end of data sheet.

SPI is a trademark of Motorola, Inc.

DOCSIS/EuroDOCSIS/OpenCable are trademarks of CableLabs®.

Features

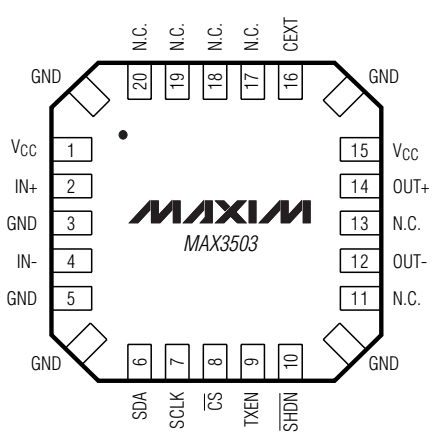
- **Single 3.3V Supply Operation**
- **Accurate Gain Control, ±1dB over 53dB Range**
- **Gain Programmable in 0.5dB Steps**
- **-55dBc Harmonic Distortion at 65MHz**
- **Low Burst On/Off Transient**
- **High Efficiency: 182mW at 34dBmV Out; 16mW in Transmit-Disable Mode**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3503EGP	-40°C to +85°C	20 QFN-EP* (5mm × 5mm)

**Exposed pad*

Pin Configuration



QFN**

****NOTE:** CORNER GND PINS AND THE EP MUST BE SOLDERED TO THE SUPPLY GROUND.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, OUT+, OUT-.....-0.5V to +6.5V
Input Voltage Levels (all inputs).....-0.3V to (V_{CC} + 0.3V)
Continuous Input Voltage (IN+, IN-).....$2V_{P-P}$
Continuous Current (OUT+, OUT-).....175mA
Continuous Power Dissipation (T_A = +85°C)
20-Pin QFN (derate 27mW/°C above +85°C) 1600mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX3503EV kit; V_{CC} = 3.1V to 3.6V, V_{GND} = 0, TXEN = $\overline{SHDN}$ = high, T_A = -40°C to +85°C. Typical parameters are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.1		3.6	V
Supply-Current Transmit Mode	I_{CC}	D7 = 1, gain code = 115 (A_V = 27dB)		235	287	mA
		D7 = 0, gain code = 92 (A_V = 0dB)		55		
Supply-Current Transmit Disable Mode	I_{CC}	TXEN = low		4.8	7	mA
Supply-Current Low-Power Standby	I_{CC}	$\overline{SHDN}$ = low		5		µA
LOGIC INPUTS						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input High Current	I_{BIASH}	V_{INH} = V_{CC}			100	µA
Input Low Current	I_{BIASL}	V_{INL} = 0V	-100			µA

AC ELECTRICAL CHARACTERISTICS

(MAX3503 EV kit; V_{CC} = 3.1V to 3.6V, V_{GND} = 0, P_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, T_A = -40°C to +85°C. Typical parameters are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain, f_{IN} = 5MHz	A_V	D7 = 1, gain code = 119, T_A = 0°C to +85°C	27.0	28.5	30	dB
		D7 = 1, gain code = 99, T_A = 0°C to +85°C	17.0	18.5	20.0	
		D7 = 1, gain code = 83, T_A = 0°C to +85°C	9	10.5	12	
		D7 = 0, gain code = 112, T_A = 0°C to +85°C	8	9.5	11	
		D7 = 0, gain code = 92, T_A = 0°C to +85°C	-2	-0.5	1	
		D7 = 0, gain code = 72, T_A = 0°C to +85°C	-12	-11.5	-9	
		D7 = 0, gain code = 43, T_A = 0°C to +85°C	-27.5	-26.0	-24.5	
Voltage Gain, f_{IN} = 65MHz	A_V	D7 = 1, gain code = 119, T_A = -40°C to +85°C (Note 2)	26.3			dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3503 EV kit; V_{CC} = 3.1V to 3.6V, V_{GND} = 0, P_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, T_A = -40°C to +85°C. Typical parameters are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Rolloff		V_{OUT} = 61dBmV, f_{IN} = 5MHz to 42MHz, (Note 2)		-0.6	-1.2	dB
		V_{OUT} = 61dBmV, f_{IN} = 5MHz to 65MHz, (Note 2)		-1.1	-1.9	
Gain Step Size		f_{IN} = 5MHz to 65MHz, A_V = -26dB to 27dB		0.5		dB
		f_{IN} = 5MHz to 65MHz, A_V = -26dB to 27dB; any 2-bit transition of D0, D1	0.7	1.0	1.3	
		f_{IN} = 5MHz to 65MHz, D7 = 0, gain code = 112; to D7 = 1, gain code = 83	0.65	1.0	1.35	
Transmit-Disable Mode Noise		TXEN = low, BW = 160kHz, f_{IN} = 5MHz to 65MHz (Note 2)			-65	dBmV
Isolation in Transmit-Disable Mode		TXEN = low, f_{IN} = 5MHz to 65MHz (Note 2)	60			dB
Transmit Mode Noise		BW = 160kHz, f_{IN} = 5MHz to 65MHz, A_V = -26dB to 27dB (Note 2)			-55.8	dBc
Transmit Enable Transient Duration		TXEN input rise/fall time < 0.1µs, T_A = +25°C (Note 2)			2	µs
Transmit Disable Transient Duration		TXEN input rise/fall time < 0.1µs, T_A = +25°C (Note 2)			2	µs
Transmit Disable/Transmit Enable Transient Step Size		D7 = 1, gain code = 115 (A_V = 27dB), T_A = +25°C		30	80	mV_{P-P}
		D7 = 0, gain code = 83 (A_V = 11dB), T_A = -40°C to +85°C			20	
		D7 = 0, gain code = 92 (A_V = 0dB), T_A = +25°C		3		
Input Impedance	Z_{IN}	f_{IN} = 5MHz to 65MHz, differential (Note 2)		2		kΩ
Output Return Loss		f_{IN} = 5MHz to 65MHz, in 75Ω system, D7 = 1, gain code = 119, (A_V = 27dB)		10		dB
Output Return Loss in Transmit-Disable Mode		f_{IN} = 5MHz to 65MHz, in 75Ω system, TXEN = low		10		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX3503 EV kit; V_{CC} = 3.1V to 3.6V, V_{GND} = 0, P_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, T_A = -40°C to +85°C. Typical parameters are at T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Two-Tone Third-Order Distortion	IM3	Input tones at 42MHz and 42.2MHz, both 31dBmV, V_{OUT} = 58dBmV/tone (Note 2)		-53	-47	dBc
		Input tones at 65MHz and 65.2MHz, both 31dBmV, V_{OUT} = 58dBmV/tone		-49		
2nd Harmonic Distortion	HD2	f_{IN} = 33MHz, V_{OUT} = 61dBmV		-55	-50	dBc
		f_{IN} = 65MHz, V_{OUT} = 61dBmV (Note 2)		-55	-50	
3rd Harmonic Distortion	HD3	f_{IN} = 22MHz, V_{OUT} = 61dBmV		-55	-50	dBc
		f_{IN} = 65MHz, V_{OUT} = 61dBmV		-55	-50	

TIMING CHARACTERISTICS

(V_{CC} = 3.1V to 3.6V, V_{GND} = 0V, TXEN = $\overline{SHDN}$ = high, T_A = +25°C, D7 = 1, unless otherwise specified.)

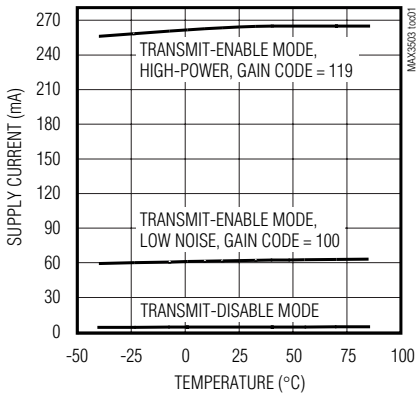
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEN-to-SCLK Rise Set Time	t_{SENS}			20		ns
SEN-to-SCLK Rise Hold Time	t_{SENH}			20		ns
SDA-to-SCLK Setup Time	t_{SDAS}			20		ns
SDA-to-SCLK Hold Time	t_{SDAH}			20		ns
SDA Pulse-Width High	T_{DATAH}			50		ns
SDA Pulse-Width Low	T_{DATAL}			50		ns
SCLK Pulse-Width High	t_{SCLKH}			50		ns
SCLK Pulse-Width Low	t_{SCLKL}			50		ns

Note 1: All parameters guaranteed by design and characterization to ±3 sigma for T_A < +25°C, unless otherwise specified.
Note 2: Guaranteed by design and characterization to ±6 sigma.

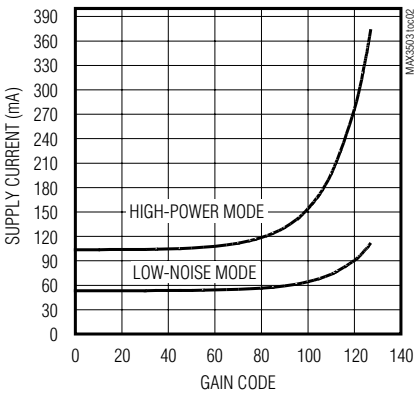
Typical Operating Characteristics

(Typical applications circuit; V_{CC} = 3.3V, V_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, f_{IN} = 20MHz, Z_{LOAD} = 75Ω, T_A = +25°C, unless otherwise noted.)

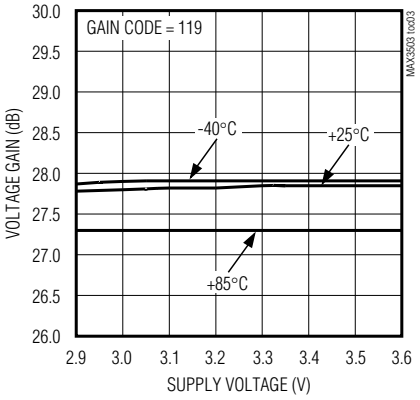
SUPPLY CURRENT vs. TEMPERATURE



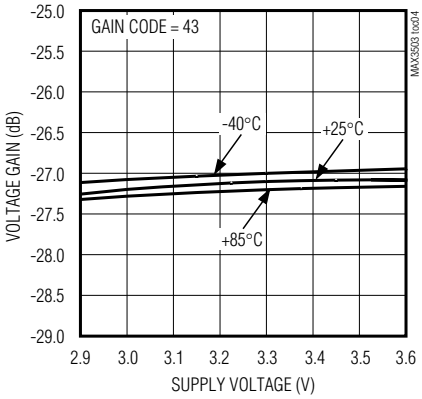
SUPPLY CURRENT vs. GAIN CODE



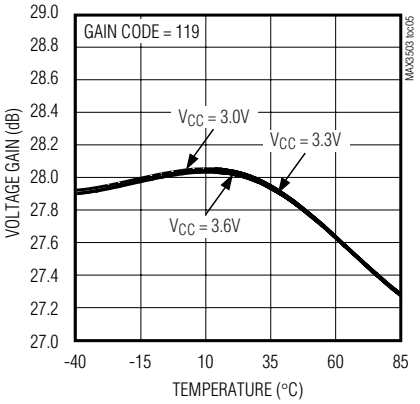
VOLTAGE GAIN vs. SUPPLY VOLTAGE HIGH-POWER MODE



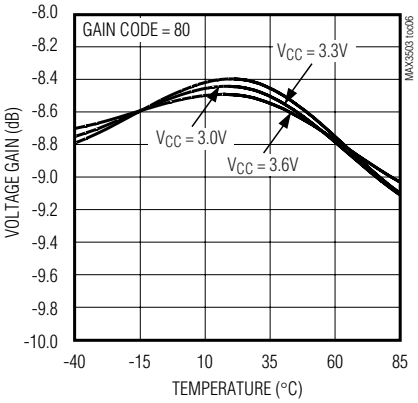
VOLTAGE GAIN vs. SUPPLY VOLTAGE LOW-NOISE MODE



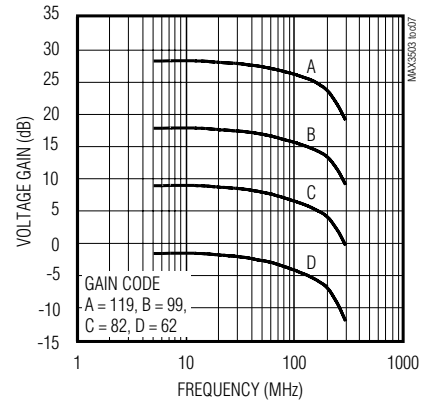
VOLTAGE GAIN vs. TEMPERATURE HIGH-POWER MODE



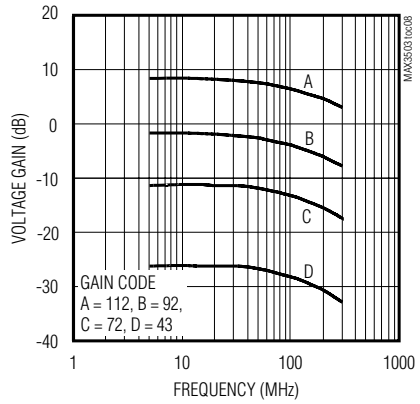
VOLTAGE GAIN vs. TEMPERATURE LOW-NOISE MODE



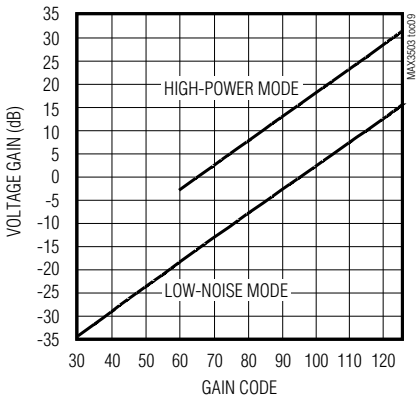
VOLTAGE GAIN vs. FREQUENCY HIGH-POWER MODE



VOLTAGE GAIN vs. FREQUENCY LOW-NOISE MODE



VOLTAGE GAIN vs. GAIN CODE

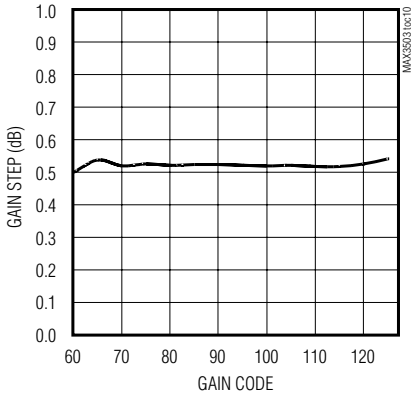


Upstream CATV Amplifier

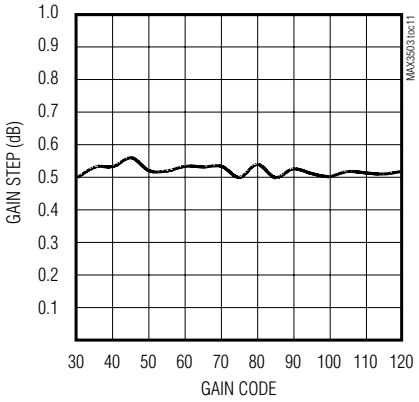
Typical Operating Characteristics (continued)

(Typical applications circuit; V_{CC} = 3.3V, V_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, f_{IN} = 20MHz, Z_{LOAD} = 75Ω, T_A = +25°C, unless otherwise noted.)

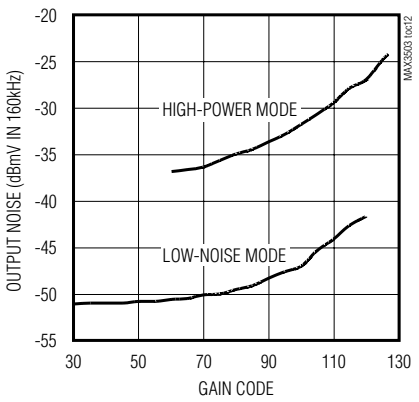
GAIN STEP vs. GAIN CODE HIGH-POWER MODE



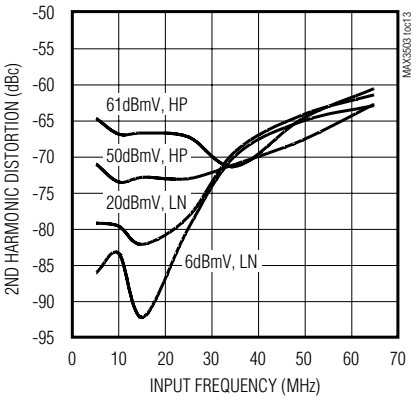
GAIN STEP vs. GAIN CODE LOW-NOISE MODE



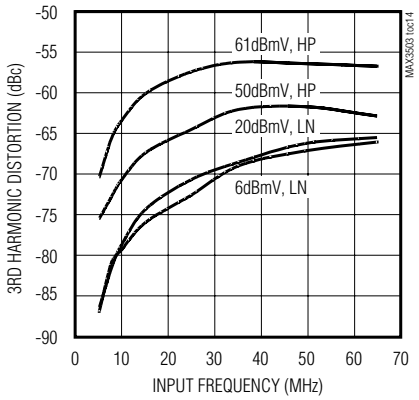
TRANSMIT NOISE vs. GAIN CODE



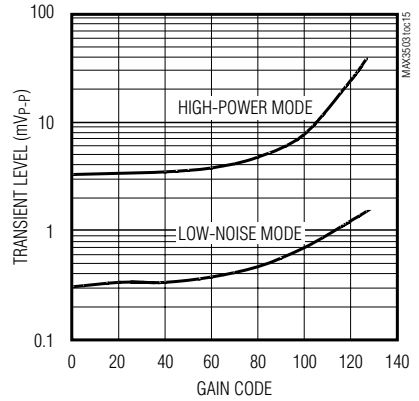
2ND HARMONIC DISTORTION vs. INPUT FREQUENCY



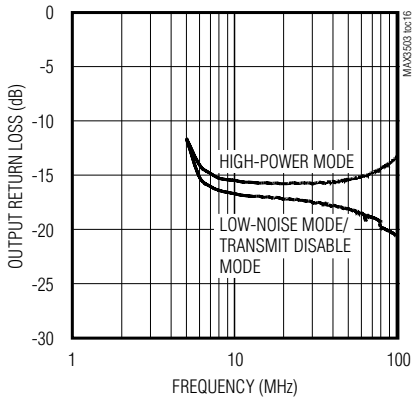
3RD HARMONIC DISTORTION vs. INPUT FREQUENCY



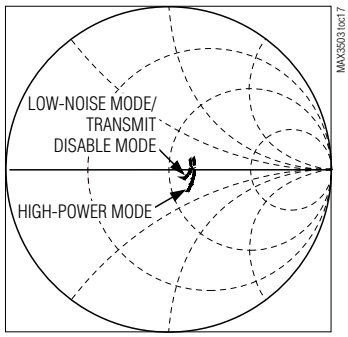
POWER-UP/DOWN TRANSIENTS vs. GAIN CODE



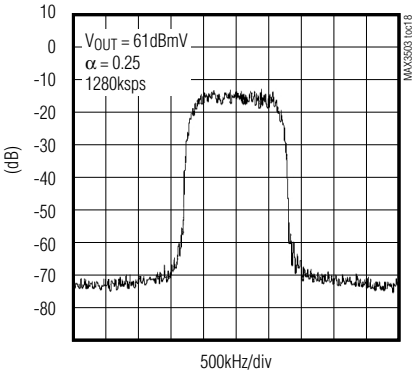
OUTPUT RETURN LOSS vs. FREQUENCY (75Ω SYSTEM)



OUTPUT IMPEDANCE (75Ω SYSTEM)

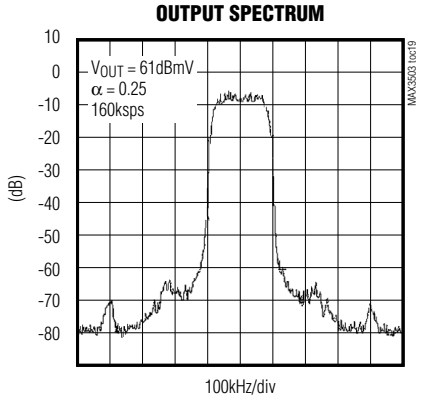


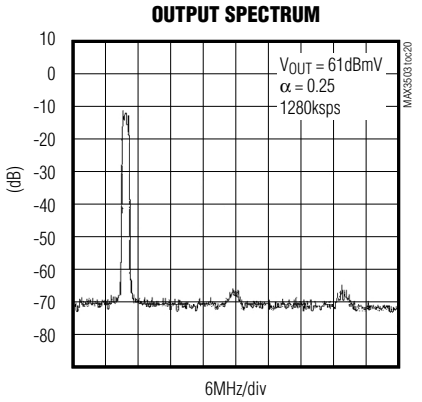
OUTPUT SPECTRUM



Typical Operating Characteristics (continued)

(Typical applications circuit; V_{CC} = 3.3V, V_{IN} = 34dBmV, TXEN = $\overline{SHDN}$ = high, f_{IN} = 20MHz, Z_{LOAD} = 75Ω, T_A = +25°C, unless otherwise noted.)



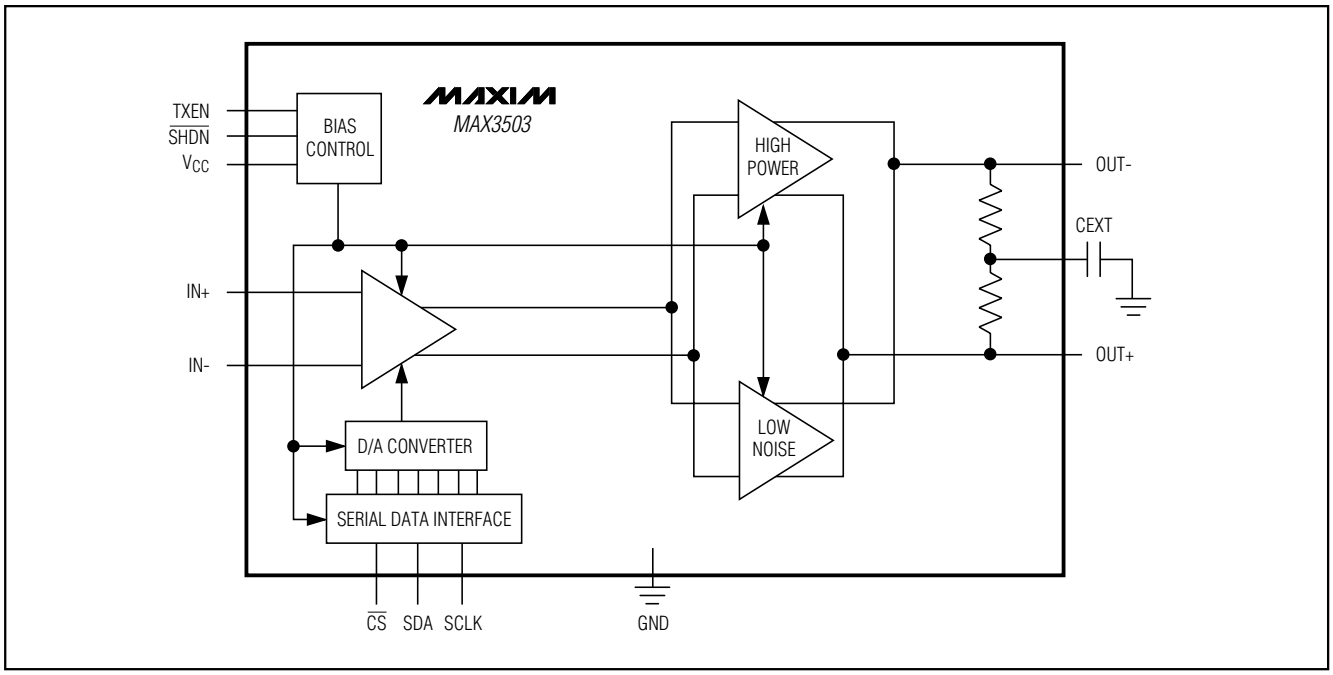


Pin Description

PIN	NAME	DESCRIPTION
1	V_{CC}	Programmable-Gain Amplifier (PGA) 3.3V Supply. Bypass to GND with a 0.1µF decoupling capacitor as close to the part as possible.
2	IN+	Positive PGA Input. Along with IN-, this port forms a high-impedance differential input to the PGA. Driving this port differentially increases the rejection of second-order distortion at low output levels.
3	GND	PGA RF Ground. As with all ground connections, maintain the shortest possible (low-inductance) length to the ground plane.
4	IN-	Negative PGA Input. When not used, this port must be AC-coupled to ground. See IN+.
5	GND	Ground
6	SDA	Serial-Interface Data. TTL-compatible input. See *Serial Interface* section.
7	SCLK	Serial-Interface Clock. TTL-compatible input. See *Serial Interface* section.
8	$\overline{CS}$	Serial-Interface Enable. TTL-compatible input. See *Serial Interface* section.
9	TXEN	Transmit Enable. Drive TXEN high to place the device in transmit-enable mode.
10	$\overline{SHDN}$	Shutdown. When $\overline{SHDN}$ is set low, all functions (including the serial interface) are disabled.
11,13,17–20	N.C.	No Connection
12	OUT-	Negative Output. Along with OUT+, this port forms a 75Ω impedance output. This port is matched to a 75Ω load using a 1:1 transformer.
14	OUT+	Positive Output. See OUT-.
15	V_{CC}	Output Amplifier Bias, 3.3V Supply. Bypass to GND with a 0.1µF decoupling capacitor as close to the part as possible.
16	CEXT	RF Output Bypass. Bypass to GND with a 0.1µF capacitor.
Exposed Paddle	GND	Ground

Upstream CATV Amplifier

Functional Diagram



Detailed Description

Programmable-Gain Amplifier

The PGA consists of the variable-gain amplifier (VGA) and the digital-to-analog converter (DAC), which provide better than 56dB of output-level control in 0.5dB steps. The PGA is implemented as a programmable Gilbert-cell attenuator. The gain of the PGA is determined by a 7-bit word (D6–D0) programmed through the serial data interface (Tables 1 and 2).

Specified performance is achieved when the input is driven differentially. The device may be driven single ended. To drive the device in this manner, one of the input pins must be capacitively coupled to ground. Use a capacitor value large enough to allow for a low-impedance path to ground at the lowest frequency of operation. For operation down to 5MHz, a 0.001µF capacitor is recommended.

Output Amplifiers

The output amplifiers are Class A differential amplifiers, capable of driving 61dBmV (QPSK) differentially. This architecture provides superior even-order distortion performance but requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the output amplifiers are powered down. A resistor is placed across the output, so that the output impedance remains matched when the amplifier is in transmit-disable mode. Disabling the output devices also results in low output noise.

To match the output impedance to a 75Ω load, the transformer must have a turns ratio of 1:1. The differential amplifier is biased directly from the 3.3V supply using the center tap of the output transformer. This provides a significant benefit when switching between transmit mode and transmit-disable mode. Stored energy due to bias currents cancels within the transformer and prevents switching transients from reaching the load.

Serial Interface

The serial interface has an active-low enable ($\overline{CS}$) to bracket the data, with data clocked in MSB first on the rising edge of SCLK. Data is stored in the storage latch on the rising edge of $\overline{CS}$. The serial interface controls the state of the PGA and the output amplifiers. Tables 1 and 2 show the register format. Serial-interface timing is shown in Figure 1.

Applications Information

High-Power and Low-Noise Modes

The MAX3503 has two transmit modes, high power (HP) and low noise (LN). Each of these modes is actuated by the high-order bit, D7, of the 8-bit programming word. When D7 is a logic 1, HP mode is enabled. When D7 is a logic 0, LN mode is enabled.

Each of these modes is characterized by the activation of a distinct output stage. In HP mode, the output stage exhibits 10.5dB higher gain than LN mode. The lower gain of LN output stage allows for significantly lower output noise and lower transmit-enable/transmit-disable transients.

The full range of gain codes (D6–D0) can be used in either mode. For DOCSIS applications, HP mode is recommended for output levels at or above 10.5dBmV (D7 = 1, gain code = 83), LN mode when the output level is below 9.5dBmV (D7 = 0, gain code = 112).

Shutdown Mode

In normal operation, the shutdown pin ($\overline{SHDN}$) is held high. When $\overline{SHDN}$ is taken low, all circuits within the IC are disabled. Only leakage currents flow in this state. Data stored within the serial-data interface latches are lost upon entering this mode. Current consumption is reduced to 5µA (typ) in shutdown mode.

Transformer

To match the output of the MAX3503 to a 75Ω load, a 1:1 transformer is required. This transformer must have adequate bandwidth to cover the intended application. Note that most RF transformers specify bandwidth with a 50Ω source on the primary and a matching resistance on the secondary winding. Operating in a 75Ω system tends to shift the low-frequency edge of the transformer bandwidth specification up by a factor of 1.5, because of primary inductance. Keep this in mind when specifying a transformer.

Bias to the output stage is provided through the center tap on the transformer primary. This greatly diminishes the on/off transients present at the output when switching between transmit and transmit-disable modes. Commercially available transformers typically have adequate balance between half-windings to achieve substantial transient cancellation.

Finally, keep in mind that transformer core inductance varies proportionally with temperature. If the application requires low temperature extremes (less than 0°C), adequate primary inductance must be present to sustain low-frequency output capability as temperatures drop. In general this is not a problem, as modern RF transformers have adequate bandwidth.

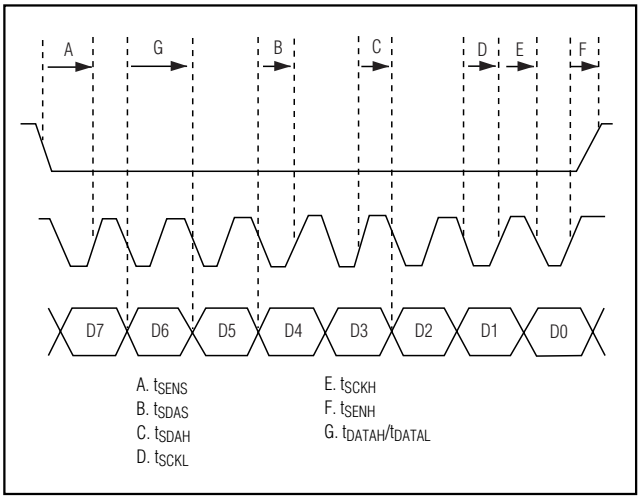


Figure1. Serial-Interface Timing Diagram

Table 1. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	High-power/low-noise mode select
6	D6	Gain code, bit 6
5	D5	Gain code, bit 5
4	D4	Gain code, bit 4
3	D3	Gain code, bit 3
2	D2	Gain code, bit 2
1	D1	Gain code, bit 1
LSB 0	D0	Gain code, bit 0

Input Circuit

To achieve rated performance, drive the inputs of the MAX3503 differentially with an appropriate input level. The differential input impedance is approximately 2kΩ. Most applications requires a differential lowpass filter preceding the device. The filter design dictates a terminating impedance of a specified value. Place this load impedance across the AC-coupled input pins (see *Typical Operating Circuit*).

The MAX3503 has sufficient gain to produce an output level of 61dBmV (QPSK) when driven with a 34dBmV input signal. When a lower input level is present, the maximum output level is reduced proportionally and output linearity increases. If an input level greater than 34dBmV is used, the 3rd-order distortion performance degrades slightly.

If single-ended sources drive the MAX3503, one of the input terminals must be capacitively coupled to ground

Table 2. Chip-State Control Bits

$\overline{SHDN}$	TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN CODE (DECIMAL)	STATES
0	X	X	X	X	X	X	X	X	X		Shutdown Mode
1	0	X	X	X	X	X	X	X	X		Transmit-Disable Mode
1	1	1	X	X	X	X	X	X	X		Transmit-Enable Mode, High Power
1	1	0	X	X	X	X	X	X	X		Transmit-Enable Mode, Low Noise
1	1	0	0	1	1	0	0	0	0	43	A_V = -26.0dB*
1	1	0	1	0	1	0	0	0	0	92	A_V = -0.5dB*
1	1	0	1	1	0	1	1	1	0	112	A_V = -95dB*
1	1	1	1	0	1	0	1	1	0	83	A_V = -10.5dB*
1	1	1	1	1	0	1	1	1	1	99	A_V = -18.5dB*
1	1	1	1	1	1	0	1	1	1	119	A_V = -28.5dB*

**Typical gain at +25°C, V_{CC} = 3.3V*

(IN+ or IN-). The value of this capacitor must be large enough to look like a short circuit at the lowest frequency of interest. For operation at 5MHz with a 75Ω source impedance, a value of 0.001µF suffices.

Layout Issues

A well-designed PC board is an essential part of an RF circuit. For best performance, pay attention to power-supply layout issues as well as to the output circuit layout.

Output Circuit Layout

The differential implementation of the MAX3503's output has the benefit of significantly reducing even-order distortion, the most significant of which is 2nd-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. Keep the trace lengths from the output pins equal.

Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the circuit. At the end of each of these traces is a decoupling capacitor that provides very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin.

The power-supply traces must be made as thick as is practical. Ground inductance degrades distortion performance. Therefore, make ground plane connections with multiple vias.

Exposed-Paddle Thermal Considerations

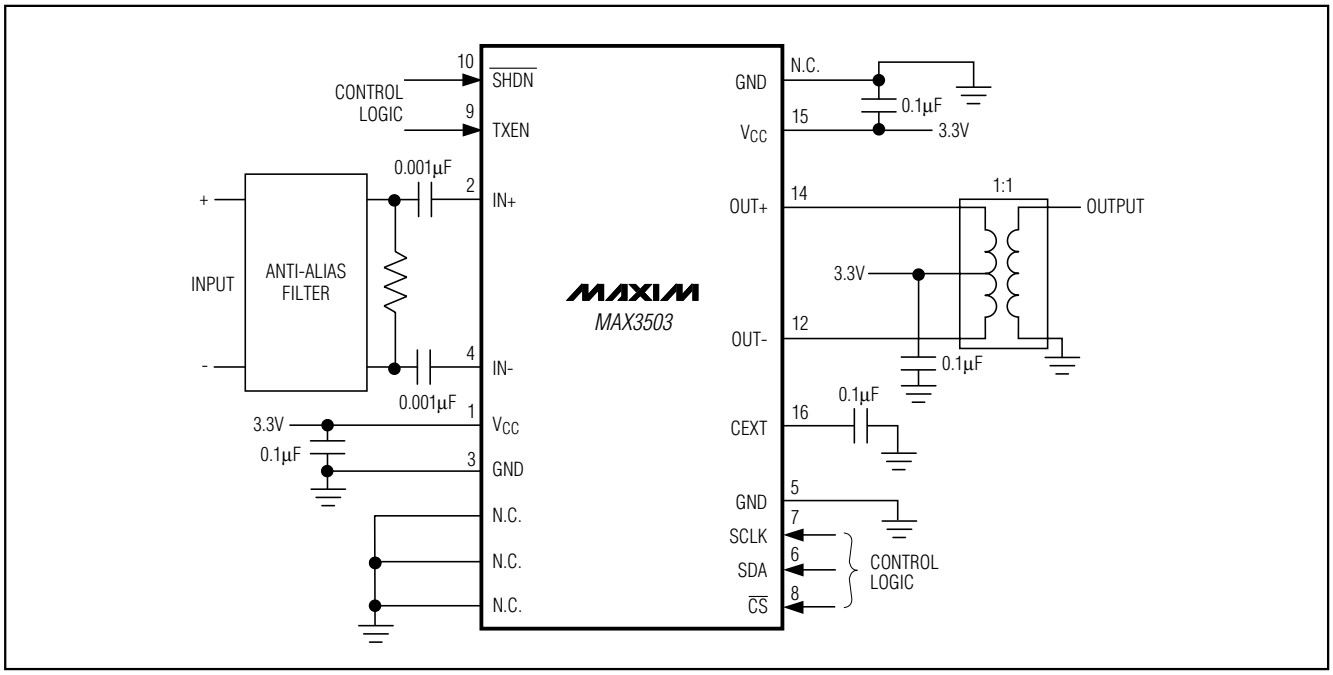
The MAX3503's 20-pin QFN package provides a low thermal-resistance path to the die. The PC board on which the MAX3503 is mounted must be designed to conduct heat from this contact. In addition, the EP should be provided with a low-inductance path to electrical ground. Maxim recommends that the EP be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Chip Information

TRANSISTOR COUNT: 1180

SUBSTRATE CONNECTED TO GND

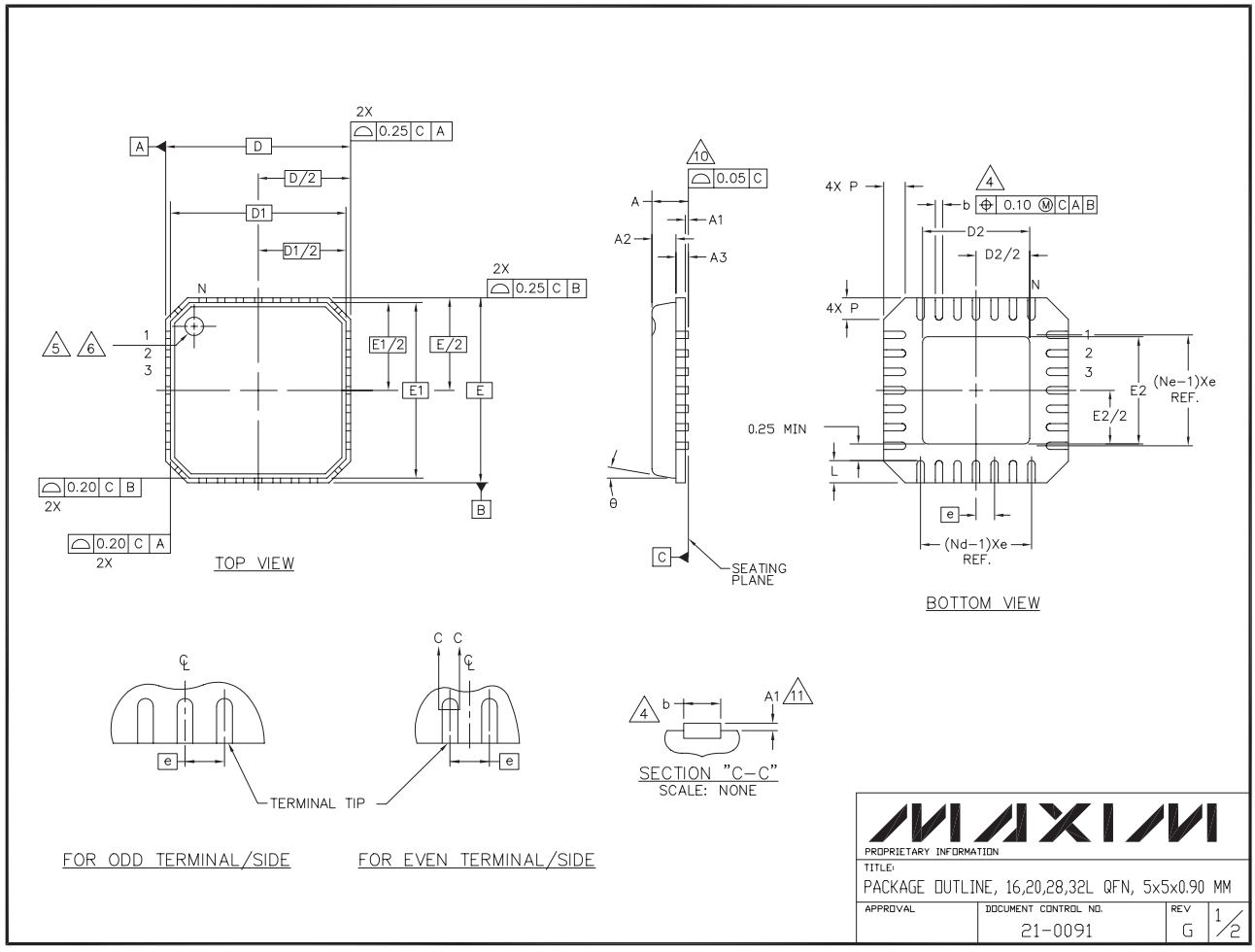
Typical Operating Circuit



Upstream CATV Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2