

LH0081

Z80 PIO Parallel Input/Output Controller

Description

The Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

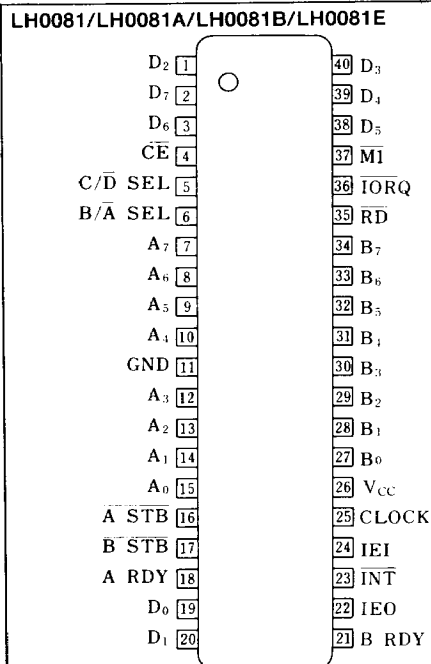
The LH0081 Z80 PIO (Z80 PIO for short below) is a programmable two port device which provides TTL compatible interfacing between peripheral devices and the Z80 CPU. The Z80 CPU configures Z80 PIO to interface with standard peripheral devices such as printers, keyboards, etc.

The LH0081A Z80A and LH0081B Z80B PIO are the high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

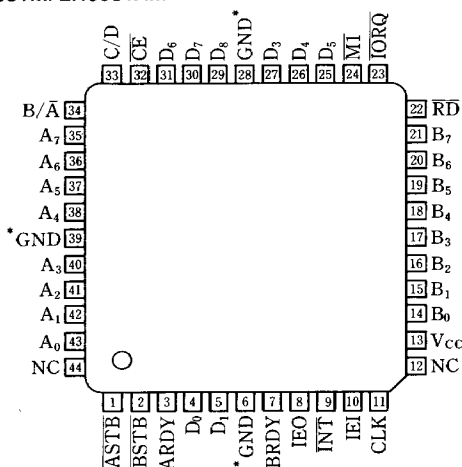
Features

1. Two independent 8-bit bidirectional peripheral interface ports with "handshake" data transfer control
2. N-channel silicon-gate process

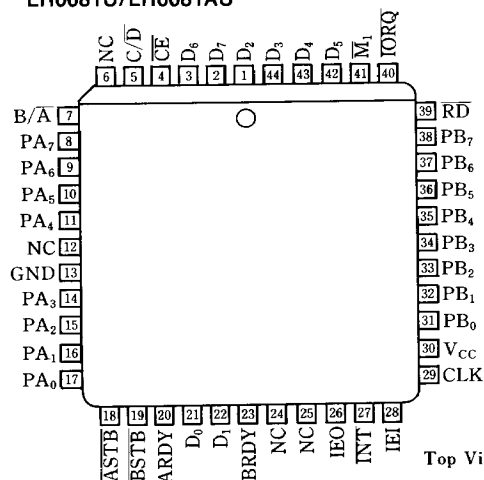
Pin Connections



LH0081M/LH0081AM



LH0081U/LH0081AU



Top View

* The GND pins must be connected to the GND level.

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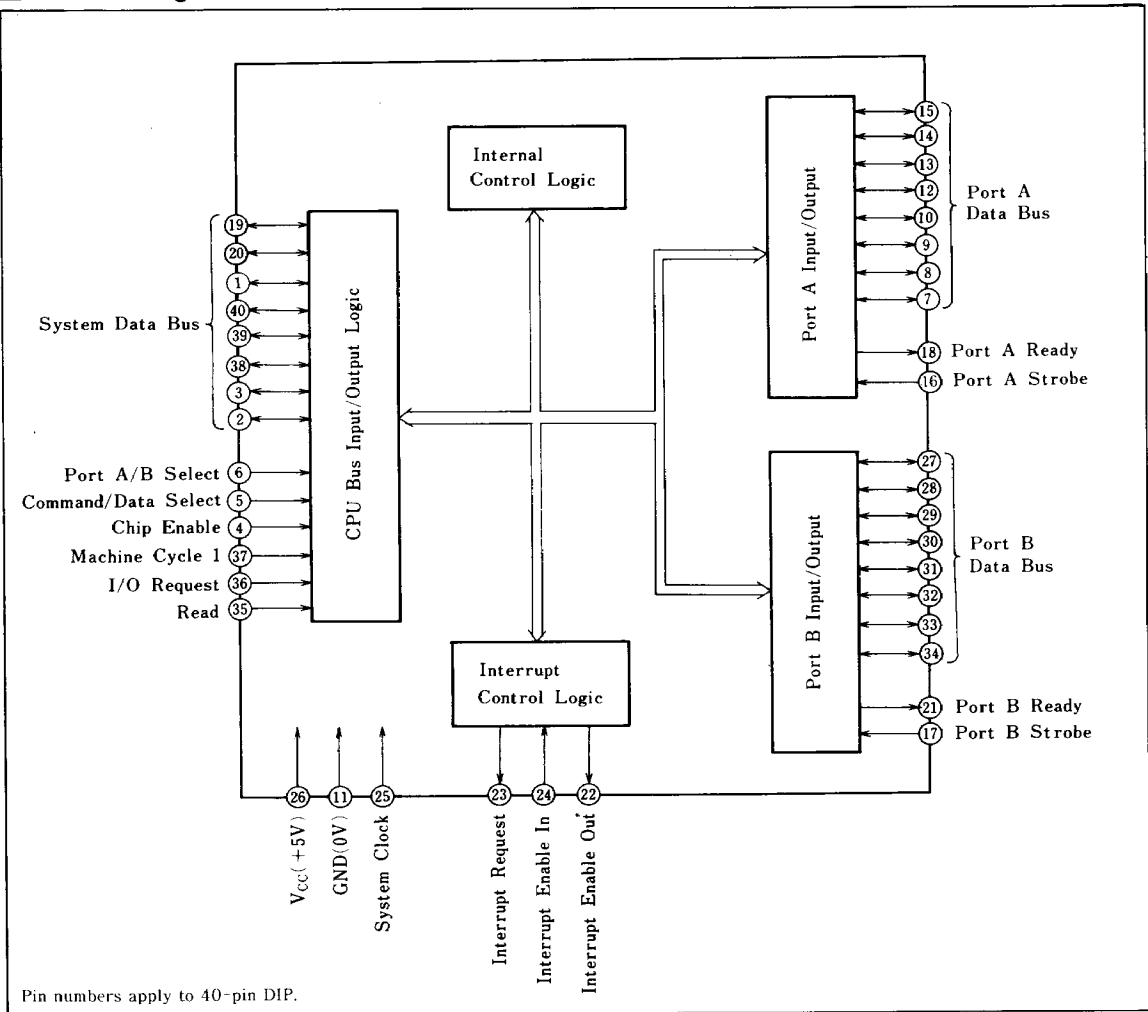
3. Any one of the following four modes of operation may be selected.
 - Byte output mode
 - Byte input mode
 - Byte bidirectional bus (available on Port A only)
 - Bit mode
4. Programmable interrupt
5. Vectored daisy chain priority interrupt logic

6. The port B outputs can drive Darlington transistors
7. All inputs and outputs fully TTL compatible
8. Single +5V power supply and single phase clock
9. 40-pin DIP (DIP40-P-600)
44-pin QFP (QFP44-P-1010A)
44-pin QFJ (QFJ44-P-S650)

Ordering Information

Product	Z80 PIO	Z80A PIO	Z80B PIO	Z80E PIO	Package	Operating temperature
Clock frequency	2.5MHz	4MHz	6MHz	8MHz		
Model No.	LH0081	LH0081A	LH0081B	LH0081E	40-pin DIP	0°C to +70°C
	LH0081M	LH0081AM			40-pin QFP	0°C to +60°C
	LH0081U	LH0081AU	LH0081BU		40-pin QFJ	0°C to +70°C

Block Diagram



Pin Description

Pin	Meaning	I/O	Function
D ₀ -D ₇	Data bus	Bidirectional 3-state	System data bus.
B/ $\overline{A}$ SEL	Port B or A select	I	Defines which port is accessed. A high selects port B, and a low port A.
C/ $\overline{D}$ SEL	Control or data select	I	Defines the type of data transfer on the data bus. A high selects control, and a low data.
$\overline{CE}$	Chip enable	I	Active "Low". A low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	Input/output request	I	Active "Low". Read operation when $\overline{RD}$ is active, and write operation when it is not active. Indicates that the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{RD}$	Read cycle status	I	Active "Low". Read operation when active.
$\overline{IEI}$	Interrupt enable in	I	Active "High". Forms a priority-interrupt daisy-chain.
$\overline{IEO}$	Interrupt enable out	O	Active "High". Forms a priority-interrupt daisy-chain.
$\overline{INT}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
A ₀ -A ₇	Port A bus	Bidirectional 3-state	Transfers information between port A and a peripheral device.
$\overline{A}$ STB	Port A strobe	I	Active "Low". Used as a handshake line for data transfer synchronization on port A. Not used in the bit control mode.
A RDY	Port A ready	O	Active "High". Used as a handshake line for data transfer synchronization on port A. Not used in the bit control mode.
B ₀ -B ₇	Port B bus	Bidirectional 3-state	Transfers information between port B and a peripheral device.
$\overline{B}$ STB	Port B strobe	I	Active "Low". Used as a handshake line for data transfer synchronization on port B. Not used in the bit control mode.
B RDY	Port B ready	O	Active "High". Used as a handshake line for data transfer synchronization on port B. Not used in the bit control mode.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input voltage	V _{IN}	-0.3 to +7.0	V
Output voltage	V _{OUT}	-0.3 to +7.0	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

DC Characteristics

(V_{CC}=5V±5%, T_a=0 to +70°C^{Note 1})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V _{ILC}		-0.3		0.45	V
Clock input high voltage	V _{IHC}		V _{CC} -0.6		V _{CC} +0.3	V
Input low voltage	V _{IL}		-0.3		0.8	V
Input high voltage	V _{IH}		2.0		5.5	V
Output low voltage	V _{OL}	I _{OL} =2mA			0.4	V
Output high voltage	V _{OH}	I _{OH} =-250μA	2.4			V
Supply current	I _{CC}	V _{OH} =1.5V			100	mA
Input leakage current	I _{LI}	0≤V _{IN} ≤V _{CC}			10	μA
3 state output/data bus input leakage current	I _z	0≤V _{IN} ≤V _{CC}			10	μA
Darlington drive current	I _{OHD}	R _{EXT} =390Ω	-1.5			mA

Note 1: T_a=0 to +60°C for 44-pin QFP.

Capacitance

(f=1MHz, T_a=25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C _{CLOCK}	Unmeasured pins returned to ground			12	pF
Input capacitance	C _{IN}				7	pF
Output capacitance	C _{OUT}				10	pF

AC Characteristics

(V_{CC}=5V±5%, T_a=0 to +70°C)

No.	Parameter	Symbol	LH0081		LH0081A		LH0081B		LH0081E		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	Clock Cycle time	T _{cC}	400	(Note 1)	250	(Note 1)	165	(Note 1)	125	(Note 1)	ns	
2	Clock width (high)	T _{wCh}	170	2000	105	2000	65	2000	55	2000	ns	
3	Clock width (low)	T _{wCl}	170	2000	105	2000	65	2000	55	2000	ns	
4	Clock fall time	T _{fC}		30		30		20		10	ns	
5	Clock rise time	T _{rC}		30		30		20		10	ns	
6	CE, B/A, C/D to RD, IORQ ↓ Setup time	T _{sCS} (RI)	50		50		50		50		ns	6
7	Any hold times for specified setup time	T _h	0		0		0		0		ns	
8	RD, IORQ to clock ↑ setup time	T _{sRI} (C)	115		115		70		60		ns	
9	RD, IORQ ↓ to deta out delay	T _{dRI} (DO)		430		380		300		210	ns	2
10	RD, IORQ ↑ to deta out float delay	T _{dRI} (DOs)		160		110		70		60	ns	
11	Data in to clock ↑ setup time	T _{sRI} (C)	50		50		40		30		ns	C _L =50pF
12	IORQ ↓ to vector out delay (INTACK cycle)	T _{dIO} (DOI)	340		160		120		90		ns	3
13	MI ↓ to clock ↑ setup time	T _{sMI} (Cr)	210		90		70		55		ns	
14	MI ↑ to clock ↓ setup time (MI cycle)	T _{sMI} (Cf)	0		0		0		0		ns	8
15	MI ↓ to IEO ↓ delay (interrupt immediately preceding MI ↓)	T _{dMI} (IEO)		300		190		100		85	ns	5, 7
16	IEI to IORQ ↓ setup time (INTACK cycle)	T _{sIEI} (IO)	140		140		100		100		ns	7
17	IEI ↓ to IEO ↓ delay	T _{dIEI} (IEOf)		190		130		120		110	ns	5 C _L =50pF
18	IEI ↑ to IEO ↑ delay (After ED decode)	T _{dIEI} (IEOr)		210		160		160		150	ns	5

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No.	Parameter	Symbol	LH0081		LH0081A		LH0081B		LH0081E		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
19	IORQ ↑ to clock ↓ setup time (to activate READY to next clock cycle)	TcIO (C)	220		200		170		160		ns	
20	Clock ↓ to READY ↑ delay	TdC (RDYr)	200		190		170		160		ns	5 C _L = 50pF
21	Clock ↓ to READY ↓ delay	TdC (RDYf)	150		140		120		110		ns	5
22	STROBE pulse width	TwSTB	150		150		120		100		ns	4
23	STROBE ↑ to clock ↓ setup time (to activate READY on next clock cycle)	TsSTB (C)	220		220		150		130		ns	5
24	IORQ ↑ to PORT DATA stable delay (Mode 0)	TdIO (PD)		200		180		160		150	ns	5
25	PORT DATA to STROBE ↑ setup time (mode 1)	TsPD (STB)	260		230		190		170		ns	
26	STROBE ↓ to PORT DATA stable (mode 2)	TdSTB (PD)		230		210		180		160	ns	5
27	STROBE ↑ to PORT DATA float delay (mode 2)	TdSTB (PDr)		200		180		160		140	ns	C _L = 50pF
28	PORT DATA match to INT ↓ delay (mode 3)	TdPD (INT)		540		490		430		380	ns	
29	STROBE ↑ to INT ↓ delay	TdSTB (INT)		490		440		350		300	ns	

↑ Rising edge, ↓ Falling edge

Ta = 0 to +60°C for 44-pin QFP.

Note 1: TcC = TwCh + TwCl + TrC + TfC.

Note 2: Increase TdRI (DO) by 10 ns for each 50 pF increase in load up to 200 pF max.

Note 3: Increase TdIO (DOI) by 10 ns for each 50 pF, increase in load up to 200 pF max.

Note 4: For Mode 2 : TwSTB > TsPD (STB).

Note 5: Increase these values by 2 ns for each 10 pF increase in load up to 100 pF max.

Note 6: TsCS (RI) may be reduced. However, the time subtracted from TsCS (RI) will be added to TdRI (DO).

Note 7: $2.5 TcC > (N-2) TdIEI (IEO) + TdM1 (IEO) + TsIEI (IO) + TTL$ buffer delay, if any.

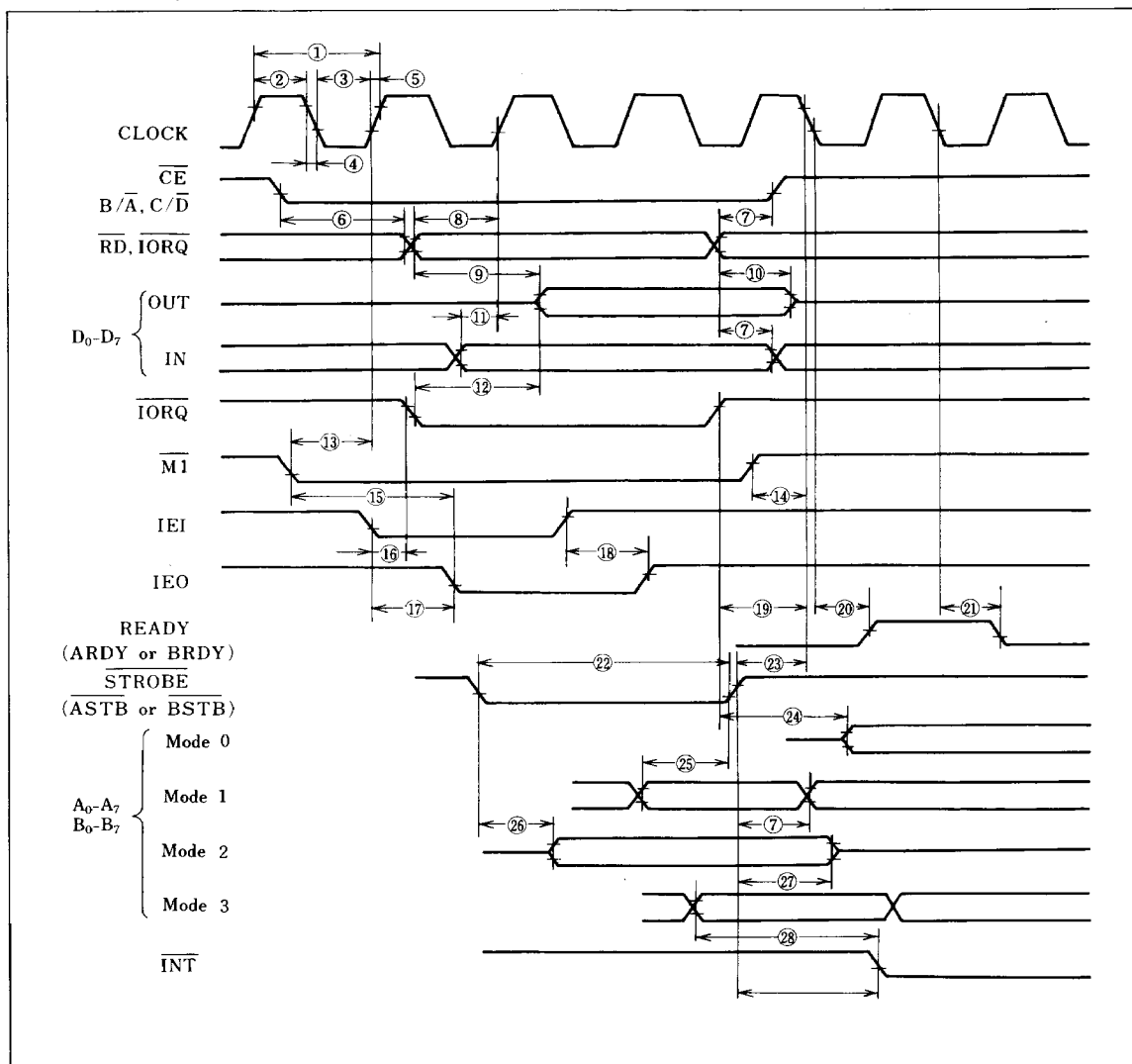
Note 8: M1 must be active for a minimum of two clock cycles to reset the PIO.

Note 9: Z80B PIO numbers are preliminary and subject to change.



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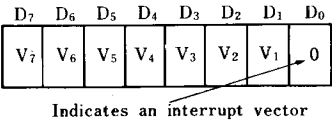
AC Timing Chart



■ Programming

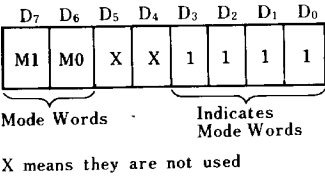
(1) Interrupt vector read

An interrupting device needs giving an 8-bit interrupt vector to the CPU. Using this vector, the CPU forms an interrupt service routine address.



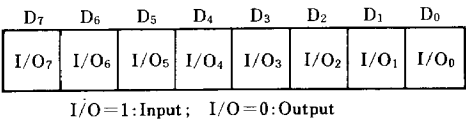
(2) Operation mode select

An operation mode is selected by writing data to the 2-bit mode control register in the following manner.



Mode	M1	M0
Byte output mode	0	0
Byte input mode	0	1
Bidirectional byte bus mode	1	0
Bit control mode	1	1

In selecting the bit control mode, an input/output direction should be set later.



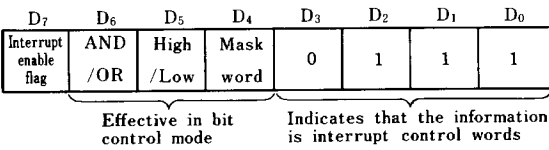
■ Timing

(1) Output mode (Mode 0)

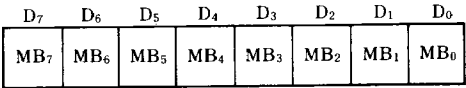
An output cycle is always started by the execution of an output instruction by the CPU. The WR* pulse from the CPU latches the data from the CPU data bus into the selected port's output register. The WR* pulse sets the Ready flag after a Low-going edge of CLK, indicating data is available.

(3) Interrupt control

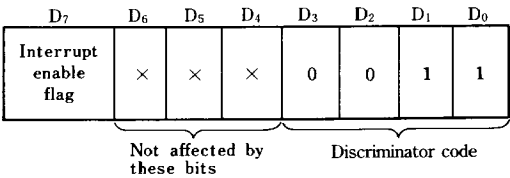
The interrupt control words are as follows.

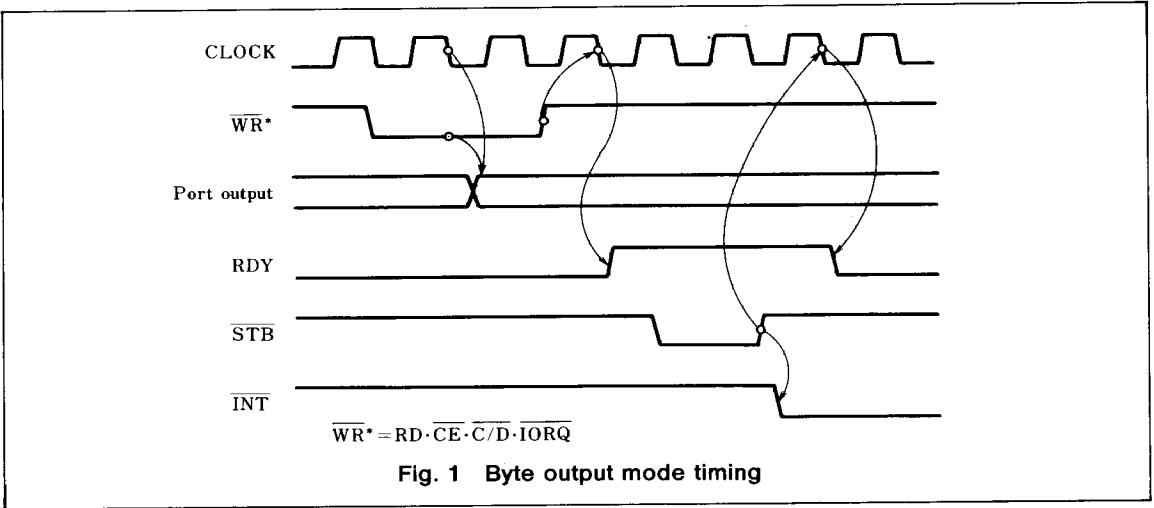


- Bit7=1: Interrupt enable flag is set to enable an interrupt.
 - Bit7=0: Interrupt enable flag is reset to disable an interrupt.
 - Bit6 to 4: Defines interrupt conditions in the bit mode. Ignored in other modes.
 - Bit3 to 0: Indicates interrupt control words.
- If bit4=1, the following control words are supposed to be written in the mask register.



Only the port data line with MB=0 is monitored. When the interrupt conditions are satisfied, an interrupt takes place.

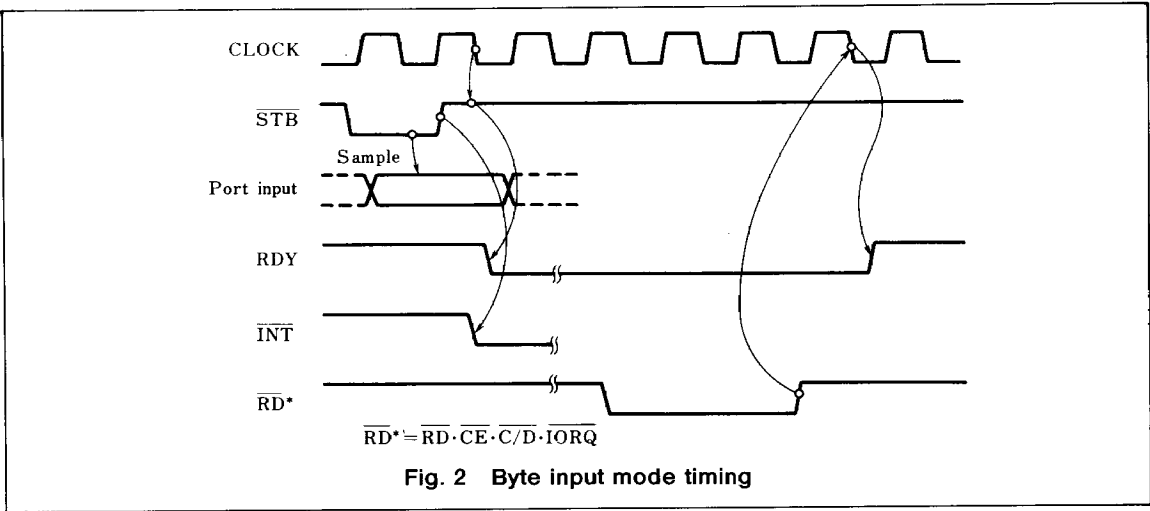




(2) Input mode (Mode 1)

When $\overline{STROBE}$ goes Low, data is loaded into the selected port input register. The next rising edge of strobe activates $\overline{INT}$, if Interrupt Enable is set and this is the highest-priority requesting device. The following falling edge of CLK resets Ready to an inactive state, indicating that the input register is full

and cannot accept any more data until the CPU completes a read. When a read is complete, the positive edge of RD sets Ready at the next Low-going transition of CLK. At this time new data can be loaded into the PIO.



(3) Bidirectional mode (Mode 2)

This is a combination of Modes 0 and 1 using all four handshake lines and the eight Port A I/O lines. Port B must be set to the bit mode and its inputs must be masked. The Port A handshake lines are used for output control and the Port B lines are used for input control. If interrupts occur,

Port A's vector will be used during port output and Port B's will be used during port input. Data is allowed out onto the Port A bus only when $\overline{ASTB}$ is Low. The rising edge of this strobe can be used to latch the data into the peripheral.

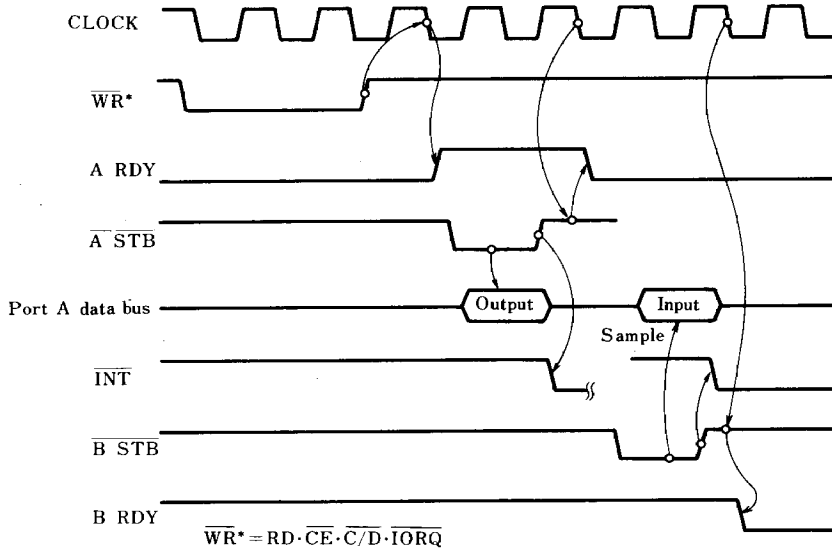


Fig. 3 Byte bidirectional bus mode timing

(4) Bit mode (Mode 3)

The bit mode does not utilize the handshake signals, and a normal port write or port read can be executed at any time. When writing, the data is latched into the output registers with the same timing as the output mode.

When reading the PIO, the data returned to the CPU is composed of output register data from those port data lines assigned as outputs and input regis-

ter data from those port data lines assigned as inputs. The input register contains data that was present immediately prior to the falling edge of $\overline{RD}$. An interrupt is generated if interrupts from the port are enabled and the data on the port data lines satisfy the logical equation defined by the 8-bit mask and 2-bit mask control registers. However, if Port A is programmed in bidirectional mode, Port B does not issue an interrupt in bit mode and must therefore be polled.

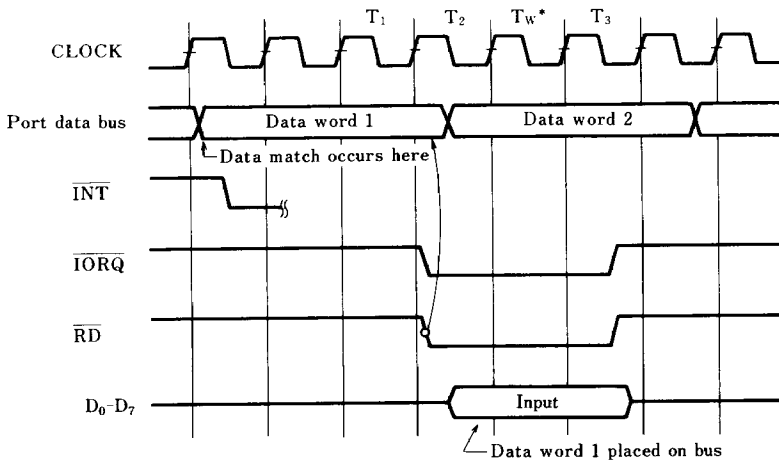


Fig. 4 Bit mode timing

(5) Interrupt acknowledge timing

During $\overline{MI}$ time, peripheral controllers are inhibited from changing their interrupt enable status, permitting the Interrupt Enable signal to ripple through the daisy chain. The peripheral with IEI High and IEO Low during $\overline{INTACK}$ places a pre-

programmed 8-bit interrupt vector on the data bus at this time. IEO is held Low until a Return From Interrupt (RETI) instruction is executed by the CPU while IEI is High. The 2-byte RETI instruction is decoded internally by the PIO for this purpose.

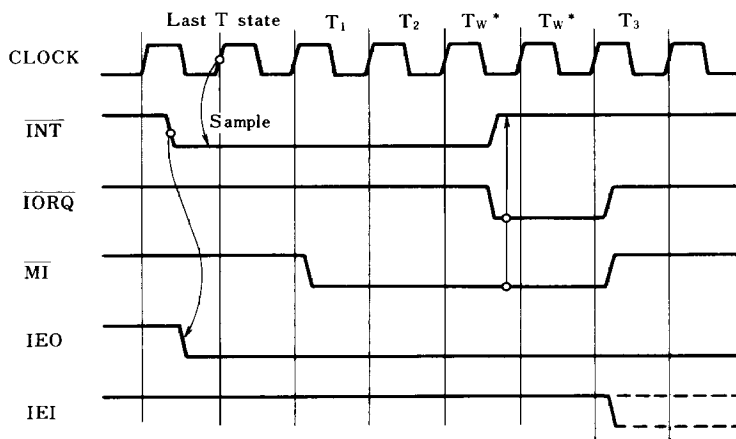


Fig. 5 Interrupt acknowledge timing

(6) Return from interrupt cycle

If a Z-80 peripheral has no interrupt pending and is not under service, then its IEO=IEI. If it has an interrupt under service (i.e., it has already interrupted and received an interrupt acknowledge) then its IEO is always Low, inhibiting lower priority devices from interrupting. If it has an interrupt pending which has not yet been acknowledged, IEO is Low unless an "ED" is decoded as the first byte of a 2-byte opcode. In this case, IEO goes High until the next opcode byte is decoded, whereupon it

goes Low again. If the second byte of the opcode was a "4D", then the opcode was an RETI instruction.

After an "ED" opcode is decoded, only the peripheral device which has interrupted and is currently under service has its IEI High and its IEO Low. This device is the highest-priority device in the daisy chain that has received an interrupt acknowledge. All other peripherals have IEI = IEO. If the next opcode byte decoded is "4D", this peripheral device resets its "interrupt under service" condition.

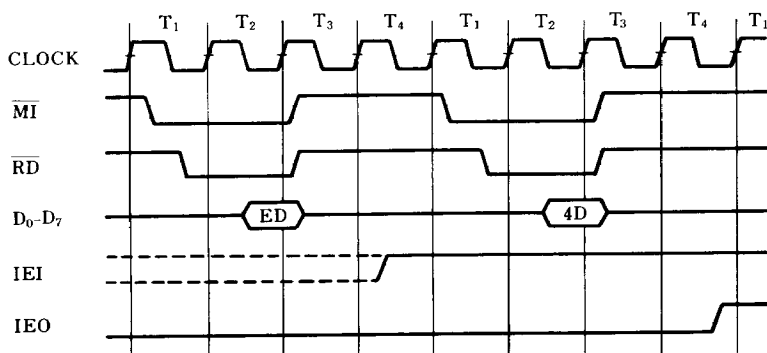


Fig. 6 Return from interrupt cycle timing

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