LH0084/LH0085 LH0086/LH0087

Z80 SIO Serial Input/Output Controller

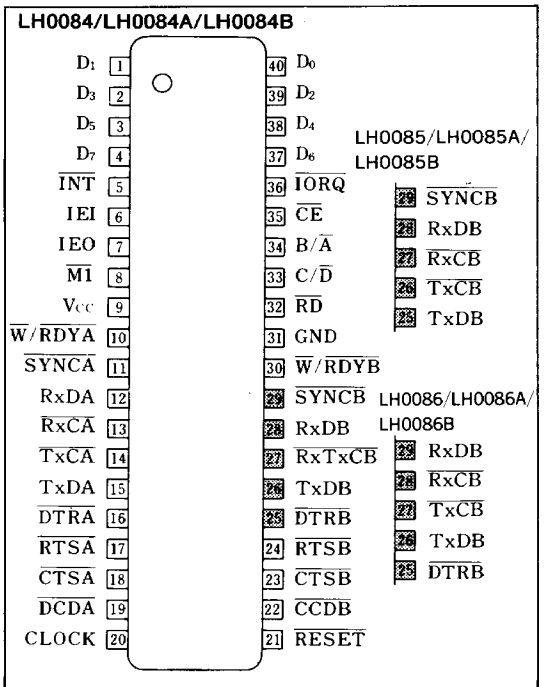
■ Description

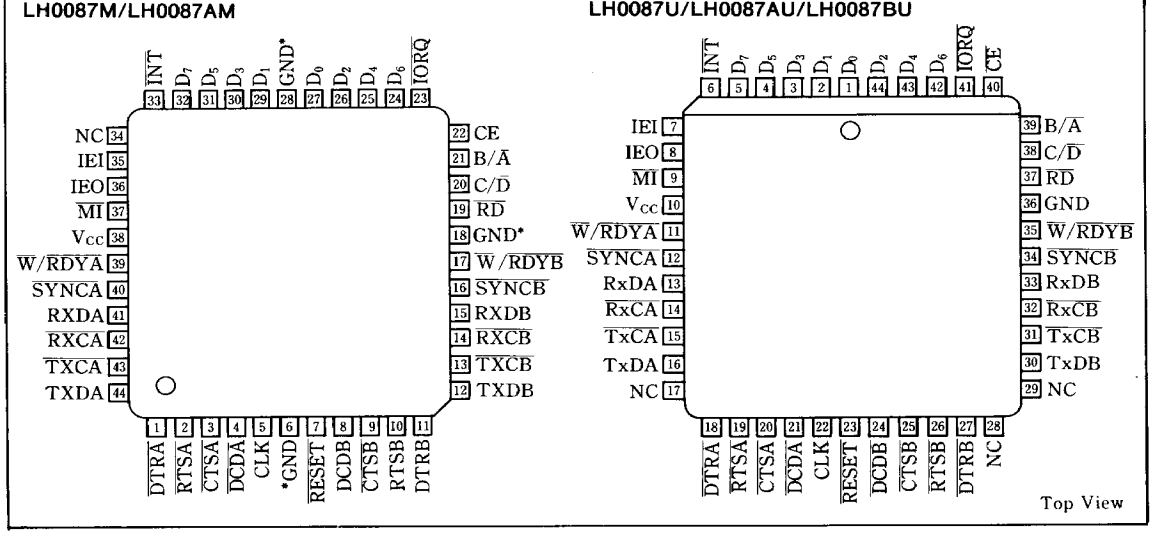
The LH0084/85/86/87, Z80 SIO (Z80 SIO for short below) is a dual-channel multi-function peripheral component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but—within that role—it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

The Z80 SIO is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications (cassette or floppy disk interfaces, for example).

The Z80 SIO can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for

■ Pin Connections





*The GND pins must be connected to the GND level.

general-purpose I/O.

The Z80 SIO has six types as below according it's system clock and bonding option. The Z80A SIO and the Z80B SIO are a high speed version which can operate at the 4MHz and 6MHz system clock, respectively.

- LH0084 Z80 SIO/0
- LH0085 Z80 SIO/1
- LH0086 Z80 SIO/2
- LH0087 Z80 SIO
- LH0084A Z80A SIO/0
- LH0085A Z80A SIO/1
- LH0086A Z80A SIO/2
- LH0087A Z80A SIO
- LH0084B Z80B SIO/0
- LH0085B Z80B SIO/1
- LH0086B Z80B SIO/2
- LH0087B Z80B SIO

Features

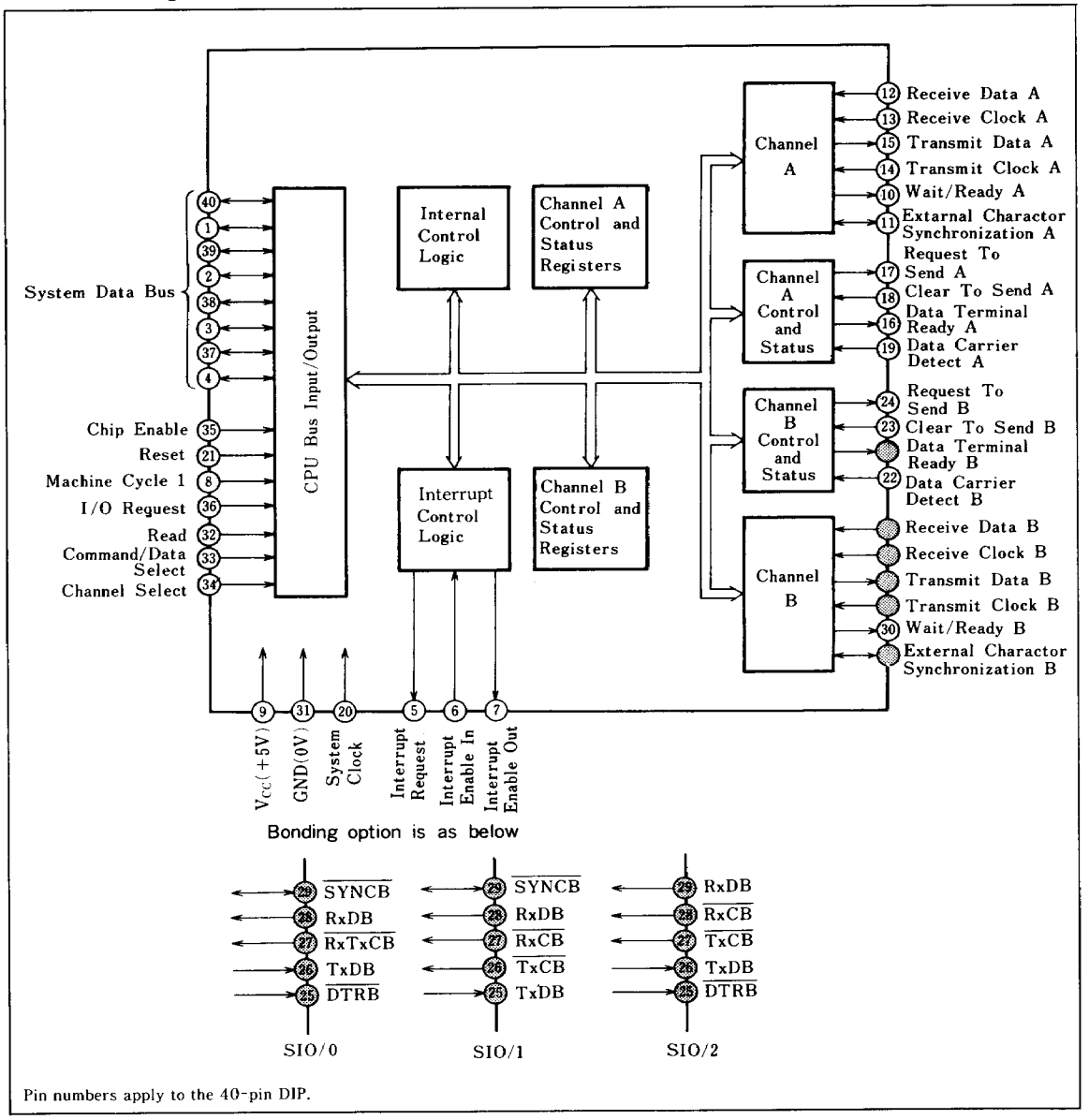
1. N-channel silicon-gate process
2. Single +5V power supply and single phase clock
3. Two independent full duplex channels
4. Data rates : 0.to 500K bits/second (at 2.5 MHz system clock)
   : 0 to 800K bits/second (at 4MHz system clock)
   : 0 to 1200K bits/second (at 6MHz system clock)
5. Asynchronous operation
   - 5, 6, 7 or 8 bits/character
   - 1, 1½ or 2 stop bits/character
   - Even, odd or no parity
   - ×1, ×16, ×32 and ×64 clock modes
   - Break generation and detection
   - Parity, Overrun and Framing error detection
6. Binary synchronous operation
   - Internal or external character synchronization
   - One or two Sync characters in separate registers
   - Automatic Sync character insertion
   - CRC generation and checking
7. HDLC or IBM SDLC operation
   - Abort sequence generation and detection
   - Automatic zero insertion and detection
   - Automatic flag insertion
   - Address field recognition
   - I-field residue handling
   - Valid receive messages protected from overrun
   - CRC generation and checking
8. Vectored daisy chain priority interrupt logic
9. CRC-16 or CRC-CCITT block check
10. Separate modem control inputs and outputs for both channels
11. Modem status can be monitored
12. 40-pin DIP (DIP40-P-600)
    44-pin QFP (QFP44-P-1010A)
    44-pin QFJ (QFJ44-P-S650)

Ordering Information

Product	Z80 SIO	Z80A SIO	Z80B SIO	Package	Operating temperature
Clock frequency	2.5MHz	4MHz	6MHz		
Model No.	LH008X	LH008XA	LH008XB	40-pin DIP	0°C to +70°C
	LH008XH	LH008XAH			−20°C to+85°C
	LH0087M	LH0087AM		44-pin QFP	0°C to +60°C
	LH0087U	LH0087AU	LH0087BU	44-pin QFJ	0°C to+70°C

X: It is the bonding option to select one of SIO/0, SIO/1 and SIO/2 on 40-pin DIP.
X=4: SIO/0
X=5: SIO/1
X=6: SIO/2
H: H affix indicates a wide temperature spec, packaged in 40-pin DIP.

Block Diagram



Pin numbers apply to the 40-pin DIP.

■ Pin Description

Pin	Meaning	I/O	Function
D_0-D_7	Data bus	Bidirectional 3-state	System data bus
B/$\overline{A}$	Channel A or B select	I	Defines which channel is accessed. Channel B at "High", channel A at "Low".
C/$\overline{D}$	Control or data select	I	Defines the type of information transfer on the data bus. Control word at "High", data at "Low".
$\overline{CE}$	Chip enable	I	Active "Low". A Low enables the CPU to transmit and receive control words and data.
CLOCK	System clock	I	Standard Z80 system clock used for internal synchronization signals.
$\overline{M1}$	Machine cycle one	I	Active "Low". Indicates that the CPU is acknowledging an interrupt, when both $\overline{M1}$ and $\overline{IORQ}$ are active.
$\overline{IORQ}$	Input/output request	I	Active "Low". Read operation when $\overline{RD}$ is active, and write operation when it is not active. Indicates that the CPU is acknowledging an interrupt, when both $\overline{IORQ}$ and $\overline{M1}$ are active.
$\overline{RD}$	Read cycle status	I	Active "Low". Read operation when active.
$\overline{RESET}$	Reset	I	Active "Low". Resets the interrupt bits.
IEI	Interrupt enable in	I	Active "High". Used to form a priority-interrupt daisy chain.
IEO	Interrupt enable out	O	Active "High" Used to form a priority-interrupt daisy chain.
$\overline{INT}$	Interrupt request	Open drain, O	Active "Low". Active when requesting an interrupt.
$\overline{W/RDYA}$ $\overline{W/RDYB}$	Wait/ready	Open drain, O	Active "Low". READY when the DMA is a bus master, $\overline{WAIT}$ when the CPU is a bus master.
$\overline{CTSA}$, $\overline{CTSB}$	Clear to send	I	Active "Low". Enables the respective transmitters. Also applicable as general-purpose input pins.
$\overline{DCDA}$, $\overline{DCDB}$	Data carrier detect	I	Active "Low". Enables the respective receivers. Also applicable as general-purpose input pins.
RxDA, RxDB	Receive data	I	Active "Low". Data line for receiving
TxDA, TxDB	Transmit data	O	Active "Low". Data line for transmitting.
$\overline{RxCA}$, $\overline{RxCB}$	Receiver clock	I	Active "Low". Receiving synchronization clock.
$\overline{TxCA}$, $\overline{TxCB}$	Transmitter clock	I	Active "Low". Transmitting synchronization clock.
$\overline{RTSA}$, $\overline{RTSB}$	Request to send	O	Active "Low". Indicates that the transmitter is empty during transfer. Also applicable as general-purpose output pins.
$\overline{DTRA}$, $\overline{DTRB}$	Data terminal ready	O	Active "Low". Also applicable as general-purpose output pins.
$\overline{SYNCA}$, $\overline{SYNCB}$	External character synchronization	I	Active "Low". Acts the same way as $\overline{CTS}$ and $\overline{DCD}$ in the asynchronous mode. Driven "Low" in the synchronous mode when a synchronizing pattern is achieved.

■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Input voltage	V_{IN}	−0.3 to +7.0	V	
Output voltage	V_{OUT}	−0.3 to +7.0	V	
Operating temperature	Topr	0 to +70	℃	1
		0 to +60		2
		−20 to +85		3
Storage temperature	Tstg	−65 to +150	℃	

Note 1: Specified for 40-pin DIP and 44-pin QFJ
Note 2: Specified for 44-pin QFP
Note 3: Specified for wide temperature type

■ DC Characteristics

(V_{CC}=5V±5%, Ta=0 to +70℃ Note 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input low voltage	V_{ILC}		−0.3		0.45	V
Clock input high voltage	V_{IEC}		Vcc−0.6		5.5	V
Input low voltage	V_{IL}		−0.3		0.8	V
Input high voltage	V_{IH}		2.0		5.5	V
Output low voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=−250 μA	2.4			V
Input leakage current	$\lvert I_{LI} \rvert$	$0<V_{IN}<V_{CC}$			10	μA
3-state output/data bus input leakage curreut	$\lvert I_Z \rvert$	$0<V_{IN}<V_{CC}$			10	μA
$\overline{SYNC}$ pin leakage current	$I_{L(SY)}$	$0<V_{IN}<V_{CC}$	−40		10	μA
Current consumption	I_{CC}				100	mA

Note 1: Ta=0 to +60℃ for 44-pin QFP, Ta=−20 to +85℃ for wide temperature types.

■ Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock capacitance	C_{CLOCK}	Unmeasured pins returned to ground			40	pF
Input capacitance	C_{IN}				5	pF
Output capacitance	C_{OUT}				10	pF

■ AC Characteristics

(1) AC characteristics (I)

(V_{CC}=5V±5%, Ta=0 to +70℃ Note 1)

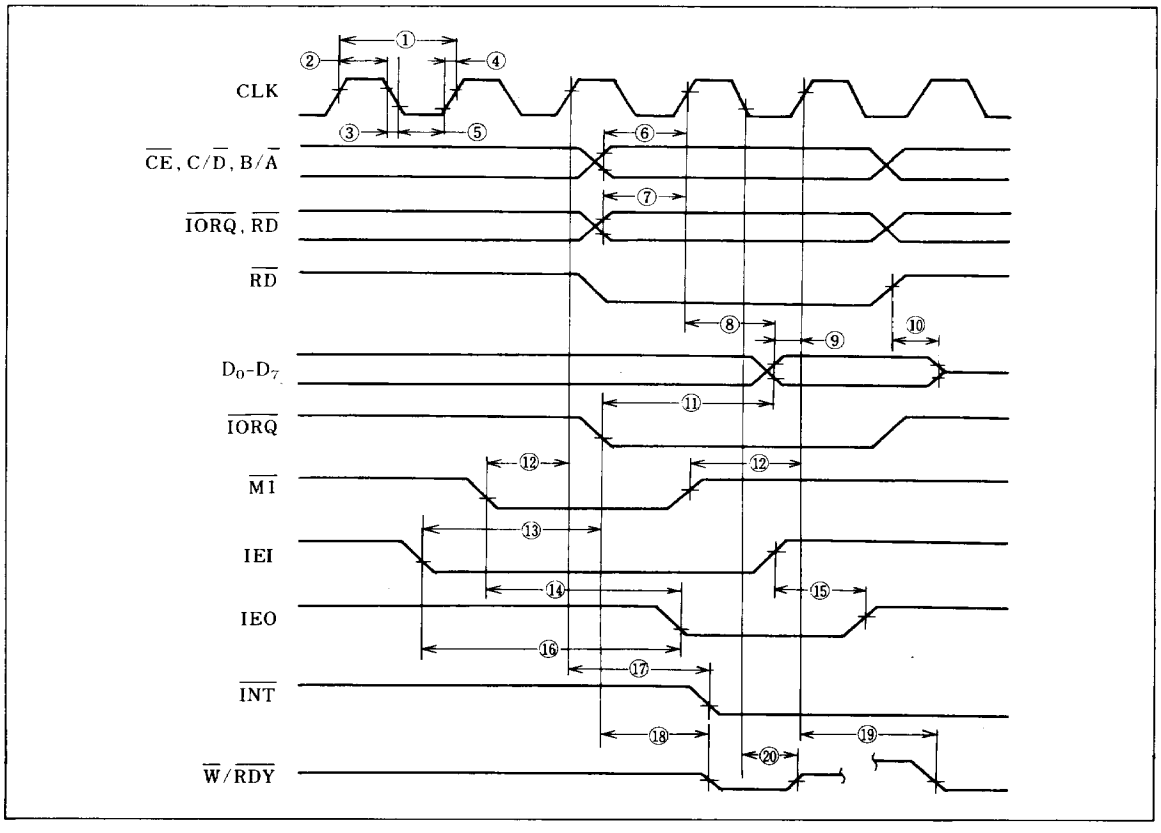
No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Clock cycle time	TcC	400	4000	250	4000	165	4000	ns
2	Clock high width	TwCh	170	2000	105	2000	70	2000	ns
3	Clock fall time	TfC		30		30		15	ns
4	Clock rise time	TrC		30		30		15	ns
5	Clock low width	TwCl	170	2000	105	2000	70	2000	ns
6	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to clock ↑ setup time	TsAD(C)	160		145		60		ns
7	$\overline{IORQ}$, $\overline{RD}$ to clock ↑ setup time	TsCS(C)	240		115		60		ns
8	Clock ↑ to data out delay	TdC(DO)		240		220		150	ns
9	Data in to clock ↑ setup (Write or $\overline{M1}$ cycle)	TsDI(C)	50		50		30		ns
10	$\overline{RD}$ ↑ to data out float delay	TdRD(DOz)		230		110		90	ns
11	$\overline{IORQ}$ ↓ to data out delay (INTACK cycle)	TdIO(DOI)		340		160		100	ns

No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
12	$\overline{M1}$ to clock ↑ setup time	TsM1(C)	210		90		75		ns
13	IEI to $\overline{IORQ}$ ↓ setup time (INTACK cycle)	TsIEI(IO)	200		140		120		ns
14	$\overline{M1}$ ↓ to IEO ↓ delay (interrupt before $\overline{M1}$)	TdM1(IEO)		300		190		160	ns
15	IEI ↑ to IEO ↑ delay (after ED decode)	TdIEI(IEOr)		150		100		70	ns
16	IEI ↓ to $\overline{INT}$ ↓ delay	TdIEI(IEOf)		150		100		70	ns
17	Clock ↑ to $\overline{INT}$ ↓ delay	TdC(INT)		200		200		150	ns
18	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to$\overline{W}/\overline{RDY}$ ↓ delay (wait mode)	TdIO(W/RWf)		300		210		175	ns
19	Clock ↑ to $\overline{W}/\overline{RDY}$ ↓ delay (ready mode)	TdC(W/PR)		120		120		100	ns
20	Clock ↓ to $\overline{W}/\overline{RDY}$ float delay (wait mode)	TdC(W/RWz)		150		130		110	ns
21	Any unspecified hold when setup is specified	Th	0		0		0		ns

↑ Rising edge, ↓ Falling edge.

Note 1: Ta=0 to +60℃ for 44-pin QFP
Ta=−20 to +85℃ for wide temperature types

(2) AC timing chart (I)



(3) AC characteristics (Ⅱ)

(V_{CC}=5V±5%, Ta=0 to +70℃ Note 1)

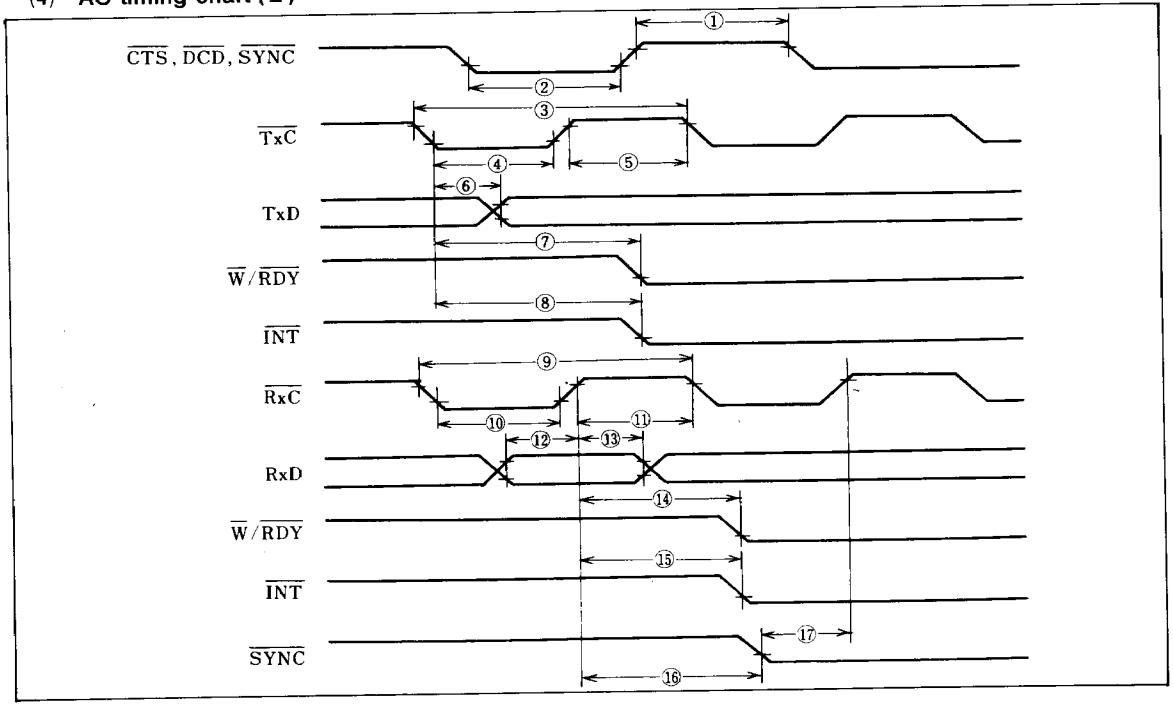
No.	Parameter	Symbol	LH0084/5/6/7		LH0084A/5A/6A/7A		LH0084B/5B/6B/7B		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	Pulse high width	TwPh	200		200		200		ns
2	Pulse low width	TwPl	200		200		200		ns
3	$\overline{TxC}$ clock time	TcTxC	400	∞	400	∞	330	∞	ns
4	$\overline{TxC}$ low width	TwTxCl	180	∞	180	∞	100	∞	ns
5	$\overline{TxC}$ high width	TwTxCh	180	∞	180	∞	100	∞	ns
6	$\overline{TxC}$ ↓ to TxD delay (x1 mode)	TdTxC(TxD)		400		300		220	ns
7	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ delay (ready mode)	TdTxC(W/RRf)	5	9	5	9	5	9	Clock period
8	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ delay	TdTxC(INT)	5	9	5	9	5	9	Clock period
9	$\overline{RxC}$ cycle time	TdRxC	400	∞	400	∞	330	∞	ns
10	$\overline{RxC}$ low width	TwRxCl	180	∞	180	∞	100	∞	ns
11	$\overline{RxC}$ high width	TwRxCh	180	∞	180	∞	100	∞	ns
12	RxD to $\overline{RxC}$ ↑ setup time (x1 mode)	TsRxD(RxC)	0		0		0		ns
13	$\overline{RxC}$ ↑ to RxD hold time (x1 mode)	ThRxD(RxC)	140		140		100		ns
14	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ delay (ready mode)	TdRxC(W/RRf)	10	13	10	13	10	13	Clock period
15	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ delay	TdRxC(INT)	10	13	10	13	10	13	Clock period
16	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ delay (output modes)	TdRxC(SYNC)	4	7	4	7	4	7	Clock period
17	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↓ setup (external sync modes)	TsSYNC(RxC)	−100		−100		100		ns

↑ Rising edge, ↓ Falling edge

Note 1: Ta=0 to +60℃ for 44-pin QFP
Ta=−20 to +85℃ for wide temperature types

Note 2: In all mode, the System Clock rate must be at least five times the maximum data rate.

(4) AC timing chart (Ⅱ)



■ Transmit and Receive Data Path

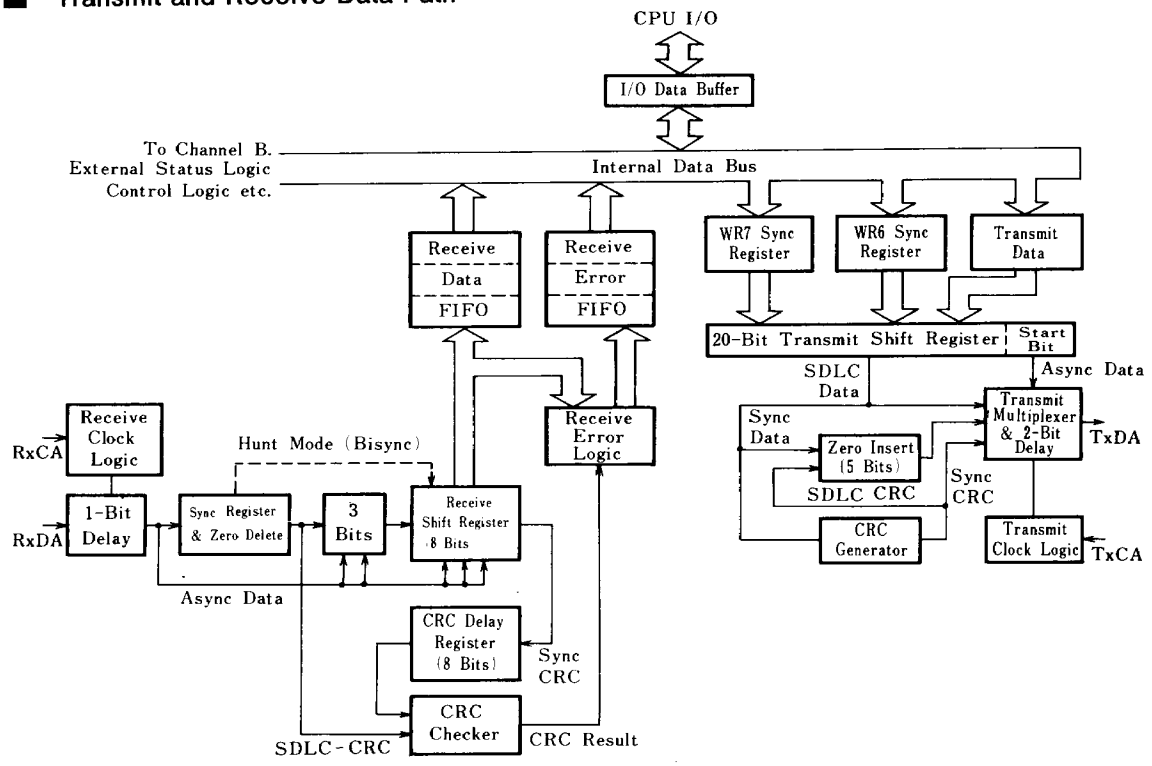


Fig. 1 Transmit and receive data path

■ Programming

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected mode.

Both channels contain registers that must be programmed via the system program prior to operation.

(1) Read Registers

The SIO contains three read registers for Channel B and three read registers for Channel A (RR0-RR2) that can be read to obtain the status information. The status information includes error conditions, interrupt vector and standard communications-interface signals

● **Read Register 0 (RR 0)**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Break /abort	Tx under-run /EOM	CTS	Sync /hunt	DCD	Tx buffer empty	INT pending (ch.A only)	Rx character available

● **Read Register 1 (RR 1)**

The RR1 contains the status bits for specific receiving coditions as well as the one-field fraction codes for the SDLC receive mode.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
End of frame	CRC/ framing error	Rx overrun error	Parity error	Fraction code 2	Fraction code 1	Fraction code 0	All sent

● **Read Register 2 (RR 2)**

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

Valiable if "status affects vector" is programmed

(2) Write Registers

The SIO contains eight write registers for Channel B and eight write registers for Channel A (WR0-WR7) that are programmed separately to configure the functional personality of the channels.

● Write Register 0 (WR 0)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CRC reset code 1	CRC reset code 0	Command bit 2	Command bit 1	Command bit 0	Pointer bit 2	Pointer bit 1	Pointer bit 0
		Control words			Register pointers		

● Write Register 1 (WR 1)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Wait ready enable	Wait/ ready function	Wait/ ready on R/$\overline{T}$	Receive inter- rupt mode 1	Receive inter- rupt mode 0	Status affects vector	Tx INT enable	Ext INT enable

● Write Register 2 (WR 2)

The WR2 contains the interrupt vector for both channels and is only in the Channel B. When the status affected vector (WR1, D_2) is 1, the vector from the SIO during the interrupt acknowledge cycle varies (V_3 - V_1) depending on the interrupt conditions. The WR2 contents do not vary then.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

● Write Register 3 (WR 3)

The WR 3 contains the bits and parameters to control the receivers.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Rx bits char- acter 1	Rx bits char- acter 0	Auto enable	Enter hunt phase	Rx CRC enable	Address search mode	Sync charac- ter load inhibit	Rx enable

● Write Register 4 (WR 4)

The WR4 has the bits control both receivers and transmitters.

In initializing for transmitting and receiving, these bits must be set up before the WR1, WR3, WR5, WR6, and WR7.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Clock rate 1	Clock rate 0	Sync mode 1	Sync mode 0	Stop bit 1	Stop bit 0	Parity Even /$\overline{ODD}$	Parity enable

● Write Register 5 (WR 5)

The WR5 contains the bits (except for D_2) to control the transmitters.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DTR	Tx bits /char- acter 1	Tx bits /char- acter 0	Send break	Tx enable	CRC16 /$\overline{SDLC}$	RTS	Tx CRC enable

● Write Register 6 (WR 6)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SYNC 7	SYNC 6	SYNC 5	SYNC 4	SYNC 3	SYNC 2	SYNC 1	SYNC 0

● Write Register 7 (WR 7)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SYNC 15	SYNC 14	SYNC 13	SYNC 12	SYNC 11	SYNC 10	SYNC 9	SYNC 8

■ Timing

(1) Read cycle

The timing signals generated by a Z-80 CPU input instruction to read a data or status byte from the SIO are illustrated in Fig. 2.

(2) Write cycle

Fig. 3 illustrates the timing and data signals generated by a Z-80 CPU output instruction to write a data or control byte into the SIO.

(3) Interrupt cycle

The interrupt-acknowledging and return-from-interrupt cycles are of the same timing as for other Z80 peripherals. (Refer to the Z80 PIO.)

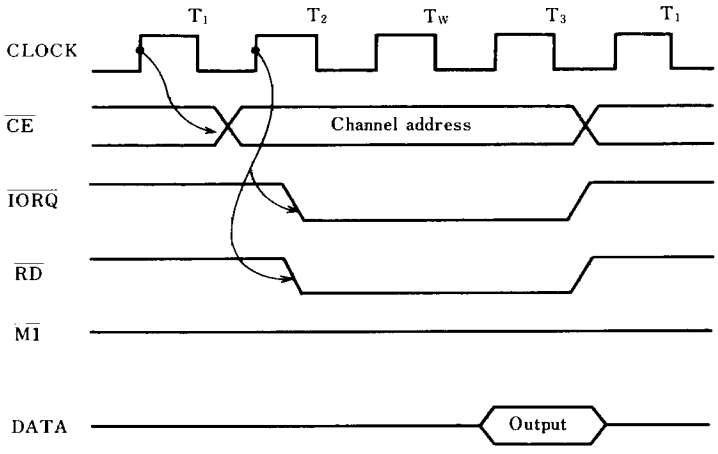


Fig. 2 Read cycle timing

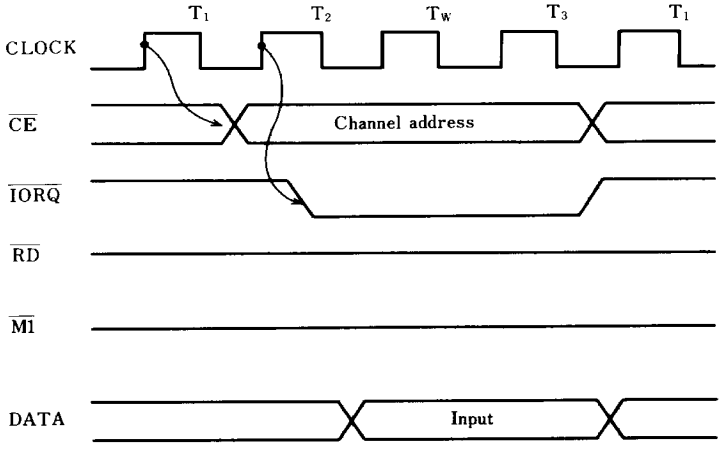


Fig. 3 Write cycle timing