National Semiconductor

LH0132, LH0132C
Ultra-Fast FET-Input Operational Amplifier

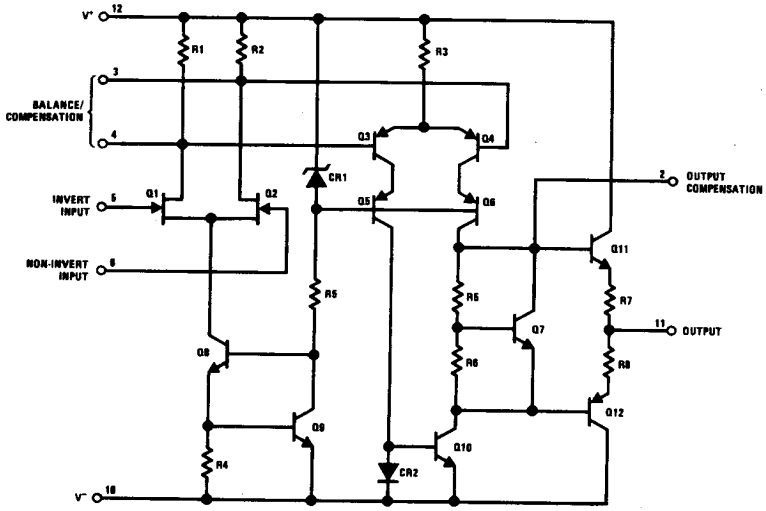
General Description

The LH0132 is a high slew rate, high input impedance differential amplifier. It was developed specifically for sample and hold and other fast signal handling applications which require very low input currents over the full input voltage range. Input offset and bias currents are guaranteed over a full input common mode range of −10 volts to +10 volts.

Features

- 600 pA I_{bias} at V_{IN} = ±10V
- 500 V/μs slew rate
- 70 MHz bandwidth
- 5 mV offset voltage
- FET input
- No compensation for gains above 50
- Peak output current to 100 mA

Block and Connection Diagrams



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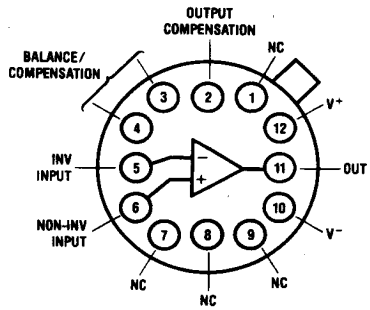

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Order Number LH0132G or LH0132CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage, V_S	±18V	Operating Temperature Range, T_A	
Input Voltage, V_{IN}	$\pm V_S$	LH0132G/AG	−55°C to +125C°C
Differential Input Voltage	±30V or $\pm 2V_S$	LH0132CG/ACG	−25°C to +85°C
Power Dissipation, P_D		Operating Junction Temperature, T_J	175°C
T_A = 25°C	1.5W, derate 100°C/W to 125°C (Note 1)	Storage Temperature Range	−65°C to +150°C
T_C = 25°C	2.2W, derate 70°C/W to 125°C (Note 1)	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2)

Parameter		Test Conditions		LH0132G			LH0132CG			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	$V_{IN}=0$	$T_A=T_J=25°C$ (Note 3)		2	5 10		2	10 20	mV
$\Delta V_{OS}\Delta T$	Average Offset Voltage Drift		(Note 4)		25	50		25	50	µV/°C
I_{OS}	Input Offset Current	$-10V \le I_N \le 10V$	$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5) $T_J=T_A=T_{MAX}$			15 150 15			30 300 5	pA pA nA
I_B	Input Bias Current		$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5) $T_J=T_A=T_{MAX}$			75 1 25			150 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$		50	60		45	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10$ V, f = 70 kHZ	$T_J=25°C$	60	70		50	70		dB
		$R_L = 1$ kΩ	(Note 6)	57			47			
V_O	Output Voltage Swing	$R_L = 1$ kΩ		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_J=25°C$, $I_O=0$	(Note 6)		18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$AV_S = 10V$	(±5 to ±15)	50	60		45	60		dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1$ kΩ, $T_J = 25°C$ (Note 7)

Parameter		Conditions		Min.	Typ.	Max.	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/µS
t_s	Settling Time to 1% of Final Value	$A_V = -1$,			100		ns
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	ns
t_D	Small Signal Delay Time				10	25	ns

Note 1. In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See Applications Notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2. LH0132G is 100% production tested as specified at 25°C, 150°C, and −55°C. LH0132CG is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3. Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25° C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4. LH0132G is 100% production tested for this parameter. LH0132CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5. Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

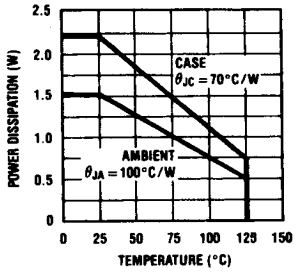
Note 6. Guaranteed thru correlated automatic pulse testing at T_J = 25°C.

Note 7. Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

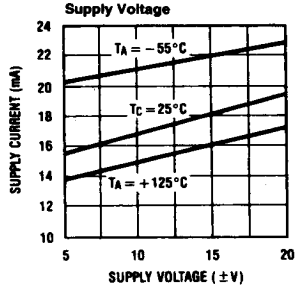
* Limits at high/low temp. are sample tested to LTPD = 10 on LH0132CG/ACG.

Typical Performance Characteristics

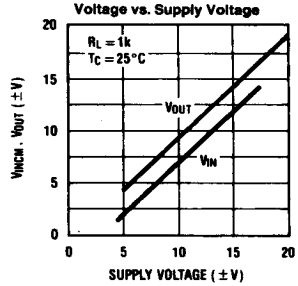
Maximum Power Dissipation



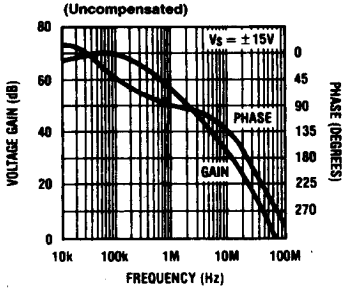
Supply Current vs. Supply Voltage



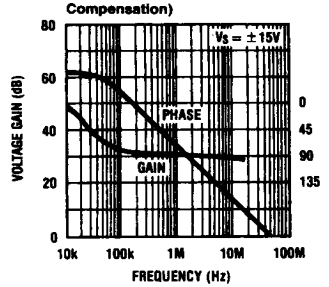
Input Voltage Range and Output Voltage vs. Supply Voltage



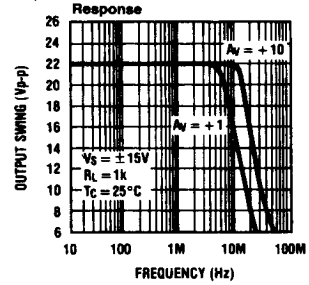
Bode Plot (Uncompensated)



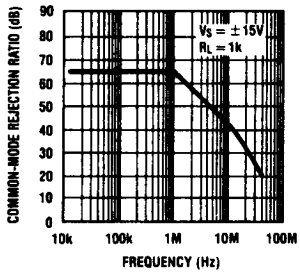
Bode Plot (Unity Gain Compensation)



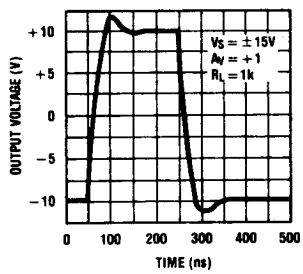
Large Signal Pulse Response



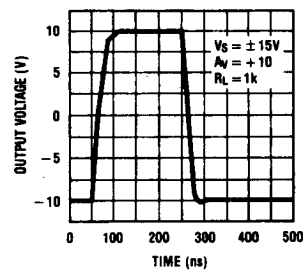
Common Mode Rejection Ratio vs. Frequency



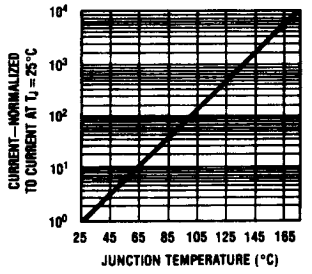
Large Signal Frequency Response



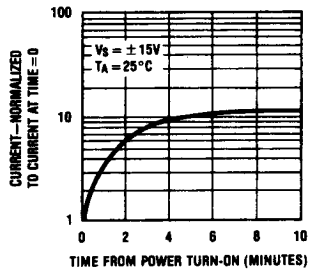
Large Signal Pulse Response



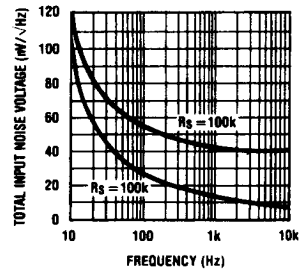
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Total Input Noise Voltage vs. Frequency*



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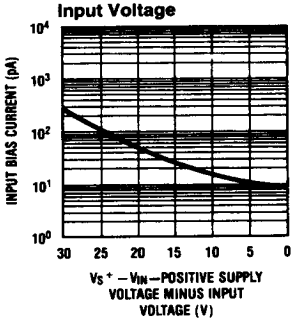
Typical Performance Characteristics (Continued)

Input Bias Current vs. Input Voltage



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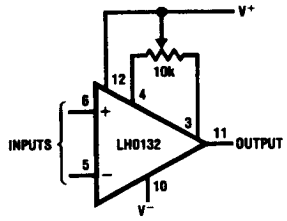
*Noise voltage includes contribution from source resistance.

Auxiliary Circuits

Offset Null



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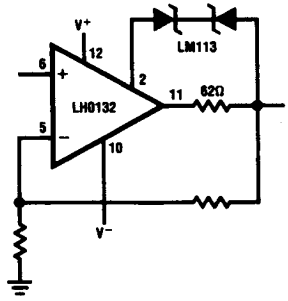
Output Short Circuit Protection



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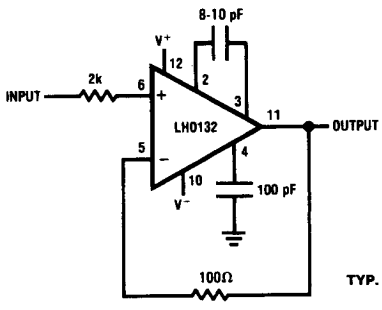
Typical Applications

Unity Gain Amplifier



TYP. $BW_{3ddBB} = 45$ MHz

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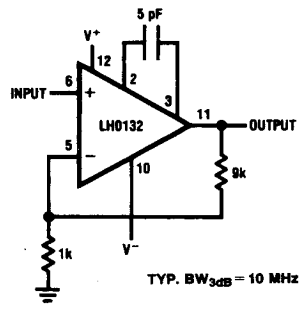
10X Buffer Amplifier



TYP. $BW_{3dB} = 10$ MHz

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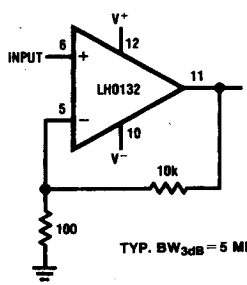
100X Buffer Amplifier



TYP. $BW_{3dB} = 5$ MHz

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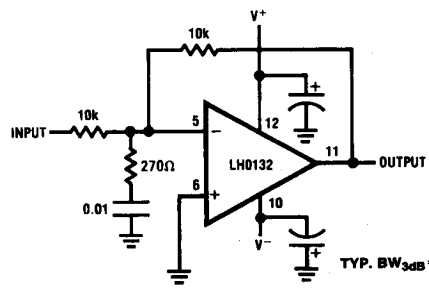
Non-Compensated Unity Gain Inverter



TYP. $BW_{3dB} = 70$ MHz

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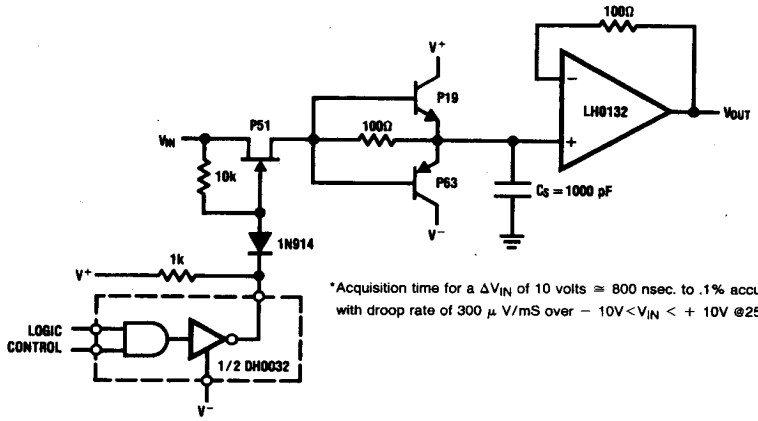
Typical Applications (Continued)

High Speed Sample and Hold



*Acquisition time for a ΔV_{IN} of 10 volts ≅ 800 nsec. to .1% accuracy with droop rate of 300 μ V/mS over − 10V < V_{IN} < + 10V @25°C.

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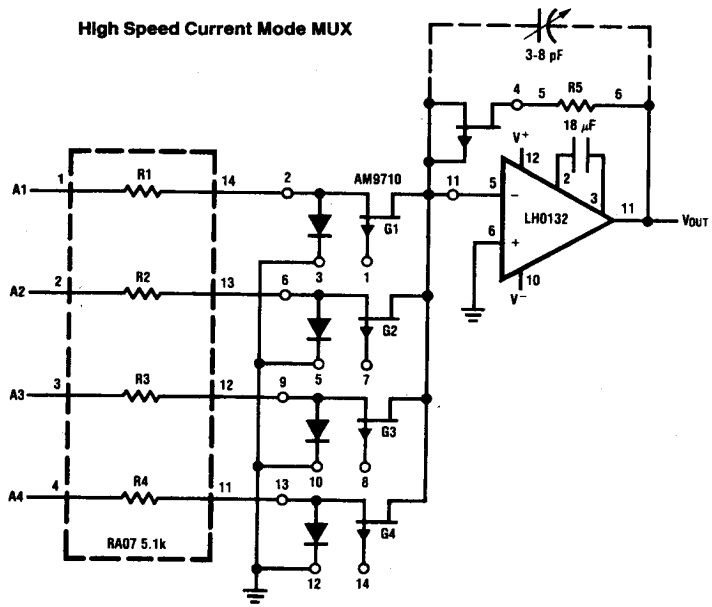
High Speed Current Mode MUX



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Applications Information

POWER SUPPLY DECOUPLING

The LH0132, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-

air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels.

Due to the cascoded FET input stage design of the LH0132, the gate-to-drain voltage is kept below this threshold, and the bias current remains relatively constant over the entire common-mode input voltage range.

INPUT CAPACITANCE

The input capacitance to the LH0132/LH0132C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0132 is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.