SHARP

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To;

TENTATIVE

SPECIFICATIONS

Product Type 240 Output LCD Common Driver

Model No. LH1537

※This tentative specifications contains 16 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: T. Mineyama

T. Mineyama
Dept. General Manager

SHARP CORPORATION ★ NOV. 14. 1997 MAIL DATE ★ IC TENRI GROUP

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- ·Instrumentation and measuring equipment
- ·Machine tools
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- ·Home appliances
- ·Communication equipment other than for trunk lines

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- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

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- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

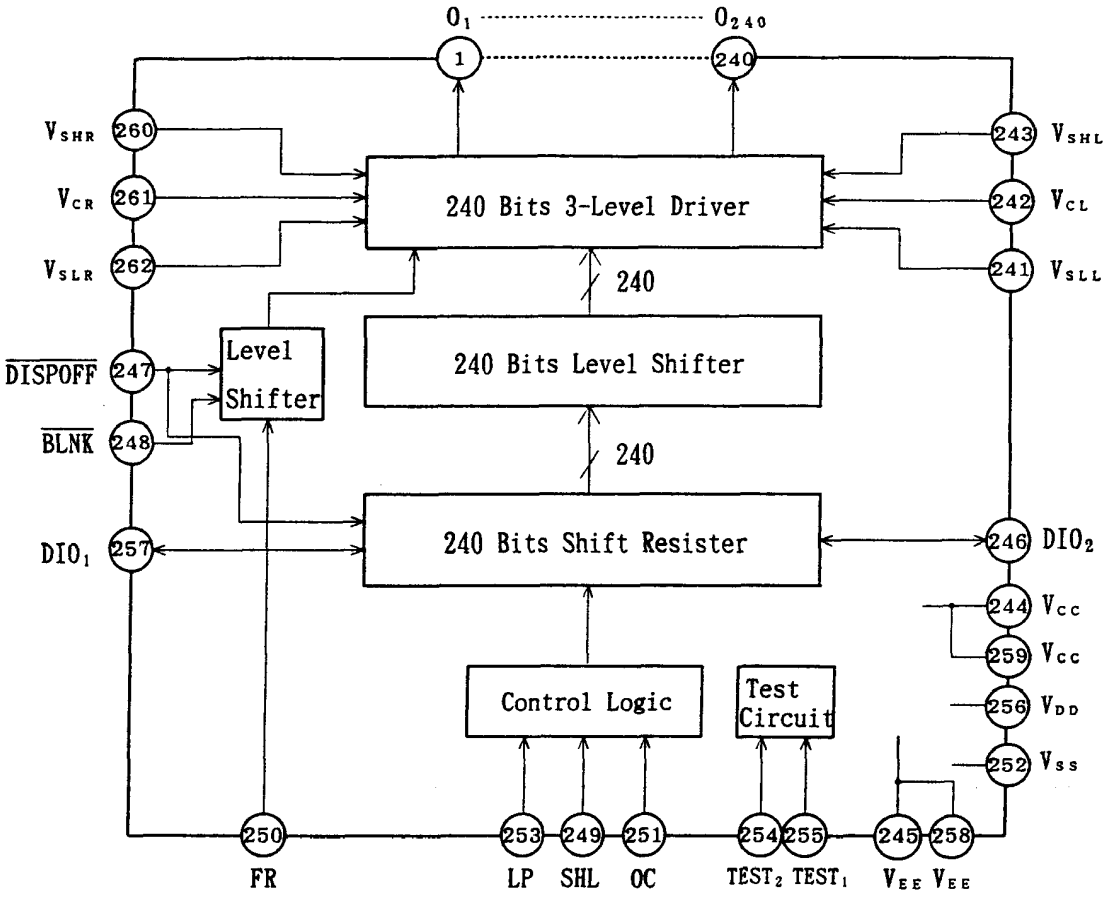
1. Summary

The LH1537 is a 240 output common driver LSI suitable for driving dot matrix LC panels using low voltage segment driving method.
With the use of SST (Super Slim TCP) technology, it is possible to decreace the size of the frame section of the LCD module.
Combined with the Segment Driver LH155E(SST) and Power Supply IC LR3694, it is possible to constitute a low power consumption LCD module.

2. Features

- Supply voltage for LC drive : +20.0 to +45.0 V
- Number of LC drive outputs : 240
- Output level : 3
- Correspond to low voltage segment driving method
- Controllable input signal directly from Controller
- Low power consumption
- Supply voltage for the logic system : +2.4 to +5.5 V
- Low output impedance : 600 Ω(Typ.)
- Shift clock frequency : 4.0 MHz(Max.)(V_{DD}=+5 V±10 %)
  : 3.0 MHz(Max.)(V_{DD}=+2.4 to +4.5 V)
- It is possible to select the number of LC drive outputs (240 outputs or 200 outputs)
- Built-in 240-bits bidirectional shift register
- Shift register circuits are reset when $\overline{\text{DISPOFF}}$ active
- Built-in blanking period control
- 2 types of shift directions are pin-selectable
  ① $O_1 \rightarrow O_{240}$ ($O_{21} \rightarrow O_{220}$)
  ② $O_{240} \rightarrow O_1$ ($O_{220} \rightarrow O_{21}$)
- CMOS silicon gate process(P-type Silicon Substrate)
- Supports a LC panel display when combined with Segment Driver LH155E and Power Supply IC LR3694
- Package : 262 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

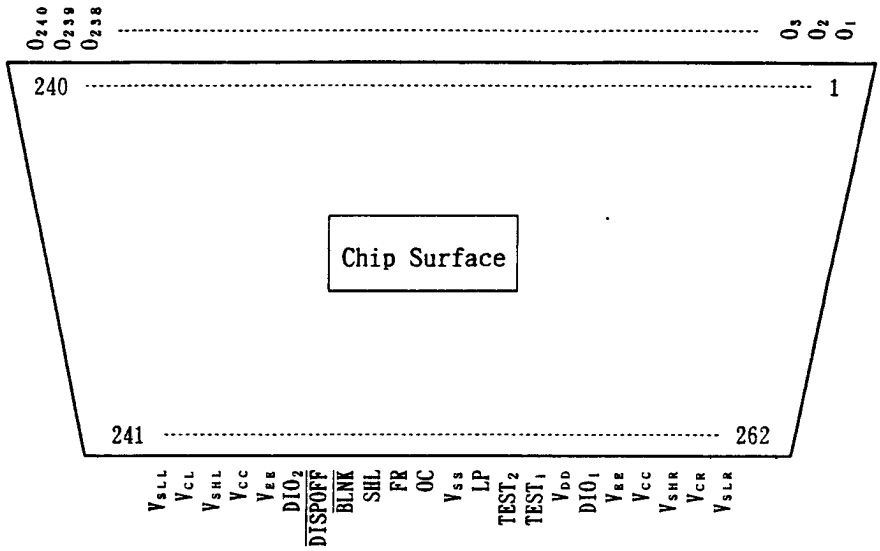
3. Block Diagram



4. Functional Operation of Each Block

Block	Function
Shift Register	The data shift direction of the shift register is controlled by Control Logic Block. According to SHL signal, input data signal(from DIO_1 or DIO_2) is shifted to next shift register responding to the falling edge of the LP signal.
Level Shifter	Level Shifter Block shifts the voltage level from the logic voltage level to the LC drive voltage, and then outputs to the 3-level Driver Block.
3-Level Driver	3-Level Driver Block otputs a level which is selected among V_{SH}, V_C, V_{SL} based on Latch data, FR, $\overline{DISPOFF}$, $\overline{BLNK}$ signals.
Control Logic	Control Logic Block controls the data shift direction of shift register according to SHL input signal.
Test Circuit	Test circuit is for the test. In general usage, it doesn't act.

5. Pin Configuration

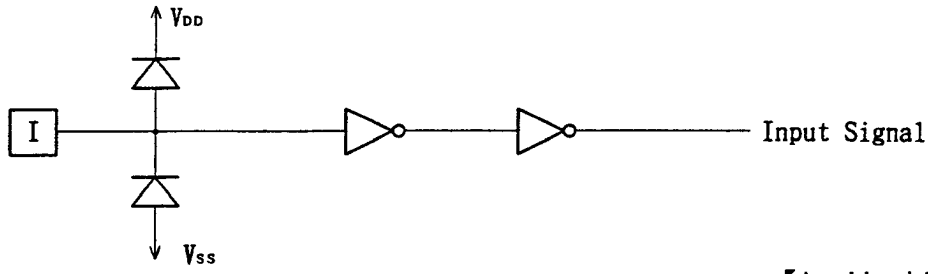


6. Pin Descriptions

6-1. Pin Designations

Pin No.	Symbol	I/O	Designation
1 ~ 240	O_1 ~O_{240}	O	LC drive output
241,262	V_{SLL},V_{SLR}	-	Power supply for LC drive
242,261	V_{CL},V_{CR}	-	Power supply for LC drive
243,260	V_{SHL},V_{SHR}	-	Power supply for LC drive
244,259	V_{CC}	-	Power supply for LC drive
245,258	V_{EE}	-	Power supply for LC drive
246	DIO_2	I/O	Data input/output for shift resister
247	$\overline{DISPOFF}$	I	Control input for unselect output level
248	$\overline{BLNK}$	I	Control input for blanking period
249	SHL	I	Shift direction selection for shift register
250	FR	I	AC-converting signal input for LC drive waveform
251	OC	I	Selection pin for the number of LC driver output
252	V_{SS}	-	Power supply for logic system(0 V)
253	LP	I	Shift clock input for shift register
254	$TEST_2$	I	Test mode selection input
255	$TEST_1$	I	Test mode selection input
256	V_{DD}	-	Power supply for logic system(+2.4 to +5.5 V)
257	DIO_1	I/O	Data input/output for shift register

6-2. Input/Output Circuits



【Applicable pins】
SHL, $\overline{DISPOFF}$
$\overline{BLNK}$, FR, LP, OC

Fig.1 Input Circuit(1)

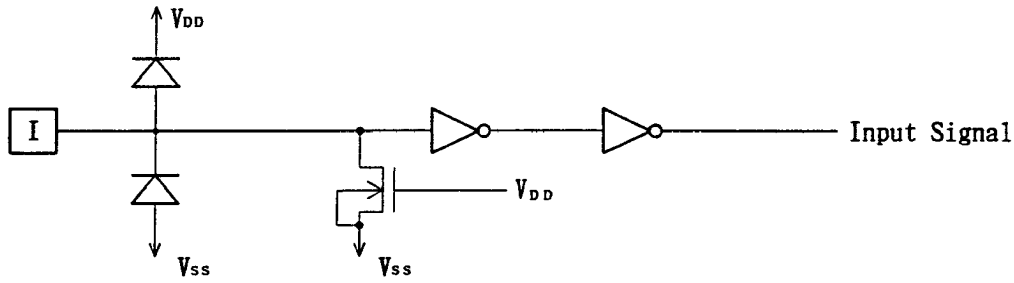
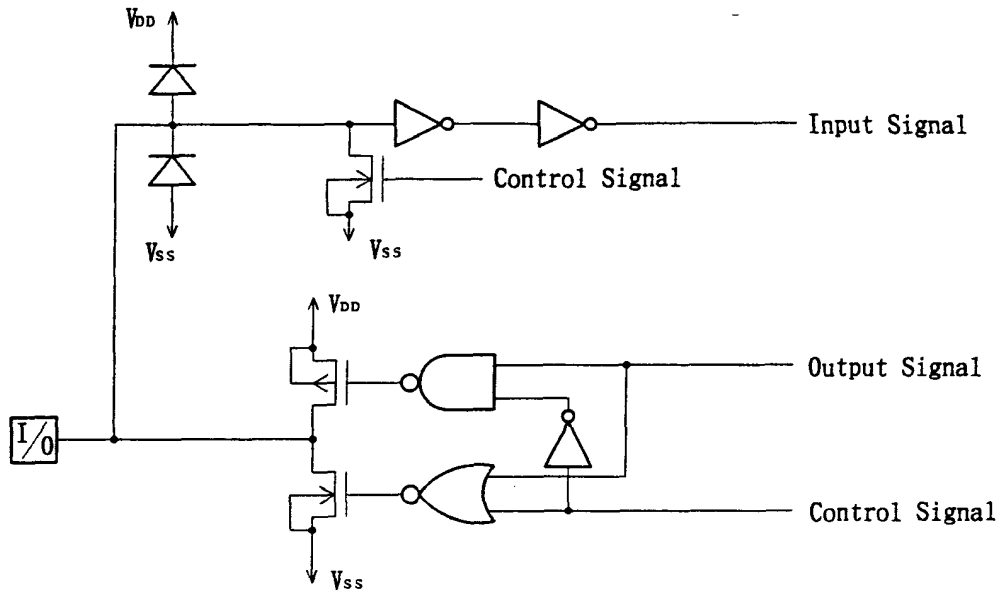


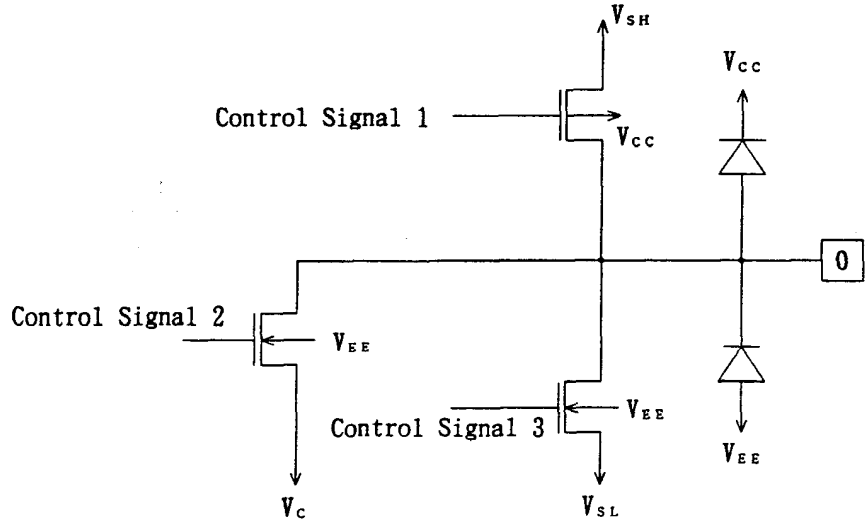
Fig.2 Input Circuit(3)

【Applicable pins】
$TEST_1$, $TEST_2$



【Applicable pins】
DIO_1, DIO_2

Fig.3 Input/Output Circuit



【Applicable pins】
O_1~O_{240}

Fig.4 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin : connect to +2.4 to +5.5 V
V_{SS}	Logic system power supply pin : connect to 0 V
V_{EE}	Power supply pin for LC drive
V_{CC}	Power supply pin for LC drive
V_{SHL}, V_{SHR} V_{CL}, V_{CR} V_{SLL}, V_{SLR}	Bias power supply pin for LC driver •Generally, the bias voltages used are set by a resistor divider. •Keep the following relation : $V_{EE} \leqq V_{SL} < V_C < V_{SH} \leqq V_{CC}$ •To reduce the difference of the output waveforms between O_1 and O_{240}, please supply the voltage externally with V_{iR} and V_{iL} pins (i=SH,C,SL).
DIO_1	Shift data input/output pin for bidirectional shift register •Input pin when SHL=L, output pin when SHL=H. •When SHL=L, DIO_1 pin becomes pull-down. When SHL=H, DIO_1 pin doesn't become pull-down.
DIO_2	Shift data input/output pin for bidirectional shift register •Input pin when SHL=H, output pin when SHL=L. •When SHL=H, DIO_2 pin becomes pull-down. When SHL=L, DIO_2 pin doesn't become pull-down.
LP	Shift clock pulse input pin for bidirectional shift register •The data is shifted responding to the falling edge of the LP pulse.
SHL	Shift derection selection pin for bidirectional shift register •The data is shifted $O_1 \rightarrow O_{240}$ when set V_{SS} level "L", and the data is shifted $O_{240} \rightarrow O_1$ when set V_{DD} level "H".
OC	Selection pin for the number of LC driver output •Selectable 240 outputs mode or 200 outputs mode. •When set V_{SS} level "L", 200 outputs mode is selected, when set V_{DD} level "H", 240 outputs mode is selected. •When this LSI is 200 outputs mode, output pins which aren't used(O_1-O_{20}, O_{221}-O_{240}) output the unselect level V_C.
$\overline{DISPOFF}$	Control input pin for output unselect level •This input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •When set V_{SS} level "L", the LC drive output pins (O_1-O_{240}) are set V_C level. •While $\overline{DISPOFF}$=L, all the shift registers are reset and don't read data. When the $\overline{DISPOFF}$ function is canceled, the shift data is read responding to the falling edge of the LP signal. However, the relation of timing between $\overline{DISPOFF}$ and LP should be kept. (AC characteristics are shown in page 12 and 13)

Symbol	Function
$\overline{BLNK}$	Control input pin for blanking period ·This input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ·When $\overline{BLNK}$=L, blanking period mode is selected, the LC drive output pins(O_1-O_{240}) are set V_C level. At this time, shift registers are active(not reset).
FR	AC conversion signal for output waveform ·The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ·Generally, input a frame inversion signal. ·Output level of this driver is defined by shift registers output (Latch data) and FR signal. ·Truth table is shown in 7-2-1.
$TEST_1$ $TEST_2$	Test mode selection pins ·During normal operation, please fix V_{SS} level "L".
O_1-O_{240}	LC driver output pins ·Corresponding to each bit of the shift register, one level (V_{SH}, V_C, V_{SL})is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	$\overline{BLNK}$	Driver Output Voltage Level (O_1-O_{240})
L	L	H	H	V_C
L	H	H	H	V_{SH}
H	L	H	H	V_C
H	H	H	H	V_{SL}
x	x	H	L	V_C
x	x	L	x	V_C

Here, $V_{EE} \leq V_{SL} < V_C < V_{SH} \leq V_{CC}$, L:$V_{SS}$(0 V), H:$V_{DD}$(+2.4 V to +5.5 V), x : Don't care

【Note】"Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Data I/O Pins and Data Transfer Direction

OC	SHL	Data Transfer Direction	DIO_1	DIO_2
L (200 outputs)	L(shift to right)	$O_{21} \rightarrow O_{220}$	Input	Output
	H(shift to left)	$O_{220} \rightarrow O_{21}$	Output	Input
H (240 outputs)	L(shift to right)	$O_1 \rightarrow O_{240}$	Input	Output
	H(shift to left)	$O_{240} \rightarrow O_1$	Output	Input

Here, L:V_{SS}(0 V), H:V_{DD}(+2.4 V to +5.5 V)

8. Precaution

○Precaution when connecting or disconnecting the power

This LSI is a LCD driver to fit high-voltage usage. So, there is a fear that this LSI may be permanently destroyed by high current, if LC drive power is supplied when the logic system power is floating.

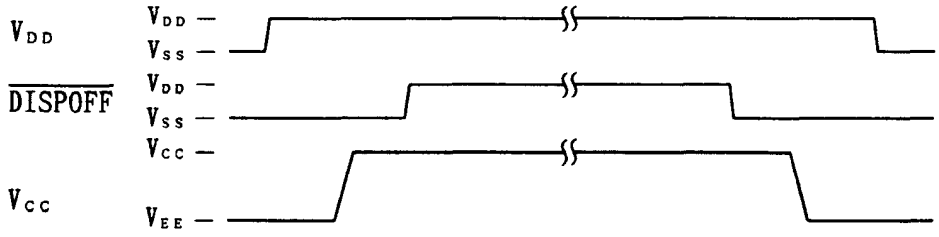
The power supply sequence is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power supply, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you to connect the serial resistor (50 to 100Ω) or fuse to the drive power V_{CC} of the system as a current limitter. And set up the suitable value of the resistor in consideration of LC display grade.

And the condition of inside of this LSI(the condition of shift register) is indefinite right after the logic power is supplied. Therefore first, please reset the logic condition(of shift register) of the inside of this LSI using $\overline{DISPOFF}$ function. Then please supply the LC drive power.

After the LC drive power has become stable, please cancel $\overline{DISPOFF}$ function. When disconnecting the power, please set the ouput of this LSI to V_C level using $\overline{DISPOFF}$ function. After that, please disconnect the LC drive power, then disconnect the logic system power.

The recommend sequence of power supply is as follows.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃ Referenced to V_{EE}	V_{DD}	V_{EE}-0.3 to V_{EE}+31.0	V
	V_{SS}		V_{SS}	V_{EE}-0.3 to V_{EE}+31.0	V
	V_{DD}-V_{SS}		V_{DD}, V_{SS}	-0.3 to +7.0	V
Supply voltage (2)	V_{CC}		V_{CC}	V_{EE}-0.3 to V_{EE}+48.0	V
	V_{SH}		V_{SHL}, V_{SHR}	V_{EE}-0.3 to V_{CC}+0.3	V
	V_C		V_{CL}, V_{CR}	V_{EE}-0.3 to V_{CC}+0.3	V
	V_{SL}		V_{SLL}, V_{SLR}	V_{EE}-0.3 to V_{CC}+0.3	V
Input voltage	V_I		DIO_1, DIO_2, SHL, LP, FR, OC, $\overline{DISPOFF}$, $\overline{BLNK}$	V_{SS}-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Note Referenced to V_{SS}	V_{DD}	V_{SS}+2.4		V_{SS}+5.5	V
Supply voltage(2)	V_{CC}		V_{CC}	V_{SS}+12.5		V_{SS}+25	V
Supply voltage(3)	V_{EE}		V_{EE}	V_{SS}-20		V_{SS}-7.5	V
Operating temperature	T_{opr}			-30		+85	℃

【Note】 Keep the following relation : $V_{EE} \leqq V_{SL} < V_C < V_{SH} \leqq V_{CC}$

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=0 V, V_{DD}=+2.4 to +5.5 V, V_{CC}-V_{EE}=+20 to +45.0 V, Ta=-30 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DIO_1, DIO_2, SHL, LP, FR, $\overline{DISPOFF}$, $\overline{BLNK}$, OC	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	DIO_1, DIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	SHL, LP, FR, $\overline{DISPOFF}$, $\overline{BLNK}$, OC			+10.0	μA
	I_{LIL}	V_I=V_{SS}	SHL, LP, FR, $\overline{DISPOFF}$, $\overline{BLNK}$, OC, DIO_1, DIO_2			-10.0	μA
Input pull-down current	I_{PD}	V_I=V_{DD}	DIO_1, DIO_2,			+100.0	μA
Output resistance	R_{ON}	|ΔV_{ON}|=0.5 V*1	O_1-O_{240}		0.6	1.0	kΩ
Stand-by current (1)	I_{STB1}	*2	V_{DD}			50.0	μA
Stand-by current (2)	I_{STB2}	*2	V_{CC}			50.0	μA
Consumed current (1)	I_{DD}	*3	V_{DD}				μA
Consumed current (2)	I_{CC}	*3	V_{CC}				μA

【Note】 *1 : V_{CC}=V_{SH}=+22.5 V, V_C=+2.5 V, V_{EE}=V_{SL}=-17.5 V, V_{DD}=+5.0 V

*2: V_{CC}=V_{SH}=+25 V, V_C=+2.5 V, V_{EE}=V_{SL}=-20 V, V_{DD}=+5.0 V, V_I=V_{SS}

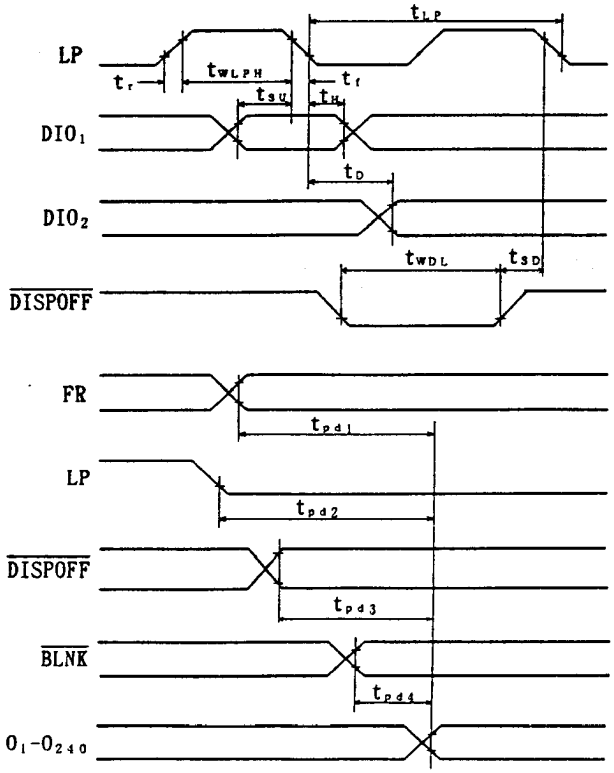
*3: V_{CC}=V_{SH}=+25 V, V_C=+2.5 V, V_{EE}=V_{SL}=-20 V, V_{DD}=+5.0 V
f_{LP}=19.2 kHz, f_{FR}=80 Hz. 1/240 Duty operation, No-load

11-2. AC Characteristics

(V_{SS}=0 V, V_{DD}=+2.4 to +5.5 V, V_{CC}-V_{EE}=+20 to +45 V, Ta=-30 to +85 ℃)

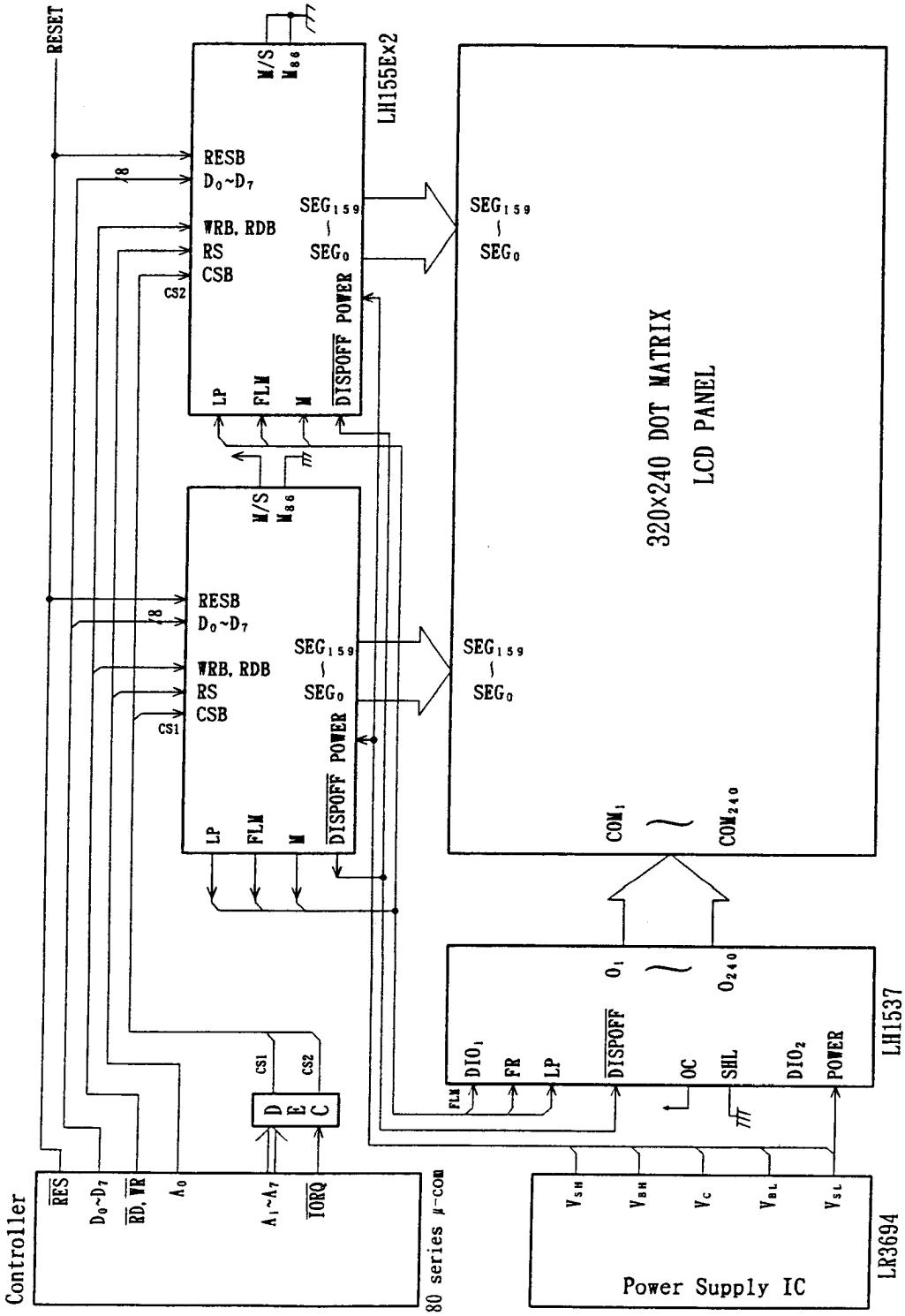
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{LP}	V_{DD}=+5 V±10%	250			ns
		V_{DD}=+2.4 to +4.5 V	330			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=+5 V±10%	30			ns
		V_{DD}=+2.4 to +4.5 V	60			ns
Shift clock "L" pulse width	t_{WLPL}	V_{DD}=+5 V±10%	120			ns
		V_{DD}=+2.4 to +4.5 V	170			ns
Data setup time	t_{SU}		50			ns
Data hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		120			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_D	C_L=15 pF V_{DD}=+5 V±10%			170	ns
		C_L=15 pF V_{DD}=+2.4 to +4.5 V			250	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	µs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	µs
Output delay time (4)	t_{pd4}	C_L=15 pF			1.2	µs

11-3. Timing Diagram



[SHL="L"]
Timing chart

12. Example of System configuration



13. Example of Typical Characteristic

(Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V)

Parameter	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time		10		ns