SHARP

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To;

TENTATIVE

SPECIFICATIONS

Product Type 160 Output LCD Segment Driver

Model No. LH1540A

※This tentative specifications contains 20 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

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SHARP CORPORATION
JAN. 07. 1998
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- ·Instrumentation and measuring equipment
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- ·Home appliances
- ·Communication equipment other than for trunk lines

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

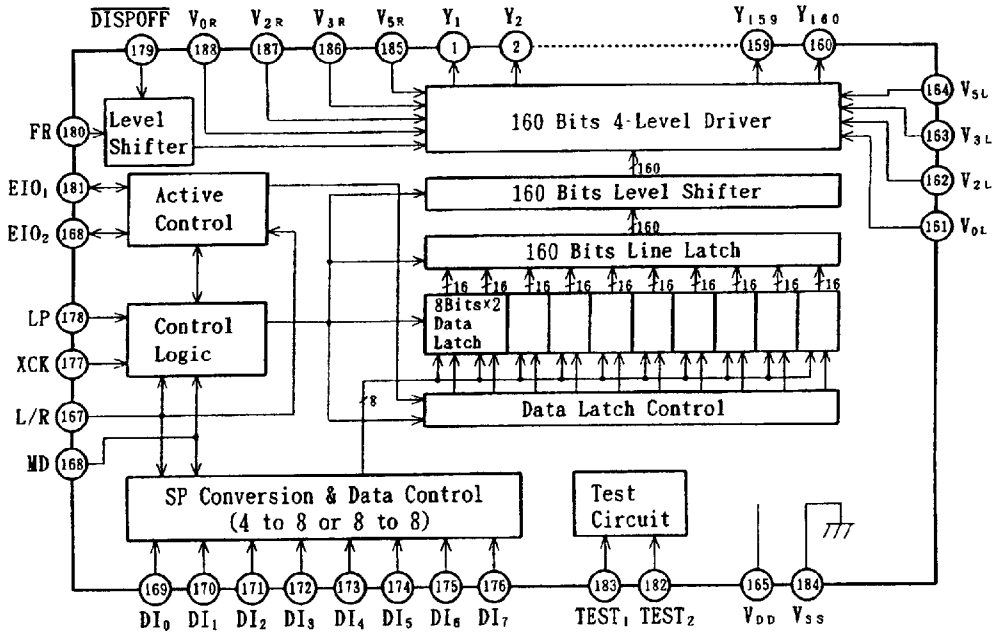
1. Summary

The LH1540A is a 160 output segment driver LSI suitable for driving large scale dot matrix LC panels using as personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. When combined with the LH1530 Common Driver, a low power consuming, high-precision LC panel display can be assembled.

2. Features

- Number of LC drive outputs : 160
- Supply voltage for LC drive : +10.0 to +42.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Low power consumption
- Shift Clock frequency : 20 MHz (Max.) V_{DD}=+5.0 V±10%
  : 15 MHz (Max.) V_{DD}=+3.0 to +4.5 V
  : 12 MHz (Max.) V_{DD}=+2.5 to +3.0 V
- Low output impedance
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 160 of input data
- Supports high capacity LC panel display when combined with the LH1530 Common Driver
- CMOS silicon gate process (P-type Silicon Substrate)
- Package : 188 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

3. Block Diagram

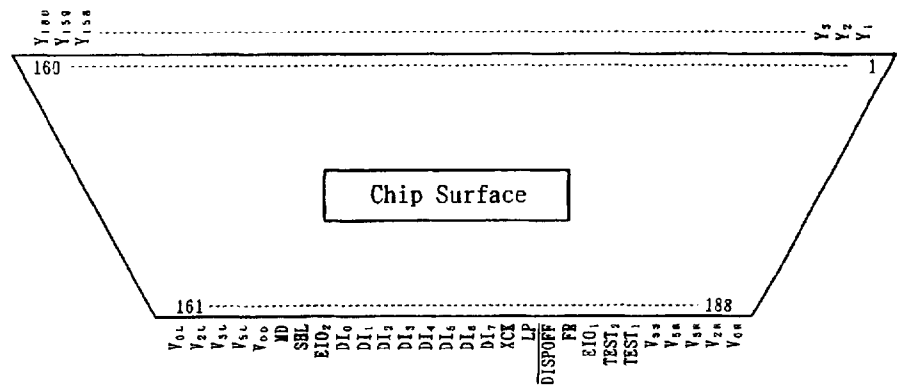


4. Functional Operations of Each Block

Block	Function
Active Control	Controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
SP Conversion & Data Control	Data is retained until 8 bits have been completely input, after which they are put on the internal data bus 8 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 160 bits of data are read in 20 sets of 8 bits.
Line Latch	All 160 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

Block	Function
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the latch data, selecting one of 4 levels (V_0, V_2, V_3, V_5) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the operation of each block. When a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

5. Pin Configuration

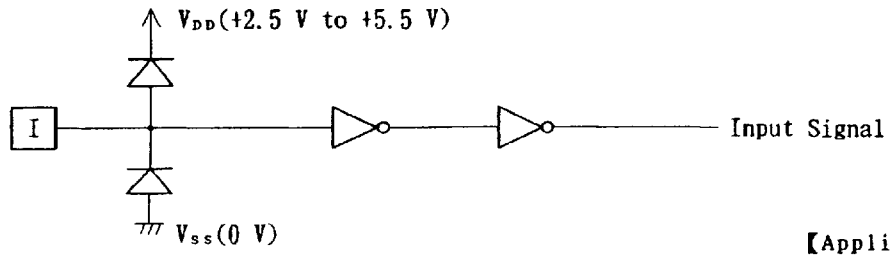


6. Pin Descriptions

6-1. Pin Designations

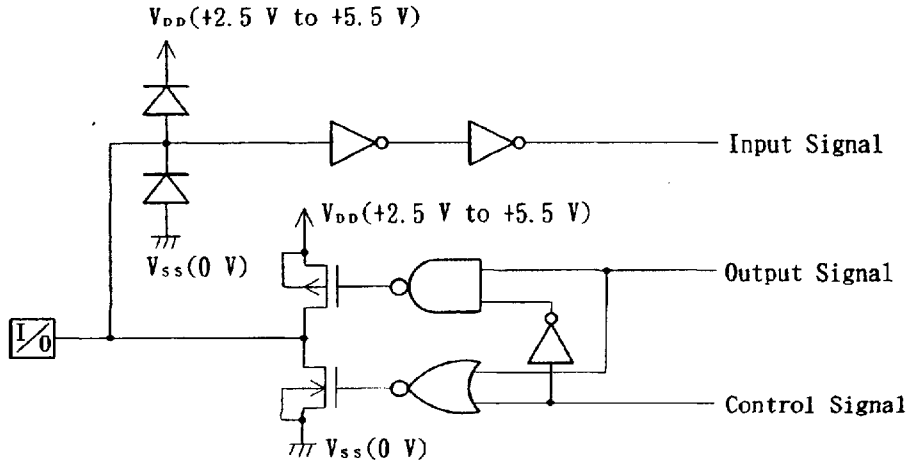
Pin No.	Symbol	I/O	Designation
1 to 160	Y_1 - Y_{160}	O	LC drive output
161, 188	V_{0R}, V_{0L}	-	Power supply for LC drive
162, 187	V_{2R}, V_{2L}	-	Power supply for LC drive
163, 186	V_{3R}, V_{3L}	-	Power supply for LC drive
164, 185	V_{5R}, V_{5L}	-	Power supply for LC drive
165	V_{DD}	-	Power supply for logic system (+2.5 to +5.5 V)
166	MD	I	Mode selection input
167	SHL	I	Display data shift direction selection
168, 181	EIO_2, EIO_1	I/O	Input/Output for chip select
169 to 176	DI_0-DI_7	I	Display data input
177	XCK	I	Display data shift clock input
178	LP	I	Display data latch pulse input
179	DISPOFF	I	Control input for deselect output level
180	FR	I	AC-converting signal input for LC drive waveform
182	$TEST_2$	I	Test mode selection input
183	$TEST_1$	I	Test mode selection input
184	V_{SS}	-	Ground (0 V)

6-2. Input/Output Circuits



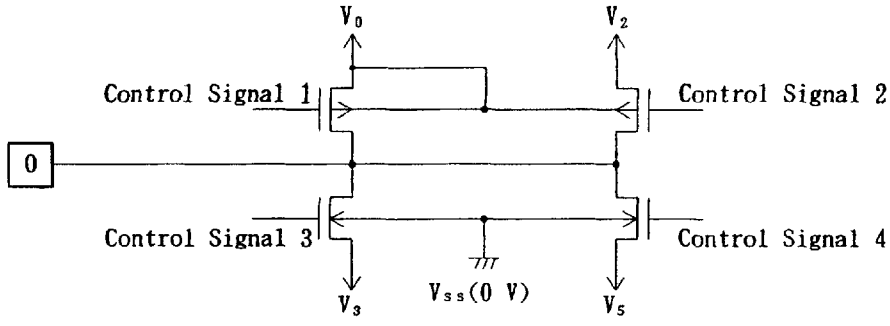
【Applicable pins】
DI_{0-7}, XCK, LP, FR
SHL, MD, $\overline{DISPOFF}$

Fig.1 Input Circuit



【Applicable pins】
EIO_1, EIO_2

Fig.2 Input/Output Circuit



【Applicable pins】
Y_1–Y_{160}

Fig.3 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{2R}, V_{2L} V_{3R}, V_{3L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. •Normally, the bias voltage ,that is set by a resistor divider. •Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$. •To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (i=0, 2, 3, 5). •If only use V_{iR} or V_{iL} as power supply pin for LC driver voltage bias, use V_{iL} pin.
DI_0-DI_7	Input Pin for display data •In 4-bit parallel input mode, input data into the 4 pins DI_0-DI_3. Connect DI_4-DI_7 to V_{SS} or V_{DD}. •In 8-bit parallel input mode, input data into the 8 pins DI_0-DI_7.
XCK	Clock input pin for taking display data •Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data •Data is latched on the falling edge of the clock pulse.
SHL	Direction selection pin for reading display data •When set to V_{SS} level "L", data is read sequentially from Y_{160} to Y_1. •When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{160}.
$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •When set to V_{SS} level "L", the LC driver output pins (Y_1-Y_{160}) are set to level V_5.
FR	AC signal input for LC driving waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. •Normally, inputs a frame inversion signal. •The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in 7-2-1.
MD	Mode selection pin •When set to V_{SS} level "L", 4-bit parallel input mode is set. •When set to V_{DD} level "H", 8-bit parallel input mode is set. •The relationship between the display data and driver output pins is shown in 7-2-2.

Symbol	Function
EIO_1 EIO_2	Input/Output pin for chip selection ·When SHL input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. ·When SHL input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. ·During output, set to "H" while LP*$\overline{XCK}$ is "H" and after 160 bits of data have been read set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". ·During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected.
$TEST_1$ $TEST_2$	Test mode select pin ·During normal operation, tie to V_{SS} level "L".
Y_1-Y_{160}	LC driver output pins ·Corresponding directly to each bit of the data latch, one level (V_0, V_2, V_3, or V_5) is selected and output.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1-Y_{160})
L	L	H	V_3
L	H	H	V_5
H	L	H	V_2
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \leq V_5 < V_3 < V_2 < V_0$, H : V_{DD}(+2.5 to +5.5 V), L : V_{SS}(0 V), X : Don't care

【Note】 "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage,LC drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.

7-2-2. Relationship between the Display Data and Driver Output pins

(a) 4-Bit Parallel Mode

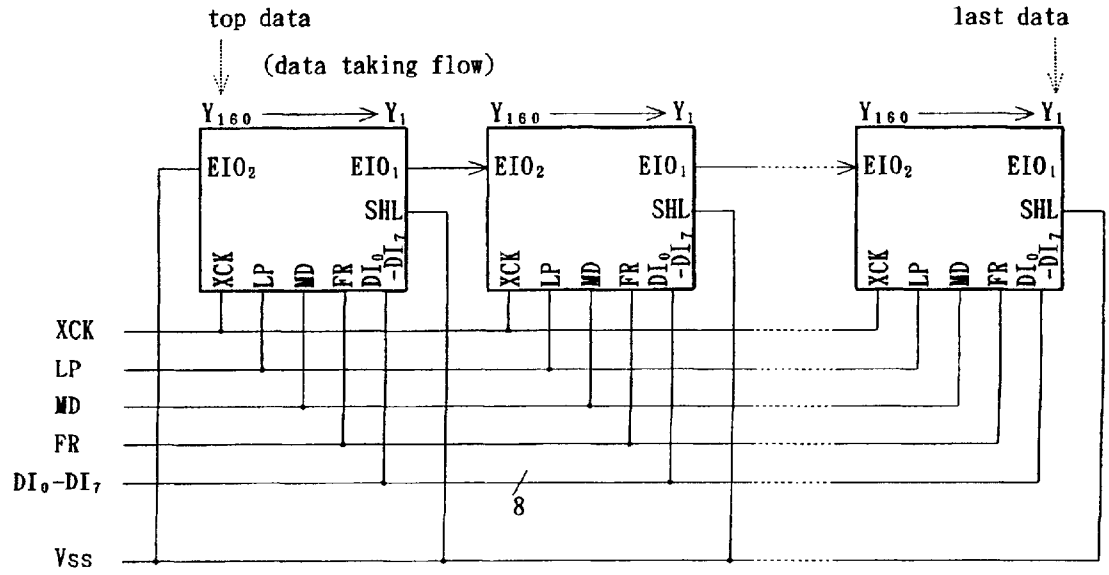
MD	SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
					40clock	39clock	38clock	···	3clock	2clock	1clock
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	···	Y_{149}	Y_{153}	Y_{157}
				DI_1	Y_2	Y_6	Y_{10}	···	Y_{150}	Y_{154}	Y_{158}
				DI_2	Y_3	Y_7	Y_{11}	···	Y_{151}	Y_{155}	Y_{159}
				DI_3	Y_4	Y_8	Y_{12}	···	Y_{152}	Y_{156}	Y_{160}
L	H	Input	Output	DI_0	Y_{160}	Y_{156}	Y_{152}	···	Y_{12}	Y_8	Y_4
				DI_1	Y_{159}	Y_{155}	Y_{151}	···	Y_{11}	Y_7	Y_3
				DI_2	Y_{158}	Y_{154}	Y_{150}	···	Y_{10}	Y_6	Y_2
				DI_3	Y_{157}	Y_{153}	Y_{149}	···	Y_9	Y_5	Y_1

(b) 8-Bit Parallel Mode

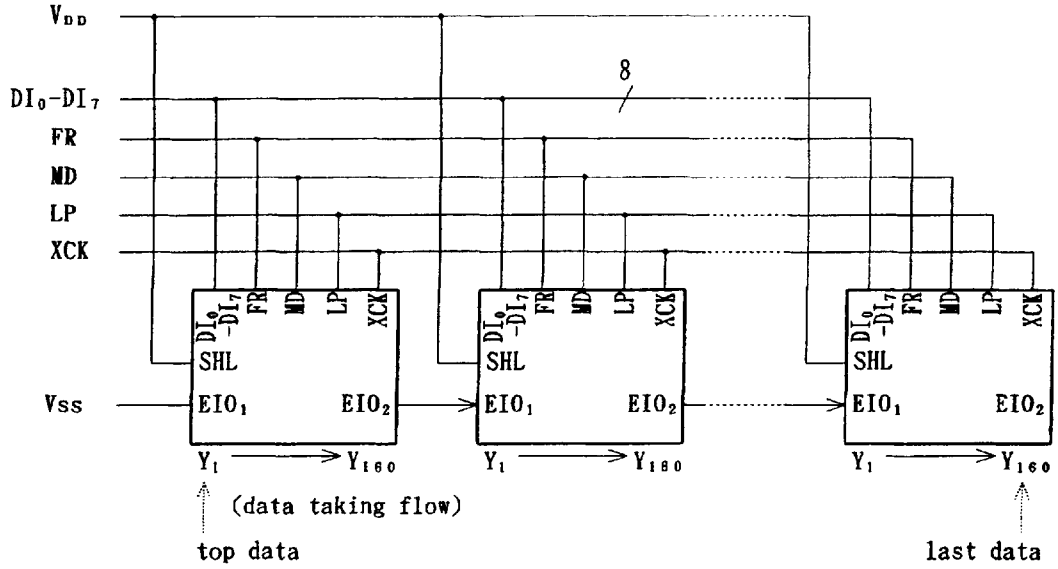
MD	SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
					20clock	19clock	18clock	···	3clock	2clock	1clock
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	···	Y_{137}	Y_{145}	Y_{153}
				DI_1	Y_2	Y_{10}	Y_{18}	···	Y_{138}	Y_{146}	Y_{154}
				DI_2	Y_3	Y_{11}	Y_{19}	···	Y_{139}	Y_{147}	Y_{155}
				DI_3	Y_4	Y_{12}	Y_{20}	···	Y_{140}	Y_{148}	Y_{156}
				DI_4	Y_5	Y_{13}	Y_{21}	···	Y_{141}	Y_{149}	Y_{157}
				DI_5	Y_6	Y_{14}	Y_{22}	···	Y_{142}	Y_{150}	Y_{158}
				DI_6	Y_7	Y_{15}	Y_{23}	···	Y_{143}	Y_{151}	Y_{159}
				DI_7	Y_8	Y_{16}	Y_{24}	···	Y_{144}	Y_{152}	Y_{160}
H	H	Input	Output	DI_0	Y_{160}	Y_{152}	Y_{144}	···	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{159}	Y_{151}	Y_{143}	···	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{158}	Y_{150}	Y_{142}	···	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{157}	Y_{149}	Y_{141}	···	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{156}	Y_{148}	Y_{140}	···	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{155}	Y_{147}	Y_{139}	···	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{154}	Y_{146}	Y_{138}	···	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{153}	Y_{145}	Y_{137}	···	Y_{17}	Y_9	Y_1

7-2-3. Connection Examples of Plural Segment Drivers

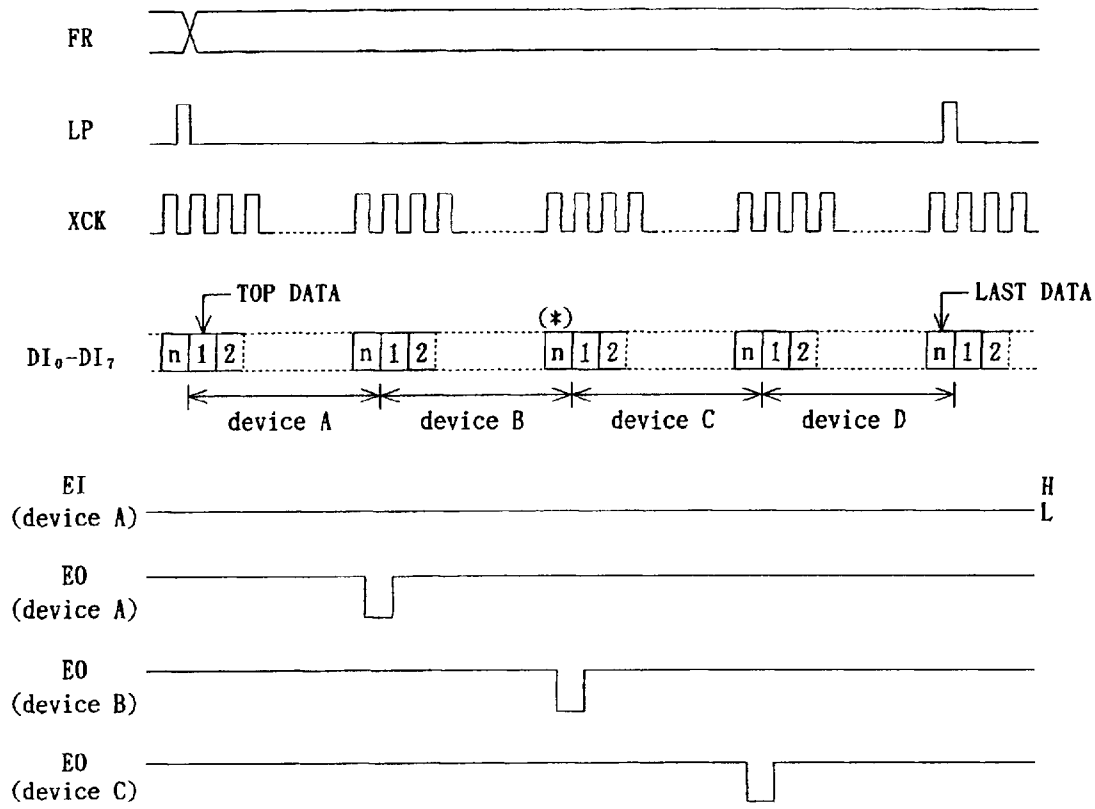
(a) Case of SHL="L"



(b) Case of SHL="H"



7-2-4. Timing Chart of 4-Device cascade Connection



(*) : 4-bit parallel mode n=40

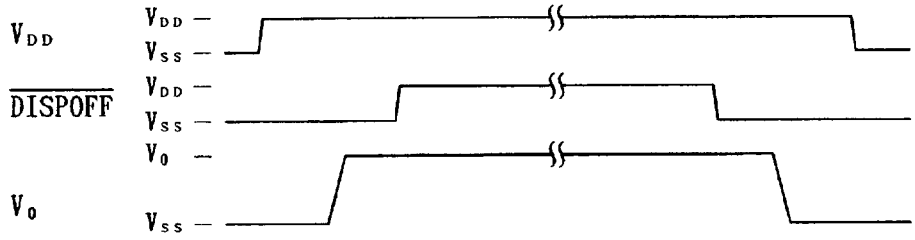
8-bit parallel mode n=20

8. Precaution

○Precaution when connecting or disconnecting the power
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor(50 to 100 Ω) or fuse to the LC drive power V_0 of the system as a current limitter. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC driver power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0	Referenced	V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_2	to V_{SS}(0 V)	V_{2L}, V_{2R}	-0.3 to V_0+0.3	V
	V_3		V_{3L}, V_{3R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, SHL, FR, MD, EIO_1, EIO_2, DISPOFF	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0	to V_{SS}(0 V)	V_{0L}, V_{0R}	+10.0		+42.0	V
Operating temperature	T_{opr}			-20		+85	℃

【NOTE】 Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$.

11. Electrical Characteristics

11-1. DC Characteristics

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ to $+5.5$ V, $V_0=+10.0$ to $+42.0$ V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DI_{0-7}, XCK, LP, SHL, FR, MD, EIO_1, EIO_2, DISPOFF	0.7V_{DD}			V
	V_{IL}					0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_I \leqq V_{DD}$	All input pins			±10.0	μA
I/O leakage current	$I_{LI/O}$	$V_{SS} \leqq V_I \leqq V_{DD}$	EIO_1, EIO_2			±10.0	μA
Output resistance	R_{ON}	*1 V_0=+40 V	Y_1-Y_{160}		1.0	1.5	kΩ
		V_0=+30 V			1.5	2.0	
		V_0=+20 V			2.0	2.5	
Stand-by current	I_{STB}	*2	V_{SS}			50.0	μA
Consumed current (1) (Deselection)	I_{DD1}	*3	V_{DD}			2.0	mA
Consumed current (2) (Selection)	I_{DD2}	*3	V_{DD}			8.0	mA
Consumed current (3)	I_0	*4	V_{0L}, V_{0R}			1.0	mA

【NOTE】

*1 : $|\Delta V_{ON}|$=0.5 V

*2 : V_{DD}=+5.0 V, V_0=+40.0 V, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$

*3 : V_{DD}=+5.0 V, V_0=+40.0 V, f_{XCK}=20 MHz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

*4 : V_{DD}=+5.0 V, V_0=+40.0 V, f_{XCK}=20 MHz, f_{LP}=41.6 kHz, f_{FR}=80 Hz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

11-2. AC Characteristics

(mode 1)

V_{SS}=0 V, V_{DD}=+5.0 V±10%, V_0=+10.0 to +42.0 V, Ta=-20 to +85 ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	50			ns
Shift clock "H" pulse width	t_{WCKH}		12			ns
Shift clock "L" pulse width	t_{WCKL}		14			ns
Data setup time	t_{DS}		10			ns
Data hold time	t_{DH}		10			ns
Latch pulse "H" pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		25			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift clock fall time	t_{LH}		25			ns
Enable setup time	t_S		10			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1,EIO_2	t_D	C_L=15 pF			30	ns
Output delay time (2) FR to Y_1-Y_{160}	tpd_1	C_L=15 pF			1.2	µs
Output delay time (3) LP to Y_1-Y_{160}	tpd_2	C_L=15 pF			1.2	µs

【Note】

*1 Take the cascade connection into consideration.

*2 $(t_{WCK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

*3 $t_r, t_f \leqq 10$ ns

(mode 2)

V_{SS}=0 V, V_{DD}=+3.0 V to +4.5 V, V_0=+10.0 to +42.0 V, Ta=-20 to +85 ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	66			ns
Shift clock "H" pulse width	t_{WCKH}		23			ns
Shift clock "L" pulse width	t_{WCKL}		23			ns
Data setup time	t_{DS}		15			ns
Data hold time	t_{DH}		20			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Enable setup time	t_S		12			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1,EIO_2	t_D	C_L=15 pF			44	ns
Output delay time (2) FR to Y_1-Y_{160}	tpd_1	C_L=15 pF			1.2	µs
Output delay time (3) LP to Y_1-Y_{160}	tpd_2	C_L=15 pF			1.2	µs

【Note】

*1 Take the cascade connection into consideration.

*2 $(t_{WCK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

*3 $t_r, t_f \leqq 10$ ns

(mode 3)

V_{SS}=0 V, V_{DD}=+2.5 to +3.0 V, V_0=+10.0 to +42.0 V, Ta=−20 to +85 ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ns
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		20			ns
Data hold time	t_{DH}		20			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Enable setup time	t_S		15			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1, EIO_2	t_D	C_L=15 pF			57	ns
Output delay time (2) FR to Y_1-Y_{160}	tpd_1	C_L=15 pF			1.2	μs
Output delay time (3) LP to Y_1-Y_{160}	tpd_2	C_L=15 pF			1.2	μs

【Note】

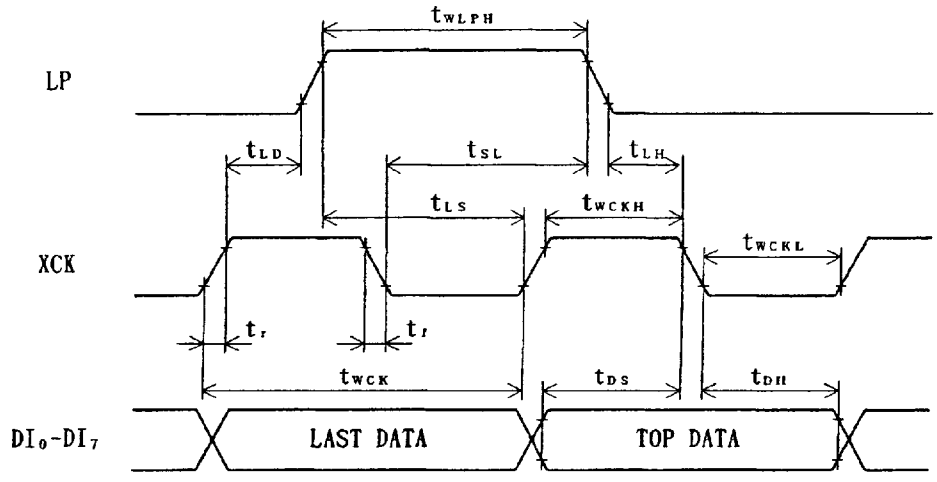
*1 Take the cascade connection into consideration.

*2 $(t_{WCK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

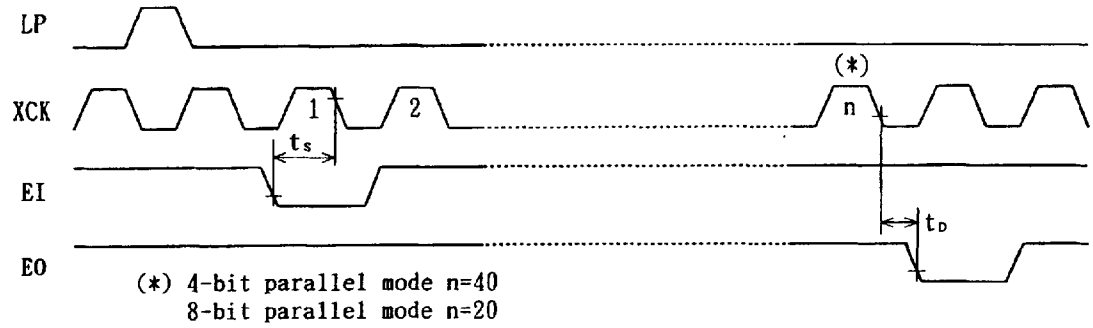
*3 t_r, t_f≦10 ns

11-3. Timing Diagrams

Input Timing Characteristics

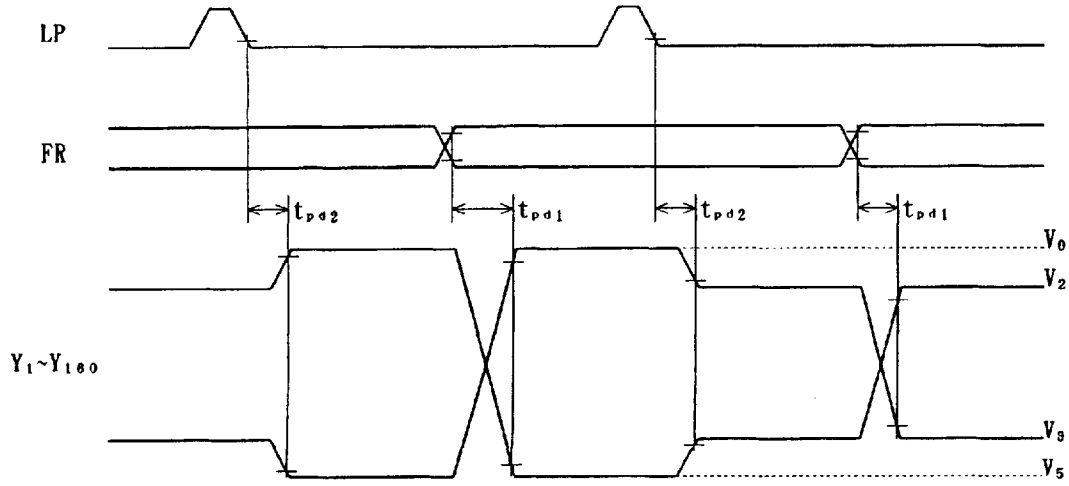


Input/Output Timing Characteristics

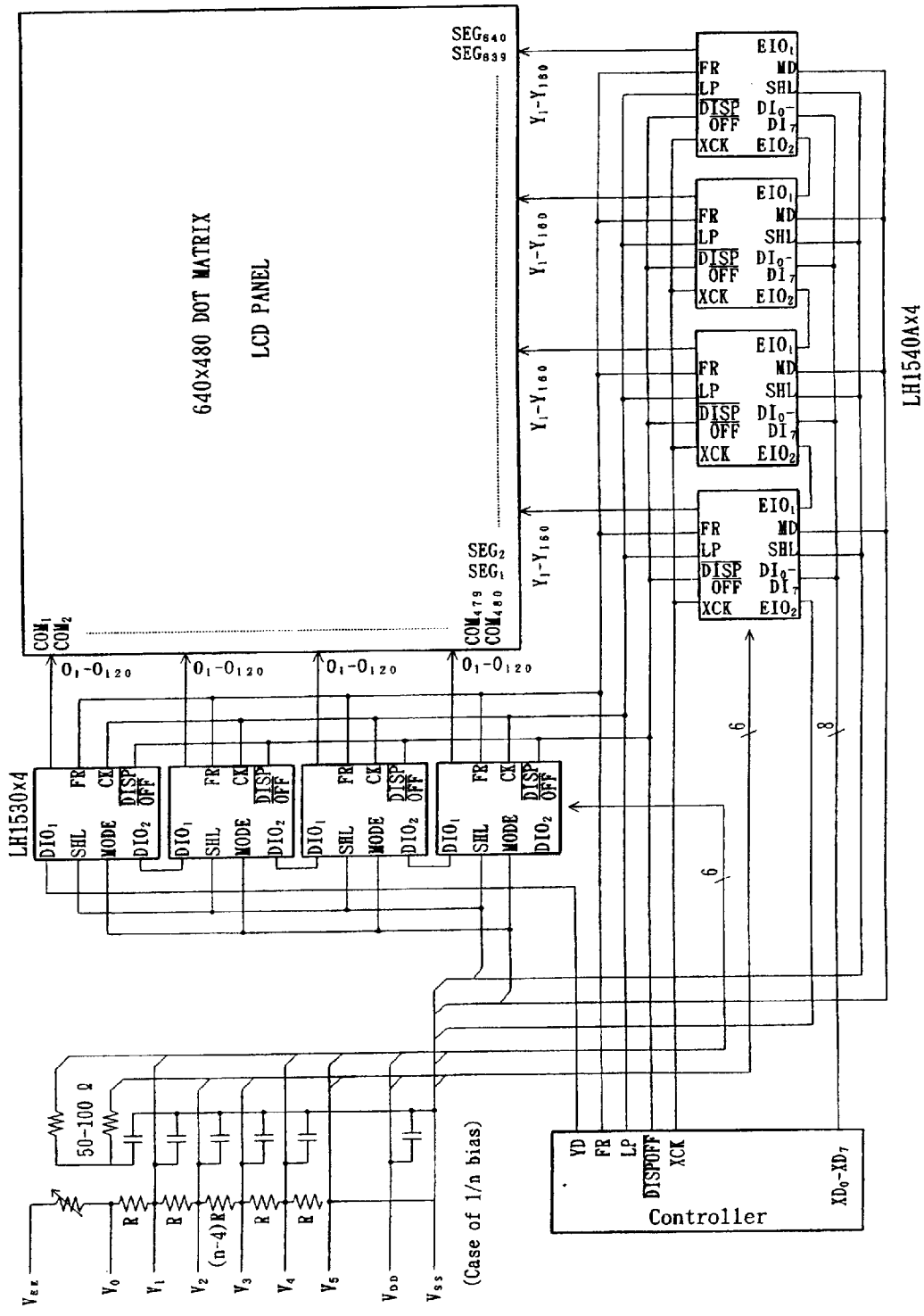


(*) 4-bit parallel mode n=40
8-bit parallel mode n=20

Output Timing Characteristics



12. Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V		10		ns