SHARP

SPEC No.	EL09Y001
ISSUE:	Nov. 7. 1997

To ;

REFERENCE

SPECIFICATIONS

Product Type 240 Output LCD Segment/Common Driver

Model No. LH1562F4

※This specifications contains 37 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

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REVIEWED BY:

PREPARED BY: A. Murakashi

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●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Summary

The LH1562F4 is a 240 output segment/common driver LSI suitable for driving large scale dot matrix LC panels using as personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. The LH1562F4 is good both segment driver and common driver, and a low power consuming, high-precision LC panel display can be assembled.
In case of segment mode, the data input is selected 4bit parallel input mode and 8bit parallel input mode by a mode(MD) pin.
In case of common mode, data input/output pins are bidirectional, four data shift directions are pin-selectable.

2. Features

(Segment mode)

- Shift Clock frequency : 20 MHz (Max.) (V_{DD}=+5 V±10%)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 240 of input data
- Line latch circuit reset function when $\overline{\text{DISPOFF}}$ active

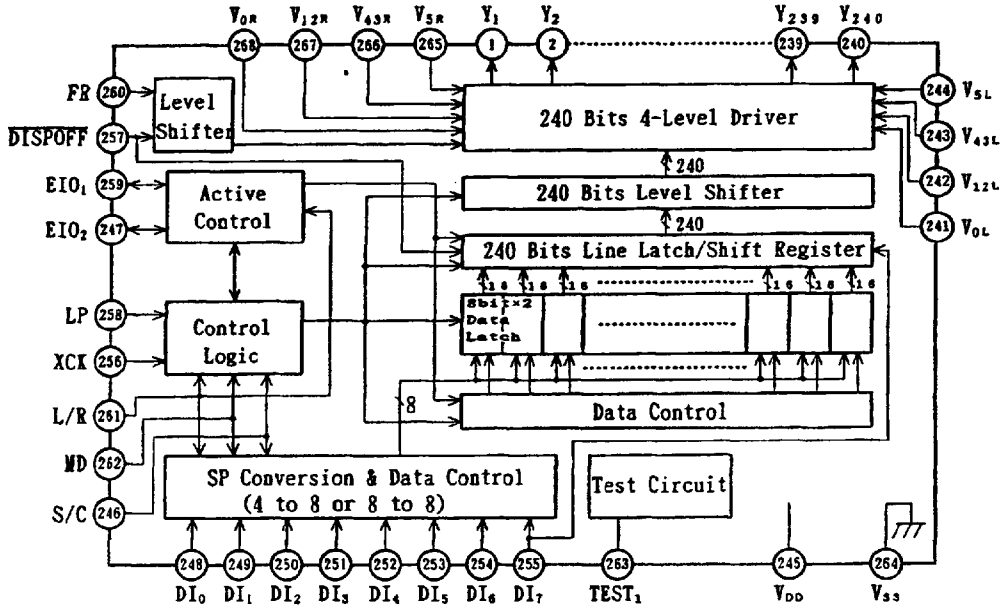
(Common mode)

- Shift clock frequency : 4.0 MHz (Max.)
- Built-in 240-bits bidirectional shift register (divisible into 120 bits x2)
- Available in a single mode (240-bits shift register) or in a dual mode (120-bits shift register x2)
  ① $Y_1 \rightarrow Y_{240}$ Single mode
  ② $Y_{240} \rightarrow Y_1$ "
  ③ $Y_1 \rightarrow Y_{120}$, $Y_{121} \rightarrow Y_{240}$ Dual mode
  ④ $Y_{240} \rightarrow Y_{121}$, $Y_{120} \rightarrow Y_1$ "
  The above 4 shift directions are pin-selectable
- Shift register circuit reset function when $\overline{\text{DISPOFF}}$ active

(Both segment mode and common mode)

- Supply voltage for LC drive : +15.0 to +42.0 V
- Number of LC drive outputs : 240
- Low output impedance
- Low power consumption
- Supply voltage for the logic system : +2.5 to +5.5 V
- CMOS silicon gate process(P-type Silicon Substrate)
- Package : 268pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

3. Block Diagram

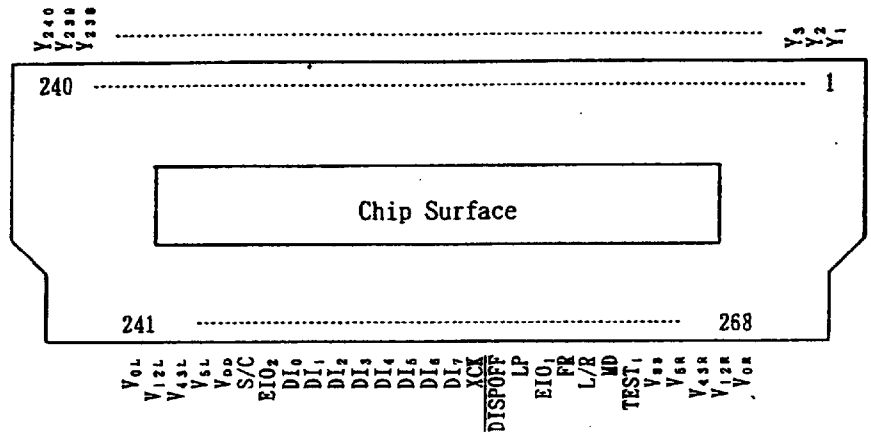


4. Functional Operations of Each Block

Block	Function
Active Control	In case of segment mode, controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected. In case of common mode, controls the input/output data of bidirectional pins.
SP Conversion & Data Control	In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit,after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

Block	Function
Data Latch	In case of segment mode, latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control. 240 bits of data are read in 30 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block. In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LC driver voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{DISPOFF}$ signals.
Control Logic	Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled.240 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.
Test Circuit	The circuit for the test. During normal operation, it doesn't act.

5. Pin Configuration

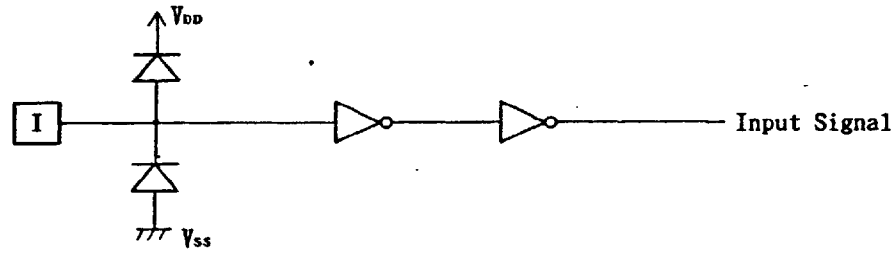


6. Pin Descriptions

6-1. Pin Designations

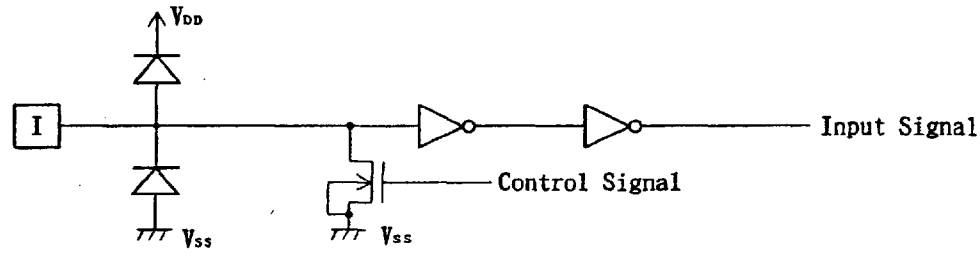
Pin No.	Symbol	I/O	Designation
1 to 240	Y_1-Y_{240}	O	LC drive output
241, 268	V_{0L}, V_{0R}	-	Power supply for LC drive
242, 267	V_{12L}, V_{12R}	-	Power supply for LC drive
243, 266	V_{43L}, V_{43R}	-	Power supply for LC drive
244, 265	V_{5L}, V_{5R}	-	Power supply for LC drive
264	V_{SS}	-	Ground(0 V)
245	V_{DD}	-	Power supply for logic system(+2.5 to +5.5 V)
246	S/C	I	Segment mode/common mode selection
247	EIO_2	I/O	Input/output for chip select or data of shift register
248 to 254	DI_0-DI_6	I	Display data input for segment mode
255	DI_7	I	Display data input for Segment mode/ Dual mode data input
256	XCK	I	Display data shift clock input for segment mode
257	$\overline{DISPOFF}$	I	Control input for deselect output level
258	LP	I	Latch pulse input/shift clock input for shift register
259	EIO_1	I/O	Input/output for chip select or data of shift register
260	FR	I	AC-converting signal input for LC drive waveform
261	L/R	I	Display data shift direction selection
262	MD	I	Mode selection input
263	$TEST_1$	I	Test mode selection input

6-2. Input/Output Circuits



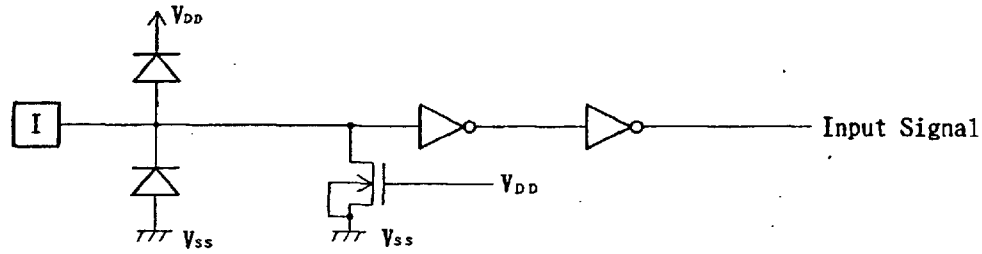
【Applicable pins】
L/R, S/C, DI_0~DI_5, $\overline{DISPOFF}$, LP, FR, MD

Fig.1 Input Circuit(1)



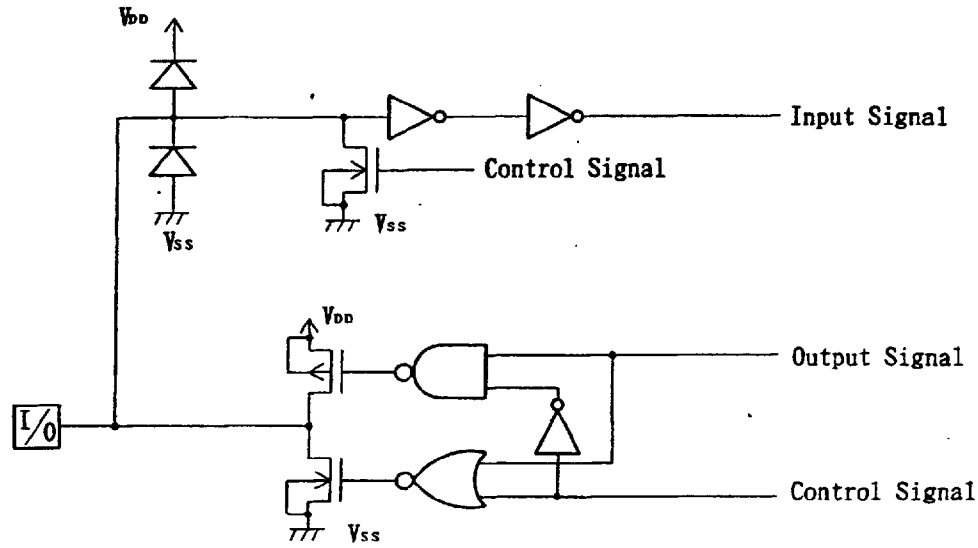
【Applicable pins】
DI_7, XCK

Fig.2 Input Circuit(2)



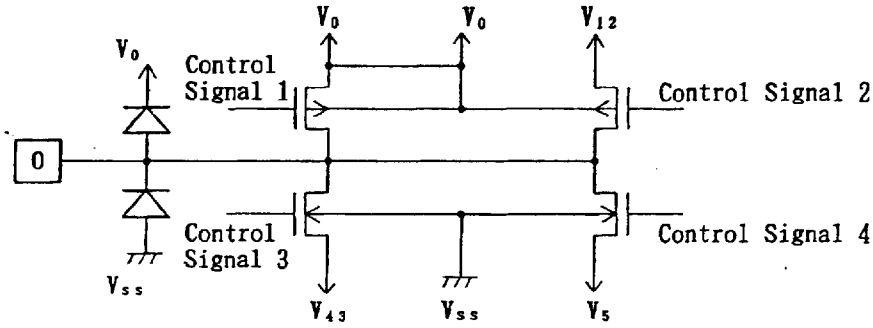
【Applicable pin】
$TEST_1$

Fig.3 Input Circuit(3)



【Applicable pins】
EIO_1, EIO_2

Fig.4 Input/Output Circuit



【Applicable pins】
Y_1 to Y_{240}

Fig.5 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

(Segment mode)

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LC driver voltage bias. ·Normally, the bias voltage used is set by a resistor divider. ·Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_{43} < V_{12} < V_0$. ·To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (i=0, 12, 43, 5).
DI_0-DI_7	Input Pin for display data ·In 4-bit parallel input mode, input data into the 4 pins DI_0-DI_3. Connect DI_4-DI_7 to V_{SS} or V_{DD}. ·In 8-bit parallel input mode, input data into the 8 pins DI_0-DI_7.
XCK	Clock input pin for taking display data ·Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data ·Data is latched on the falling edge of the clock pulse.
L/R	Direction selection pin for reading display data ·When set to V_{SS} level "L", data is read sequentially from Y_{240} to Y_1. ·When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input pin for output deselect level ·The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. ·When set to V_{SS} level "L", the LC drive output pins (Y_1-Y_{240}) are set to level V_5. ·While set to "L",the contents of the line latch are reset,but read the display data in the data latch regardless of condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is canceled,the driver outputs deselect level (V_{12} or V_{43}),then outputs the contents of the date latch on the next falling edge of the LP. That time,if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics (Page 21),can not output the reading data correctly.
FR	AC signal input for LC driving waveform ·The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. ·Normally,inputs a frame inversion signal. ·The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in 7-2-1.
MD	Mode selection pin ·When set to V_{SS} level "L", 8-bit parallel input mode is set. ·When set to V_{DD} level "H", 4-bit parallel input mode is set. ·The relationship between the display data and driver output pins is shown in 7-2-2.

Symbol	Function
S/C	Segment mode/common mode selection pin •When set to V_{DD} level "H", segment mode is set.
EIO_1 EIO_2	Input/Output pin for chip selection •When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. •When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. •During output, set to "H" while LP*$\overline{XCK}$ is "H" and after 240-bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". •During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected.
$TEST_1$	Test mode select pin. •During normal operation, tie to V_{SS} level "L".
Y_1-Y_{240}	LC driver output pins •Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. Table of truth values is shown in 7-2-1.

(Common mode)

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V.
V_{SS}	Ground pin connects to 0 V.
V_{0R},V_{0L} V_{12R},V_{12L} V_{43R},V_{43L} V_{5R},V_{5L}	Power supply pin for LC driver voltage bias. •Normally, the bias voltage used is set by a resistor divider. •Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$. •To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (i=0, 12, 43, 5).
EIO_1	Bidirectional shift register shift data input/output pin •Output pin when L/R is at V_{SS} level "L", input pin when L/R is at V_{DD} level "H". •When EIO_1 is used as input pin, it will be pull-down. •When EIO_1 is used as output pin, it won't be pull-down.
EIO_2	Bidirectional shift register shift data input/output pin •Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". •When EIO_2 is used as input pin, it will be pull-down. •When EIO_2 is used as output pin, it won't be pull-down.
LP	Bidirectional shift register shift clock pulse input pin •Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection pin •Data is shifted from Y_{240} to Y_1 when set to V_{SS} level "L", and data is shifted from Y_1 to Y_{240} when set to V_{DD} level "H".

$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •When set to V_{SS} level "L", the LC driver output pins (Y_1-Y_{240}) are set to level V_5. •While set to "L",the contents of the shift resister are reset not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), and the shift data is reading on the falling edge of the LP. That time,if $\overline{DISPOFF}$ removal time can not keep regulation what is shown AC characteristics (Page 25), the shift data is not reading correctly.
FR	AC signal input for LC driving waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •Normally, input a frame inversion signal. •The LC driver output pin's output voltage level can be set using the shift register output signal and the FR signal. Table of truth values is shown in 7-2-1.
MD	Mode selection pin •When set V_{SS} level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DI_7	Dual Mode data input pin •According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used as Dual Mode, DI_7 will be pull-down. When the chip is used as Single Mode, DI_7 won't pull-down.
S/C	Segment mode/common mode selection pin •When set to V_{SS} level "L", common mode is set.
DI_0-DI_6	Not used •Connect DI_0-DI_6 to V_{SS} or V_{DD}. Avoiding floating.
XCK	Not used •XCK is pull-down in common mode, so connect to V_{SS} or open.
$TEST_1$	Test mode select pins •During normal operation, tie to V_{SS} level "L".
Y_1-Y_{240}	LC driver output pins •Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5)is selected and output. Table of truth values is shown in 7-2-1.

7-2. Functional Operations

7-2-1. Truth Table

(Segment Mode)

FR	Latch Data	DISPOFF	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
x	x	L	V_5

Here, $V_{ss} \leq V_5 < V_{43} < V_{12} < V_0$, H : V_{DD}(+2.5 to +5.5 V), L : V_{ss}(0 V),
x : Don't care

(Common Mode)

FR	Latch Data	DISPOFF	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
x	x	L	V_5

Here, $V_{ss} \leq V_5 < V_{43} < V_{12} < V_0$, H : V_{DD}(+2.5 to +5.5 V), L : V_{ss}(0 V),
x : Don't care

【Note】There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin.
That time "Don't care" should be fixed to "H" or "L", avoiding floating.

7-2-2. Relationship between the Display Data and Driver Output pins

(Segment Mode)

(a) 8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock: 30clock	29clock	28clock	..	3clock	2clock	1clock
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	..	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	..	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	..	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	..	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}	..	Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}	..	Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}	..	Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}	..	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	..	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	..	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	..	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	..	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	..	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	..	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	..	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	..	Y_{17}	Y_9	Y_1

(b) 4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock: 60clock	59clock	58clcok	..	3clock	2clock	1clock
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	..	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	..	Y_{230}	Y_{234}	Y_{228}
				DI_2	Y_3	Y_7	Y_{11}	..	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	..	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	..	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	..	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	..	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	..	Y_9	Y_5	Y_1

(Common Mode)

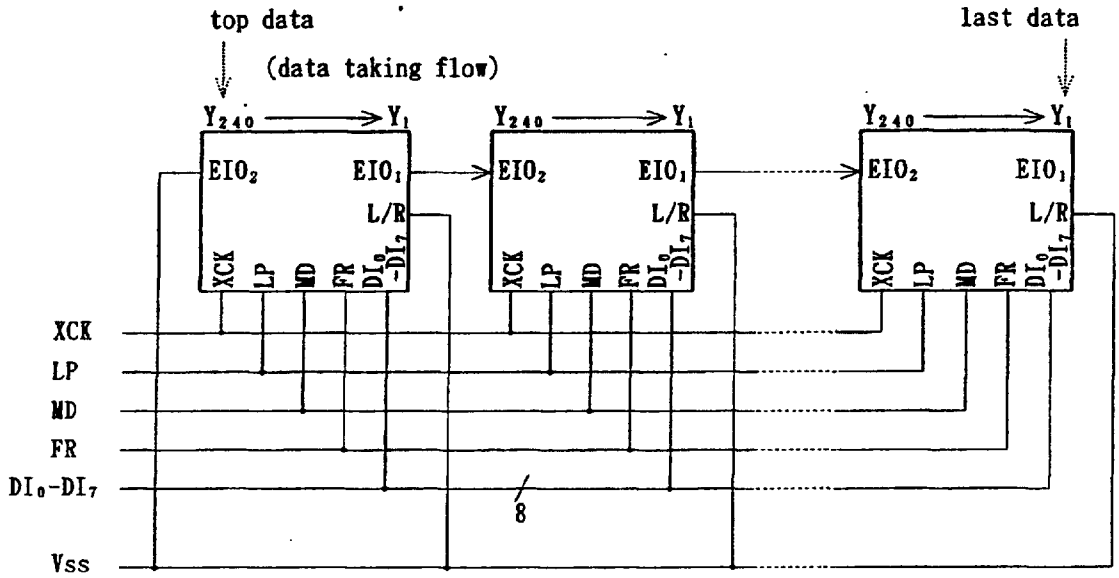
MD	L/R	Data Transfer Direction	EIO_1	EIO_2	DI_7
L (Single)	L(shift to left)	$Y_{240} \rightarrow Y_1$	Output	Input	x
	H(shift to right)	$Y_1 \rightarrow Y_{240}$	Input	Output	x
H (Dual)	L(shift to left)	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Inpout	Output	Input

Here, L:V_{SS}(0 V), H:V_{DD}(+2.5V to +5.5 V), x:Don't Care

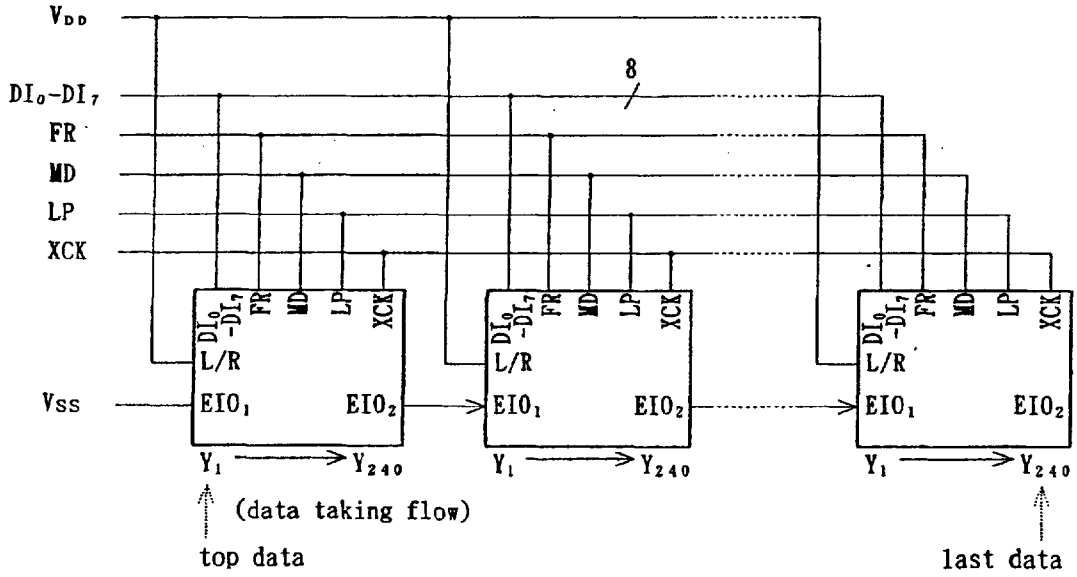
【Note】 "Don't care" should be fixed to "H" or "L", avoiding floating.

7-2-3. Connection Examples of Plural Segment Drivers

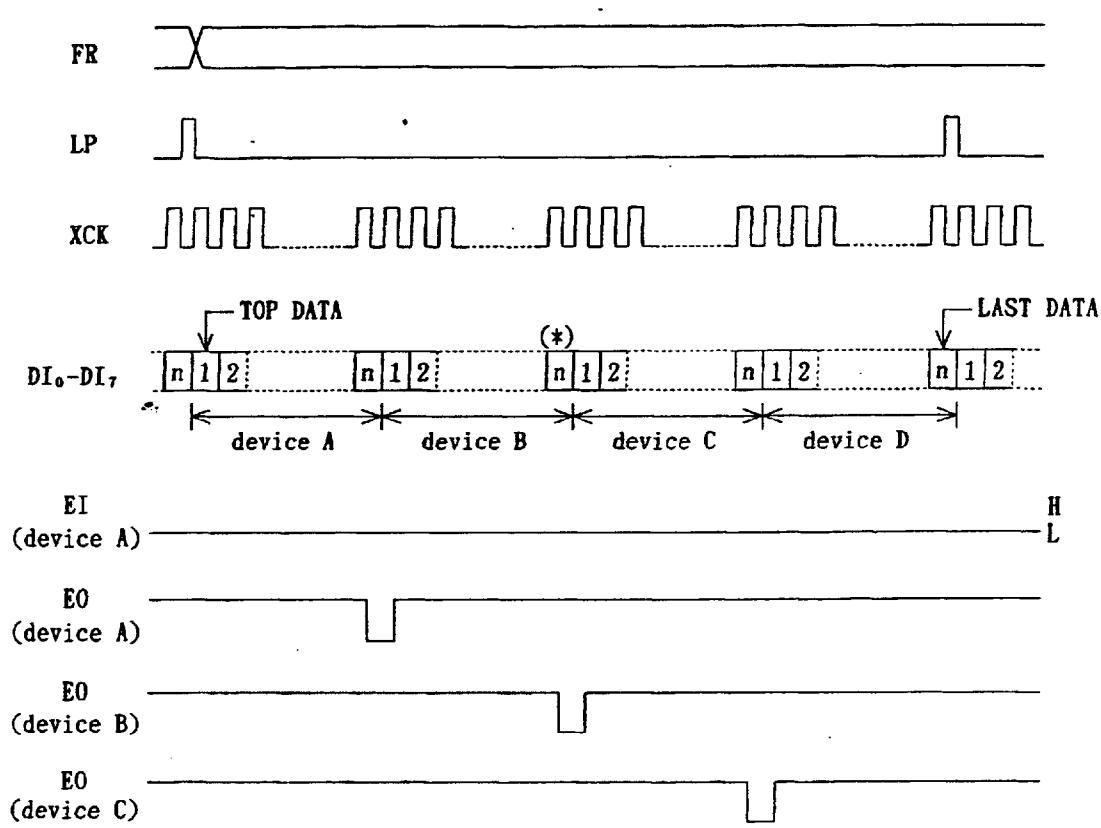
(a) Case of L/R="L"



(b) Case of L/R="H"



7-2-4. Timing Chart of 4-Device cascade Connection of Segment Drivers



(*) n : 4-bit parallel mode 60
8-bit parallel mode 30

7-2-5. Connection Examples for Plural Common Drivers

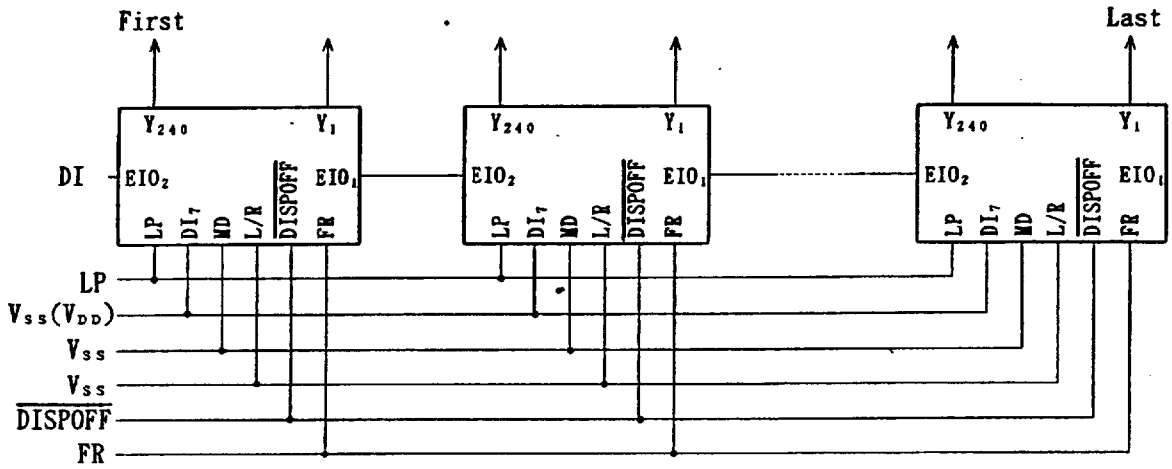


Fig. 1 Single Mode (Shifting toward left)

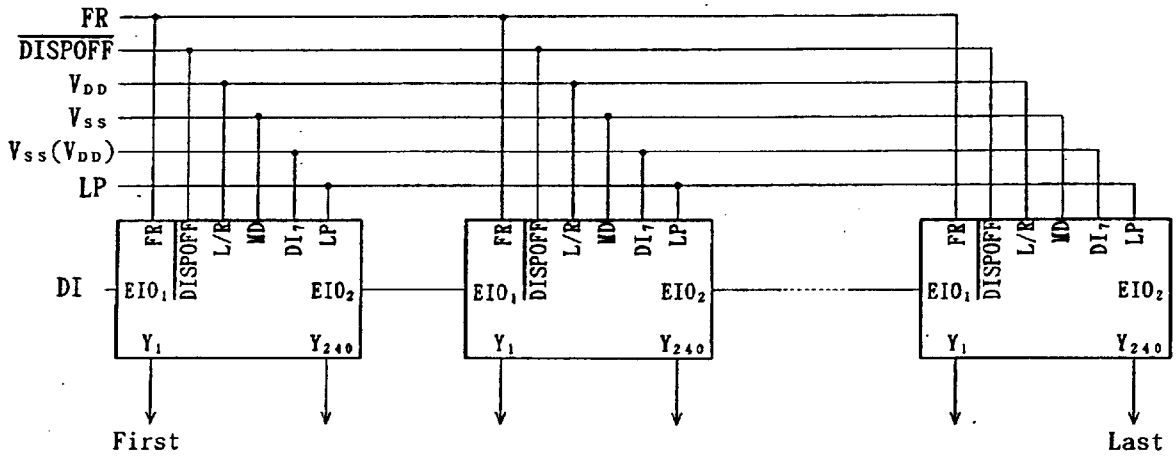


Fig. 2 Single Mode (Shifting toward right)

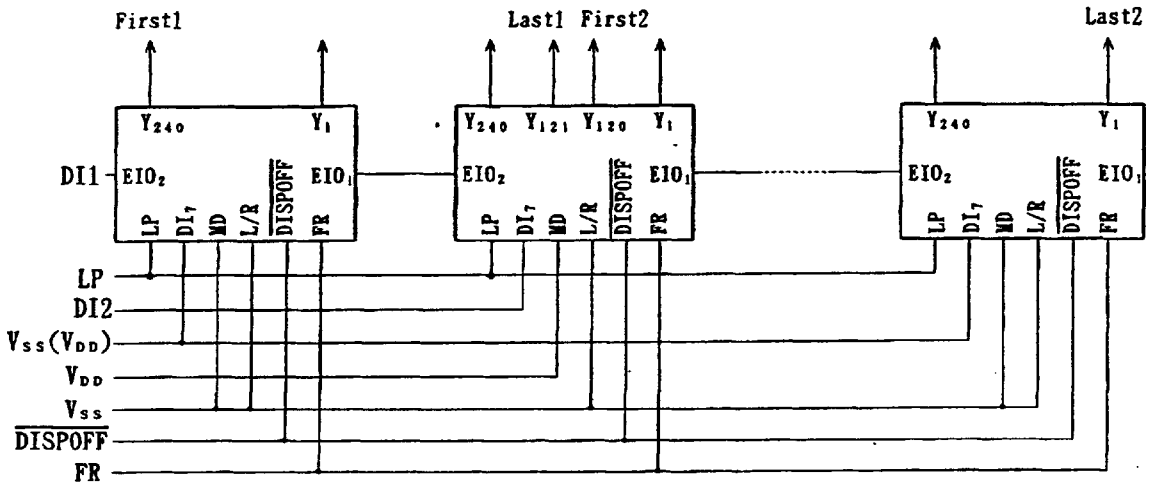


Fig. 3 Dual Mode (Shifting toward left)

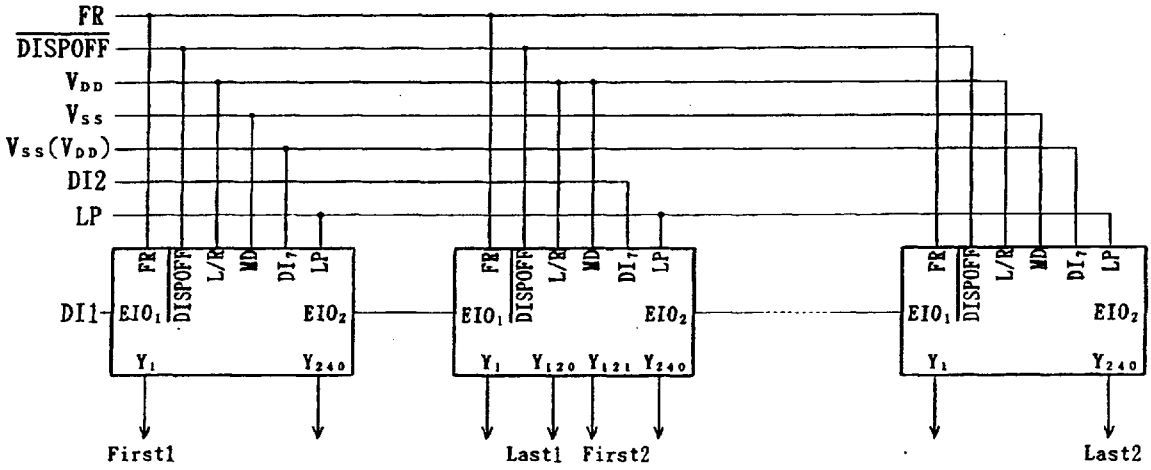


Fig. 4 Dual Mode (Shifting toward right)

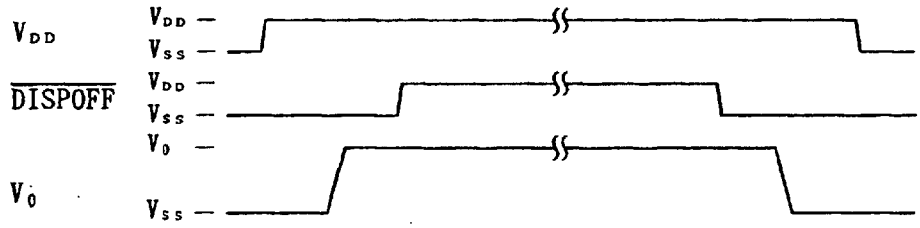
8. Precaution

○Precaution when connecting or disconnecting the power

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor(50~100 Ω) or fuse to the LC drive power V_0 of the system as a current limitter. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_S on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0	Referenced to V_{SS} (0 V)	V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$, $TEST_1$	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS} (0 V)	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15.0		+42.0	V
Operating temperature	T_{opr}			-20		+85	℃

【Note】Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$

11. Electrical Characteristics

11-1. DC Characteristics

(Segment Mode)

(V_{SS}=V_S=0 V, V_{DD}=+2.5 V to +5.5 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DI_{0-7}, XCK, LP, L/R	0.8V_{DD}			V
	V_{IL}		FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	DI_{0-7}, XCK, LP, L/R			+10.0	μA
	I_{LIL}	V_I=V_{SS}	FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			-10.0	μA
Output resistance	R_{ON}	|ΔV_{ON}|=0.5 V, V_0=+40.0 V	Y_1-Y_{240}		1.0	1.5	kΩ
		|ΔV_{ON}|=0.5 V, V_0=+30.0 V			1.5	2.0	
		|ΔV_{ON}|=0.5 V, V_0=+20.0 V			2.0	2.5	
Stand-by current	I_{STB}	*1	V_{SS}			75.0	μA
Consumed current(1) (Deselection)	I_{DD1}	*2	V_{DD}			2.0	mA
Consumed current(2) (Selection)	I_{DD2}	*3	V_{DD}			12.0	mA
Consumed current	I_0	*4	V_0			1.5	mA

【Note】

*1 V_{DD}=+5.0 V, V_0=+42.0 V, V_I=V_{SS}

*2 V_{DD}=+5.0 V, V_0=+42.0 V, f_{XCK}=20 MHz, No-load, EI=V_{DD}
The input data is turned over by data taking clock(4-bit parallel input mode)

*3 V_{DD}=+5.0 V, V_0=+42.0 V, f_{XCK}=20 MHz, No-load, EI=V_{SS}
The input data is turned over by data taking clock(4-bit parallel input mode)

*4 V_{DD}=+5.0 V, V_0=+42.0 V, f_{XCK}=20 MHz, f_{LP}=41.6 kHz, f_{FR}=80 Hz, No-load
The input data is turned over by data taking clock(4-bit parallel input mode)

(Common Mode)

(V_{SS}=V_S=0 V, V_{DD}=+2.5 V to +5.5 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	$DI_{0\sim6}$, LP, L/R, FR, MD, S/C, $\overline{DISPOFF}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}	$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			-10.0	μA
Input pull-down current	I_{PD}	V_I=V_{DD}	XCK, EIO_1, EIO_2, DI_7			100.0	μA
Output resistance	R_{ON}	|ΔV_{ON}|=0.5 V, V_0=+40.0 V	Y_1-Y_{240}		1.0	1.5	kΩ
		|ΔV_{ON}|=0.5 V, V_0=+30.0 V			1.5	2.0	
		|ΔV_{ON}|=0.5 V, V_0=+20.0 V			2.0	2.5	
Stand-by current	I_{STB}	*1	V_{SS}			75.0	μA
Consumed current(1)	I_{DD}	*2	V_{DD}			120.0	μA
Consumed current(2)	I_0	*2	V_0			240.0	μA

*1 V_{DD}=+5.0 V, V_0=+42.0 V, V_I=V_{SS}

*2 V_{DD}=+5.0 V, V_0=+42.0 V, f_{LP}=41.6 kHz, f_{FR}=80 Hz
case of 1/480 duty operation, No-load

11-2. AC Characteristics

(Segment Mode 1)

(V_{SS}=V_S=0 V, V_{DD}=+4.5 V to +5.5 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r, t_f≦10 ns	50			ns
Shift clock "H" pulse width	t_{WCKH}		15			ns
Shift clock "L" pulse width	t_{WCKL}		15			ns
Data setup time	t_{DS}		10			ns
Data hold time	t_{DH}		12			ns
Latch pulse "H" pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift pulse fall time	t_{LH}		25			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_S		10			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			μs
Output delay time (1)	t_D	C_L=15 pF			30	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	μs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	μs

【Note】

*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 2)

(V_{SS}=V_S=0 V, V_{DD}=+3.0 V to +4.5 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r, t_f≦10 ns	66			ns
Shift clock "H" pulse width	t_{WCKH}		23			ns
Shift clock "L" pulse width	t_{WCKL}		23			ns
Data setup time	t_{DS}		15			ns
Data hold time	t_{DH}		23			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		50			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift pulse fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_S		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			μs
Output delay time (1)	t_D	C_L=15 pF			41	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	μs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	μs

【Note】

*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 3)

(V_{SS}=V_S=0 V, V_{DD}=+2.5 V to +3.0 V, V_0=+15.0 to +42.0 V, Ta=-20 to +85 ℃)

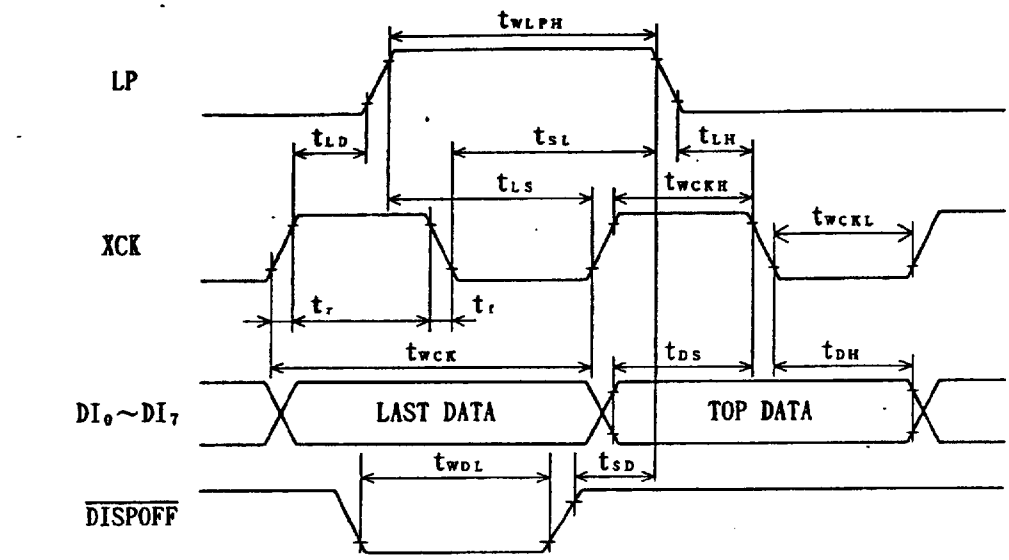
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r, t_f≦10 ns	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ns
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		20			ns
Data hold time	t_{DH}		23			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		65			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift pulse fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_S		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_D	C_L=15 pF			57	ns
Output delay time (2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	µs
Output delay time (3)	t_{pd3}	C_L=15 pF			1.2	µs

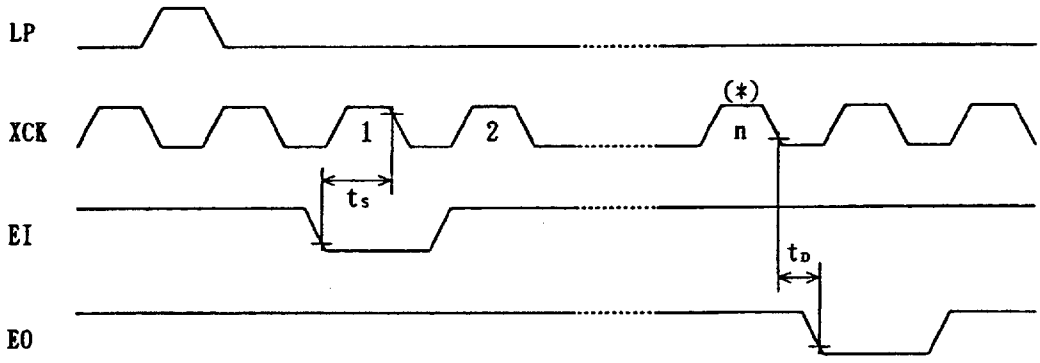
【Note】

*1 Take the cascade connection into consideration.

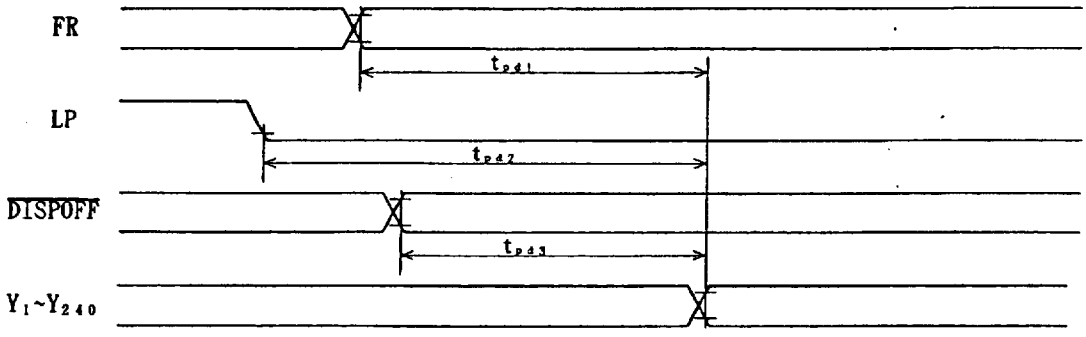
*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Timing characteristics of Segment Mode)





(*) n :4-bit parallel mode 60
8-bit parallel mode 30

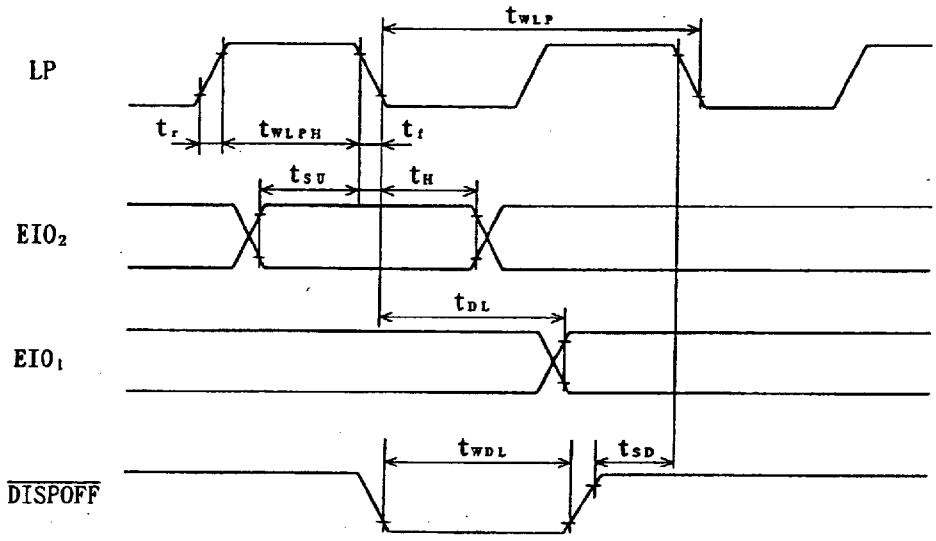


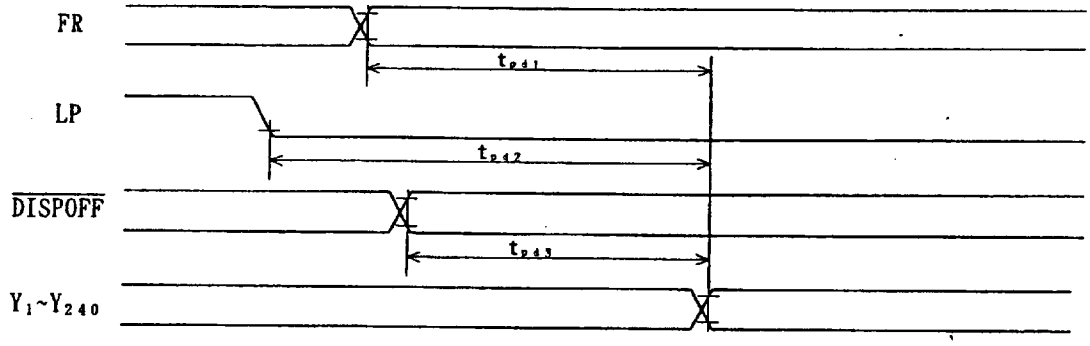
(Common Mode)

(V_{SS}=V_S=0 V, V_{DD}=+2.5 to +5.5 V, V0=15.0 to+42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	t_r, t_f≤20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=+5.0 V±10%	15			ns
		V_{DD}=+2.5 V~+4.5 V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2			µs
Output dalay time(1)	t_{DL}	C_L=15 pF			200	ns
Output delay time(2)	t_{pd1}, t_{pd2}	C_L=15 pF			1.2	µs
Output dalay time(3)	t_{pd3}	C_L=15 pF			1.2	µs

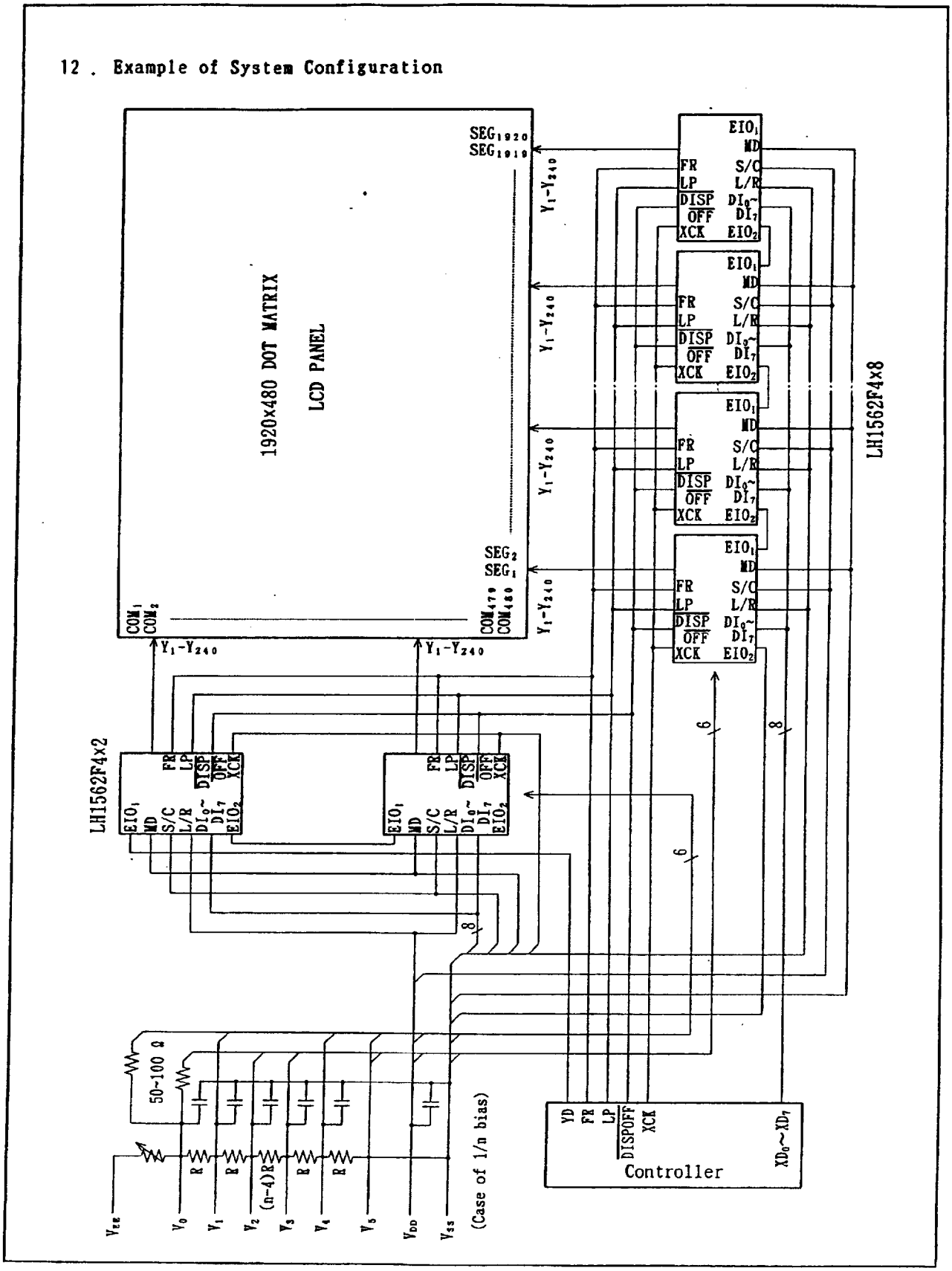
(Timing Characteristics of Common Mode)





[L/R="L"]

12 . Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V		10		ns

14. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPS6581-00
2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.
   (1) Date code (example) : 7 (a) 28 (b) D (c) 0 (d)
   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes factory code (of production)
   d) denotes the number of times of alteration
3. Packing Specifications
   3-1 Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405 mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μ mt)	Protects device and prevents ESD (Electro Static Discharge)
Aluminum laminated bag	(520×600 mm)	Moisture proof.
Adhesive tape paper		Fixing of tape carrier package and separator.
Label	Paper	Indicates production name, lot.No., and quantity.
Desiccant	Silica gel	Drying of device
Inner carton	Cardboard(420×420×85mm)	Contains a reel.
Outer carton	Cardboard(445×285×450mm)	Contains 3 inner cartons.

   3-2 Packing Form
   a) Tape carrier package(TCP)is wound on a reel with separator and the ends of them are fixed with adhesive tape.
   b) A label indicating production name, lot number and quantity is stuck on one side of the reel.
   c) The reel and silica gel are put in a laminated aluminum bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the inner carton.
   d) 3 inner cartons are put in an outer carton and the same label(b) is affixed to one side of the outer carton.

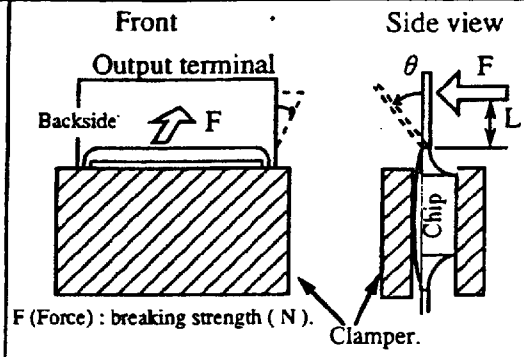
   * Specification of label

TYPE	
	Production name Lot No.
QUANTITY	Quantity
LOT(DATE)	Shipping date

   3-3 Other
   (1) The length of the TCP is typically 40 m per reel, but this may change in accordance with the inventory quantity.
   (2) Faulty devices is completely punched out at the part of the device.
   (3) The maximum number of continuous faulty devices is 9.

ISSUE DATE	NOV. 6, 1997	APPROVE	T. Akagi	(NOTE)
ISSUE NUMBER	H9Y001	CHECK	A. Honda	
S/C NUMBER		DESIGN	K. Fukuta	

4. Cautions concerning handling.
Although the strength of the device has been verified in accordance with the test method shown below, do not subject the resin parts or the slit terminals to any excessive bending or pressure.

Test	Test method	Rating
Flexure test		Indicate as moment M. M=F×L (N·m) M=1.47×10^{-3} N·m MAX. (for both +θ and -θ)

5. Cautions concerning storage.
- When storing the product, it is recommended that it be left in its shipping package. After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
- Storage conditions

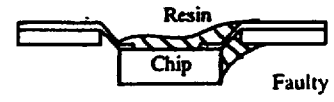
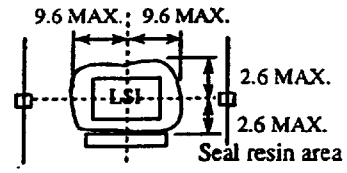
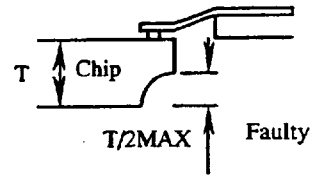
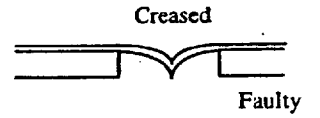
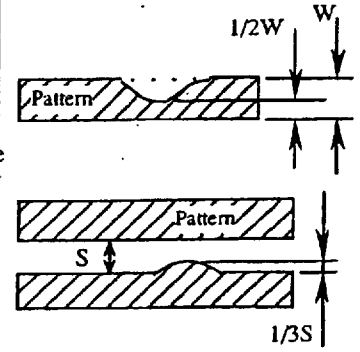
Storage state	Storage conditions
Unopened(less than 60 days)	Temperature: 5 to 30℃, humidity : 80% RH or less.
After seal of broken(less than 30 days)	Temperature: 25℃, humidity : 15% RH or less, dry nitrogen atmosphere.

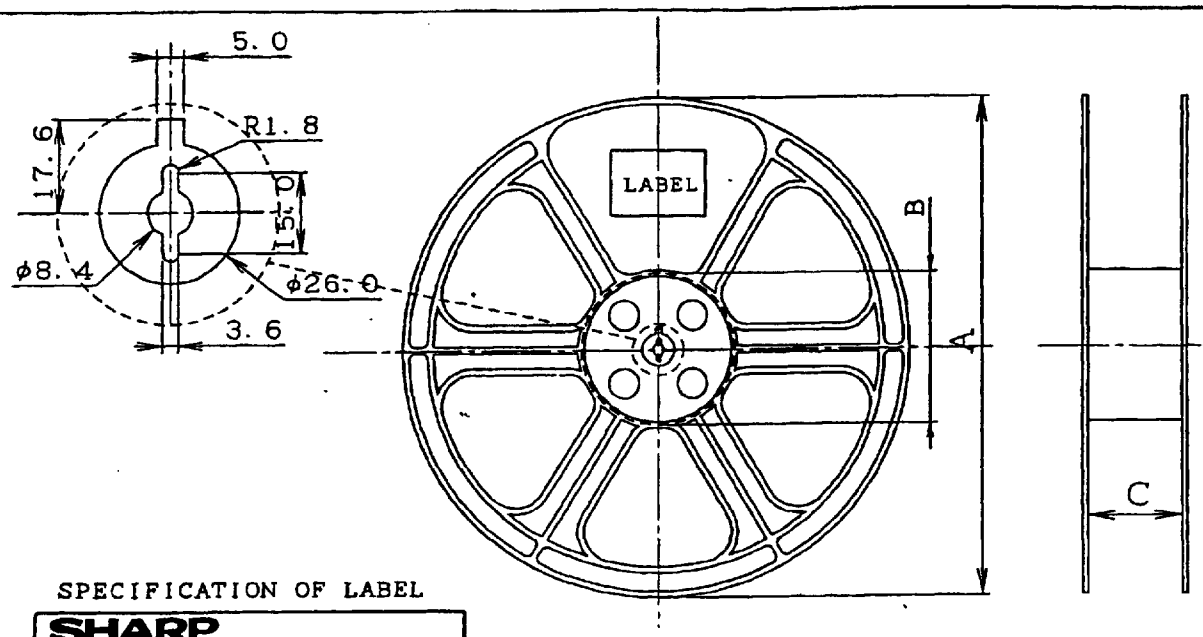
- Don't store in a location exposed to corrosive gas or excessive dust.
- Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.
- Don't store the product such that it subjected to an excessive load weight, such as by stacking.
- Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.

6. Other cautions.
- Immediately after opening the moisture-proof packing, the measurement will shrink slightly. In order to return the measurements to those shown in the drawing, it is necessary to store the product for at least 48 hours at a temperature of 20 to 25℃ and humidity of 50 to 60%.
- When soldering TCP, the TCP wiring pattern may become corroded if non-reacted halogen remains within the flux deposited on the TCP. Therefore, avoid applying flux to areas other than the part to be soldered, and ensure that no solvent remains in the flux after mounting.
Avoid using flux containing highly concentrated .

7. External appearance inspection

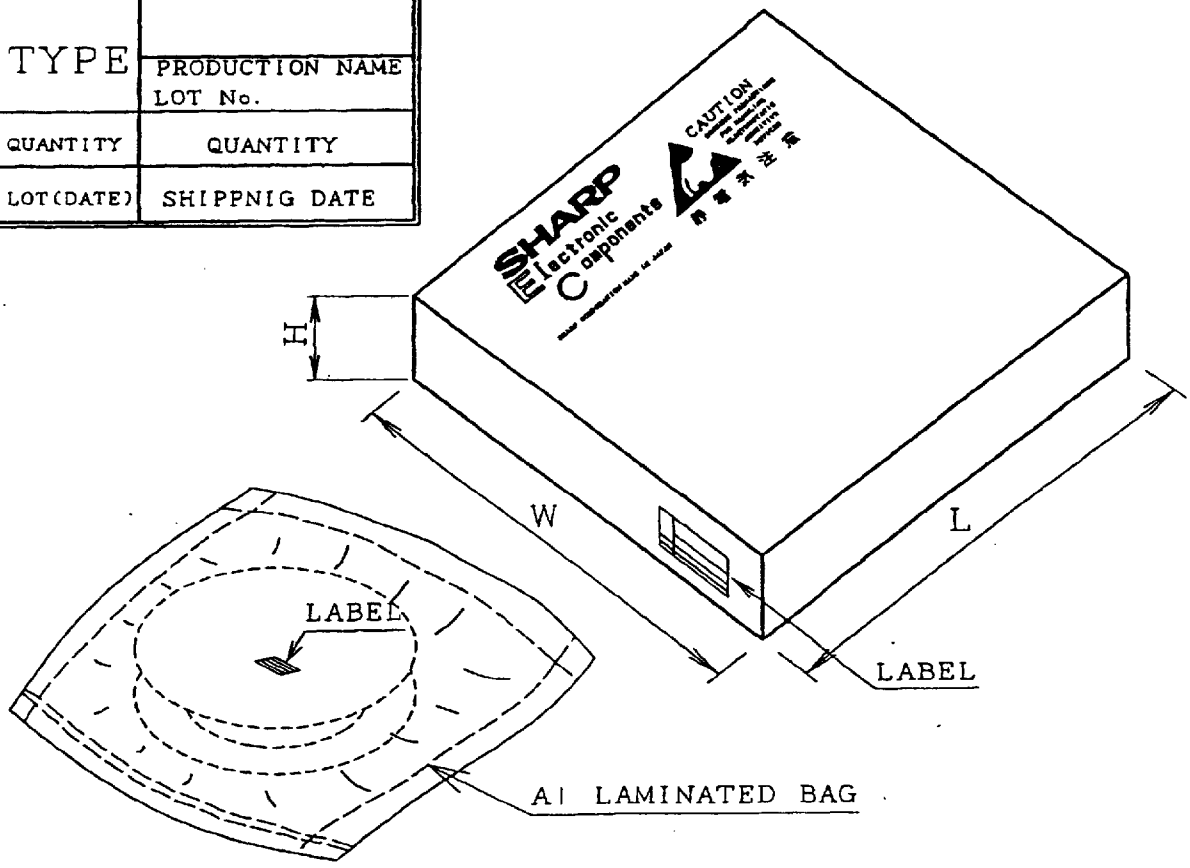
The standards for the inspection of the external appearance of the package are shown below.

Item	Inspection standards	Remarks
1. Exposure of the inner leads and device holes	·Faulty if the chip or inner leads are completely exposed. ·Faulty if the device holes are not completely filled with resin.	
2. Air bubbles	·Faulty if there are air bubbles extending as far as the surface of the chip. ·Faulty if there are air bubbles at the inner leads.	
3. Seal resin area	·Faulty if the area of the seal resin area exceeds the specifications.	Upper side:19.2×5.20mmMAX Underside:19.2×5.20mmMAX
4. Seal resin thickness	·Faulty if the thickness of the device exceeds the specifications.	Upper side:0.30 mm MAX. Underside:0.75 mm MAX. Total thickness:1.20 mm MAX.
5. Adherence of resin or foreign matter except the seal resin area.	·Faulty if any deposits of foreign matter or resin is allowed to bridge the conductor pattern gaps. However, deposits of foreign matter or resin which can be removed easily can be ignored.	
6. Underside of the chip	·Faulty if there are any cracks in the chip. ·Faulty if there is any chipping in the underside of the chip that is lager than one-half the thickness of the chip. ·Faulty if adherence of the resin to the underside of the chip that causes the thickness of the devices exceed the specifications.	
7. Scratches, cracks and chipping in the tape carrier	·Faulty if there are any scratches exposing the substrate (chip, pattern, or inner leads) at the seal resin. ·Faulty if there are holes or scratches which bridge two conductor patterns at the lower part of the applied solder resist. ·Faulty if there are any cracks or chipping at the perforations.	
8. Pattern deformation	·Faulty if the pattern overhanging the slits is markedly deformed	
9. Discoloration	·Faulty if the tin plating is markedly discolored. ·Faulty if the cover coating is markedly discolored.	
10. Markings	·Faulty if the markings are illegible.	
11. Missing parts of output leads	·Faulty if the width of the output lead is reduced to less than one-half of the standard. ·Faulty if copper foil remnants reduce the clearance between the output leads to less than two-thirds of the standards.	
12. Other	·Faulty if there is any warping, twisting, bending, etc., of the tape that would impair use. ·Faulty if there are no indication holes at the non-effective indication holes.	



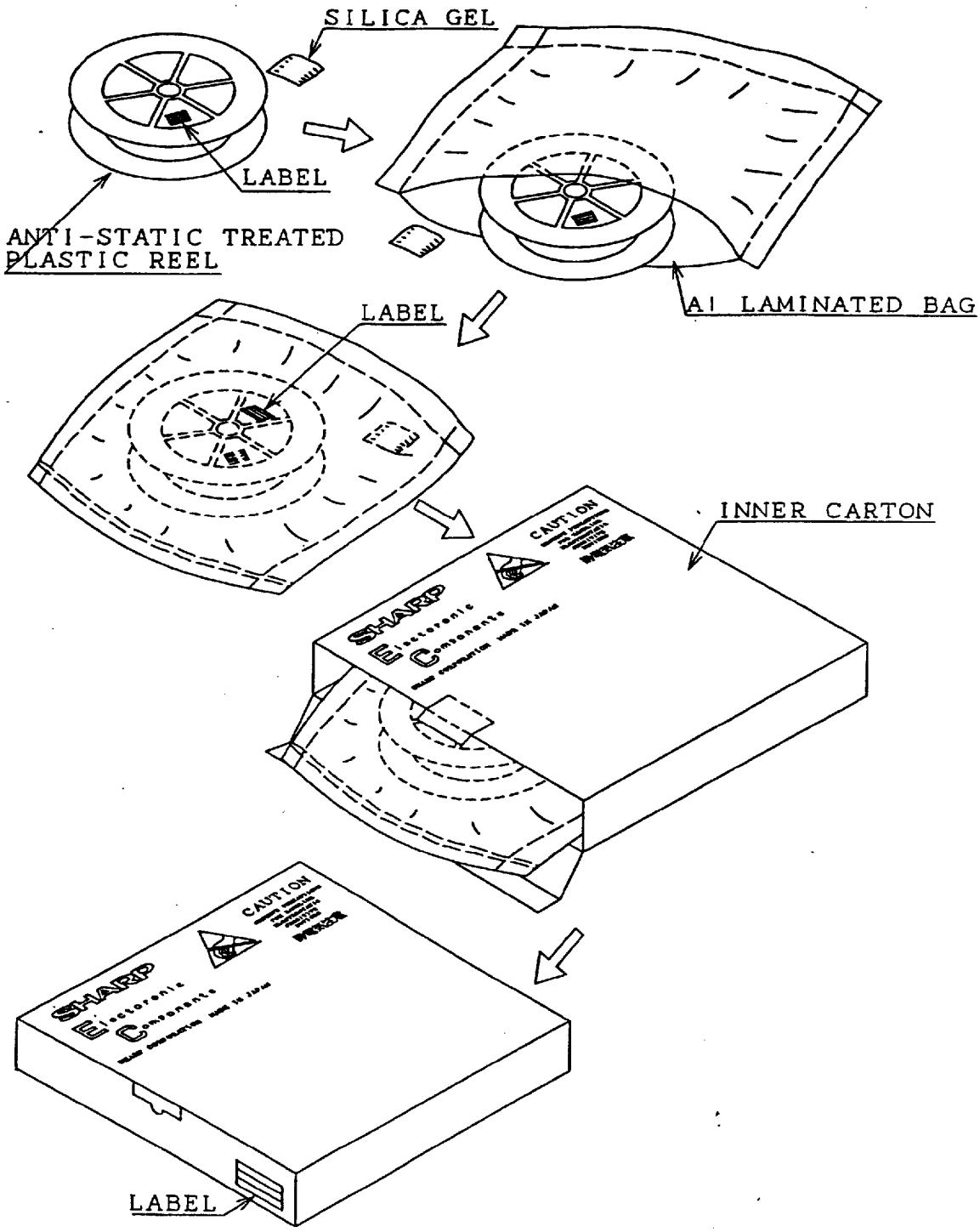
SPECIFICATION OF LABEL

SHARP	
TYPE	
	PRODUCTION NAME LOT No.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPNIG DATE

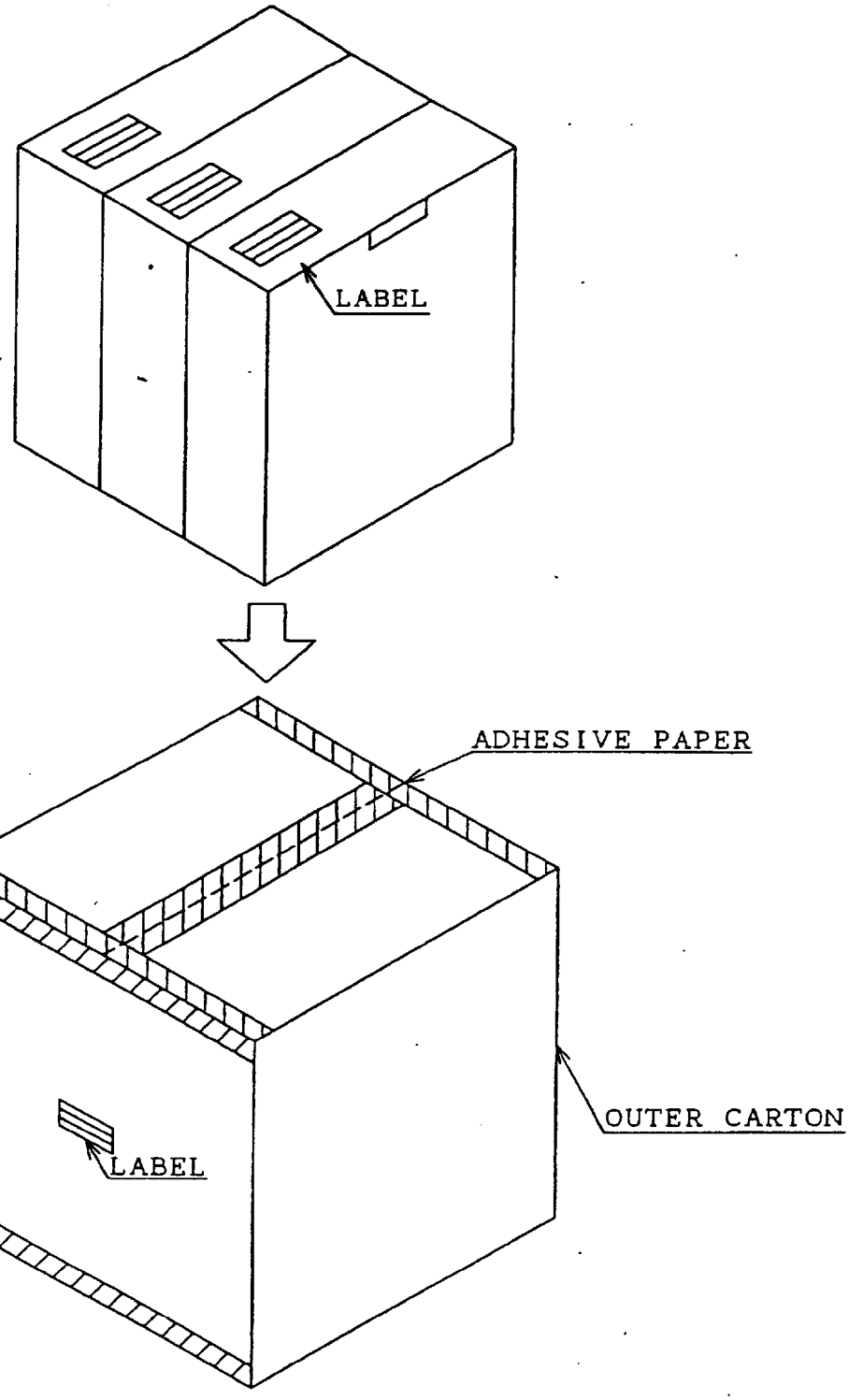


REEL			INNER CARTON			DATE	JAN. 17. 1997	TITLE	REEL AND INNER CARTON OF TCP PACKING
SIZE	A	φ405	SIZE	L	420	UNIT	mm		
	B	φ127		W	420			DRAWING No.	KPS010
	C	71		H	85	DESIGN	T. Kidaguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.	
MATERIAL	ANTI-STATIC TREATED PLASTIC		MATERIAL	CARDBOARD		CHECK	H. Honda	IC FUKUYAMA GROUP	
						APPROVE	T. Tanaka	SHARP CORPORATION	

8180798 0027842 264

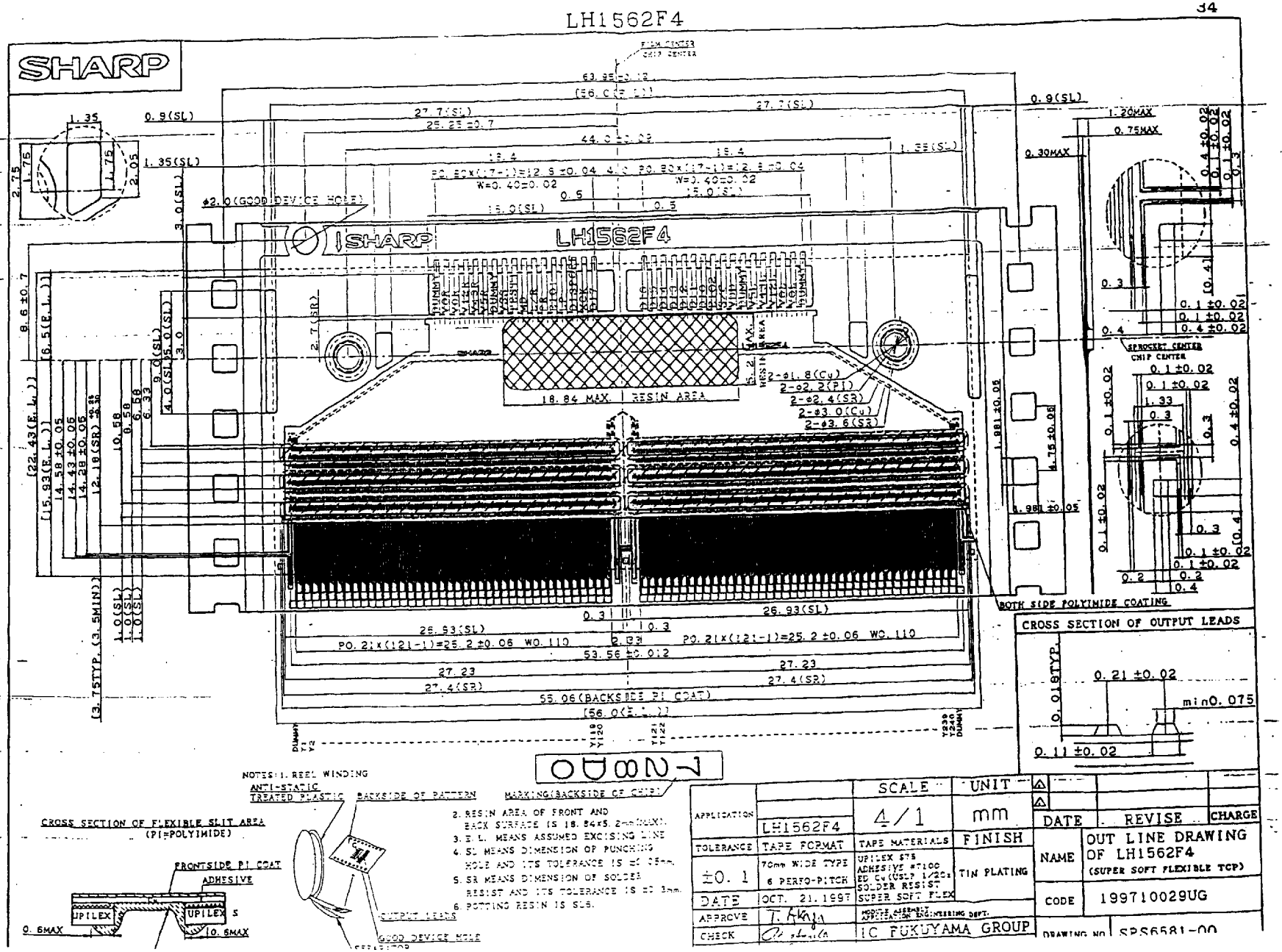


DATE	JANUARY 17, 1997				
ITEM	MATERIAL	NUMBER			
ANTI-STATIC TREATED PLASTIC REEL	ANTI-STATIC TREATED PORYSTYLENE	1 REEL			
DESICCANT	SILICA GEL	10g	TITLE	PACKING VIEW OF TCP (1)	
BAG	ALUMINUM	1 PACK			
LABEL	PAPER	3 PCS			
INNER CARTON	CARDBOARD	1 CASE	CODE		
DESIGN	T. Kidoguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.			
CHECK	G. Honda	IC FUKUYAMA GROUP	DRAWING No		



DATE	JANUARY 17, 1997					
ITEM	MATERIAL	NUMBER				
OUTER CARTON	CARDBOARD	1 CASE				
ADHESIVE TAPE	PAPER					
			TITLE	PACKING VIEW OF TCP (2)		
DESIGN	T. Kidoguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.	CODE			
CHECK	H. Honda	IC FUKUYAMA GROUP				
APPROVE			DRAWING No.			

8180798 0027845 T73



		SCALE	UNIT
APPLICATION	LH1562F4	4/1	mm
TOLERANCE	TAPE FORMAT	TAPE MATERIALS	FINISH
±0.1	70mm WIDE TYPE 6 PERFO-PITCH	UPILEX ST5 ADHESIVE #7100 ED Cu(USLP 1/2oz) SOLDER RESIST SUPER SOFT FLEX	TIN PLATING
DATE	OCT. 21. 1997		
APPROVE	T. Akaji	MOBILE ASSEMBLY APPLICATION ENGINEERING DEPT.	
CHECK		IC FUKUYAMA GROUP	

DATE	REVISE	CHARGE

NAME	OUT LINE DRAWING OF LH1562F4 (SUPER SOFT FLEXIBLE TCP)
CODE	199710029UG
DRAWING NO	SPS6581-00