82C284

T-52-19

Clock Driver and Ready Interface for iAPX 286 Processors

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

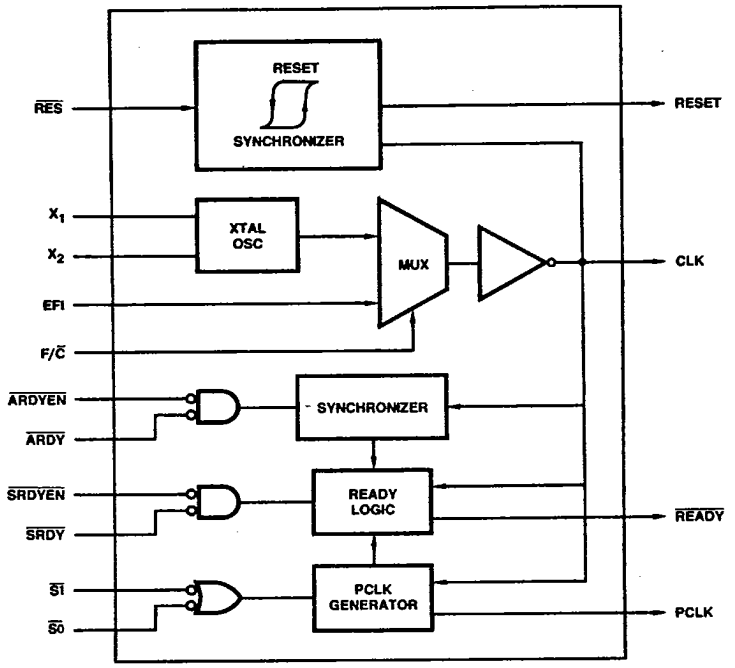
- Generates system clock for iAPX 286 processors
- Uses crystal or TTL signal for frequency source
- Provides local-$\overline{\text{READY}}$ and Multibus*-$\overline{\text{READY}}$ synchronizer
- Functionally identical to bipolar 82284
- Generates system reset output from Schmitt Trigger input
- 18-pin DIPs
- Single +5-volt power supply
- Low-power operation

GENERAL DESCRIPTION

The 82C284 is a clock generator/driver which provides clock signals for iAPX 286 processors and support components.

The device contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources. It also generates a synchronous reset signal from an asynchronous input with hysteresis.

BLOCK DIAGRAM



BD005980

*Multibus is a registered trademark of Intel Corporation.

Order #07747A

Advanced Micro Devices

February 1986

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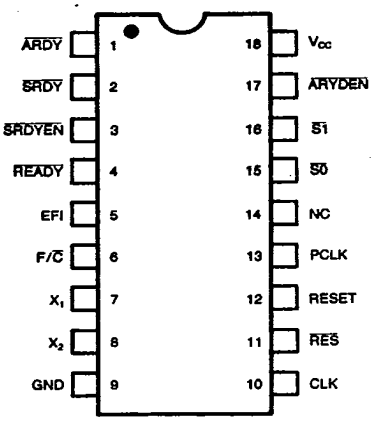
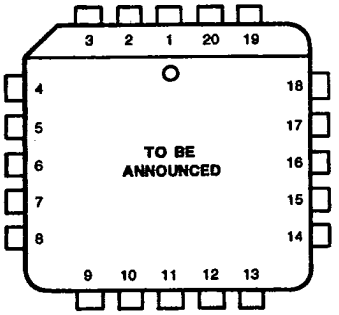
CONNECTION DIAGRAMS
Top View



CD009240



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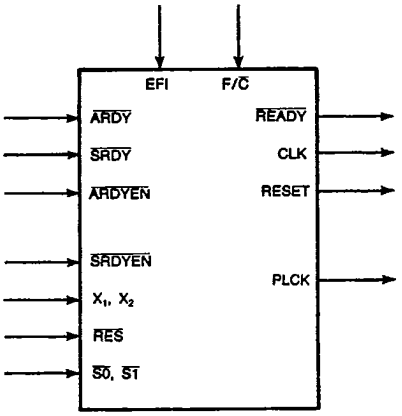
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002260

V_{CC} = Power Supply
GND = Ground

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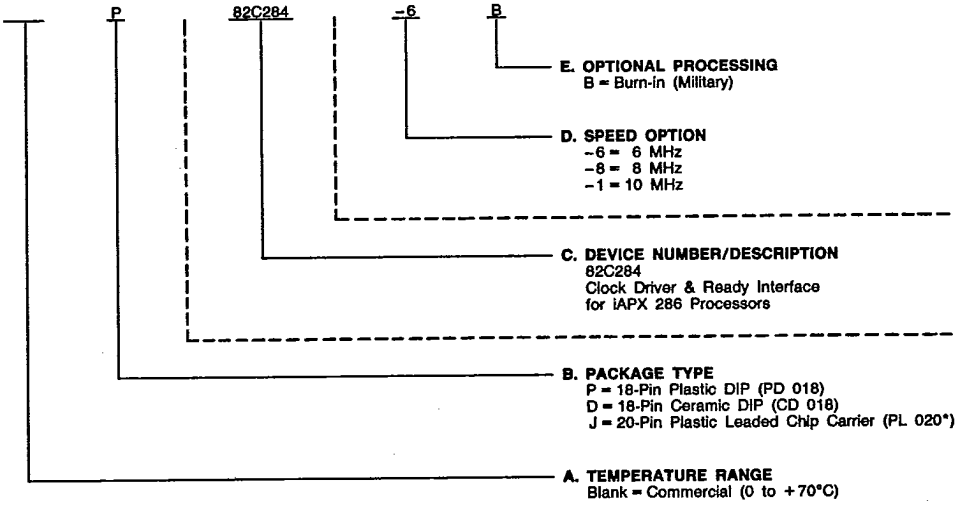
ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Temperature Range
B. Package Type
C. Device Number
D. Speed Option
E. Optional Processing



*To Be Announced.

Valid Combinations		
P, D	82C284	-6, -6B, -8, -8B, -1, -1B

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

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$\overline{ARDY}$ Asynchronous Ready (Input, Active LOW)
$\overline{ARDY}$ is used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to $\overline{ARDY}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

$\overline{SRDY}$ Synchronous Ready (Input, Active LOW)
$\overline{SRDY}$ is used to terminate the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be satisfied for proper operation.

$\overline{SRDYEN}$ Synchronous Ready Enable (Input, Active LOW)
$\overline{SRDYEN}$ qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.

$\overline{READY}$ Ready (Output, Active LOW)
$\overline{READY}$ signals the current bus cycle is to be completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$, and $\overline{RES}$ inputs control $\overline{READY}$ as explained later under Functional Description. $\overline{READY}$ is an open-collector output requiring an external 910-ohm pull-up resistor.

EFI External Frequency In (Input)
The EFI input drives CLK when F/$\overline{C}$ is strapped HIGH. The EFI-input frequency must be twice the processor's internal-clock frequency.

F/$\overline{C}$ Frequency/$\overline{Crystal\ Select}$ (Input)
F/$\overline{C}$ is a strapping option used to select the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal drives CLK. When F/$\overline{C}$ is strapped HIGH, the EFI input drives the CLK output.

X_1, X_2 Crystal In (Input)
These are the pins to which a parallel-resonant, fundamental-mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is strapped LOW, the oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the processor's internal-clock frequency.

CLK System Clock (Output)
CLK output is used by the processor and any support devices which must be synchronized with the processor. The frequency of the CLK output is twice the processor's internal-clock frequency. CLK can drive both TTL- and MOS-level inputs.

$\overline{RES}$ $\overline{Reset\ In}$ (Input, Active LOW)
$\overline{RES}$ generates the system reset signal, RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt Trigger input is provided on $\overline{RES}$ so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

RESET Reset (Output, Active HIGH)
RESET is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW).

PCLK Peripheral Clock (Output)
PCLK is an output which provides a 50% duty cycle clock with one-half the frequency of CLK. PCLK will be in phase with the processor's internal clock following the first bus cycle after the processor has been reset.

$\overline{S0}$, $\overline{S1}$ $\overline{Status}$ (Input, Active LOW)
These inputs prepare the 82C284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pull-up resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.

$\overline{ARDYEN}$ Asynchronous Ready Enable (Input, Active LOW)
$\overline{ARDYEN}$ qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of $\overline{READY}$ for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.

FUNCTIONAL DESCRIPTION

The 82C284 generates the clock, ready, and reset signals required for iAPX 286 processors and support components. The 82C284 is packaged in 18-pin plastic and ceramic DIPs and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready-synchronization logic, and reset-generation logic.

Clock Generator

The CLK output provides the basic timing control for an iAPX 286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When HIGH, the EFI input drives the CLK output.

The 82C284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL-output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see Switching Waveforms). PCLK is forced HIGH when either $\overline{S0}$ or $\overline{S1}$ was active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the 82C284 is a linear Pierce oscillator which requires an external parallel-resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the processor's internal-clock frequency. The crystal should have a typical load capacitance of 32 pF.

X_1 and X_2 are the oscillator-crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Figure 1. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X_1 and X_2 pins. V_{CC} and GND pins should be decoupled as close to the 82C284 as possible.

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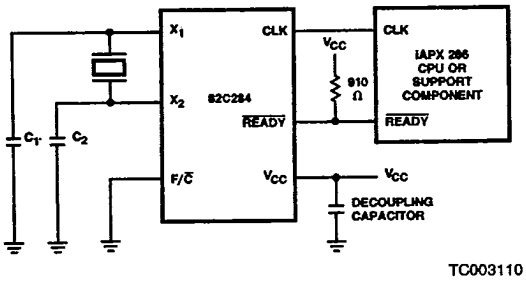

Figure 1. Recommended Crystal and Ready Connections*

*See Table 1 for capacitor values.

TABLE 1. 82C284 CRYSTAL LOADING CAPACITANCE VALUES

Crystal Frequency	C_1 Capacitance	C_2 Capacitance
1 to 8 MHz	60 pF	40 pF
8 to 16 MHz	25 pF	15 pF

Note: Capacitance values must include stray board capacitance.

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see Switching Waveforms). Synchronization of the $\overline{RES}$ input introduces a one- or two-CLK delay before affecting the RESET output.

At power up, a system does not have a stable V_{CC} and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. iAPX 286 processors and support components also require their RESET inputs be HIGH a minimum of sixteen CLK cycles. An RC network (shown in Figure 2) will keep $\overline{RES}$ LOW long enough to satisfy both needs.

A Schmitt Trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH-to-LOW input-transition voltage is lower than the $\overline{RES}$ LOW-to-HIGH input-transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input-transition voltage, the RESET output will make a single transition.

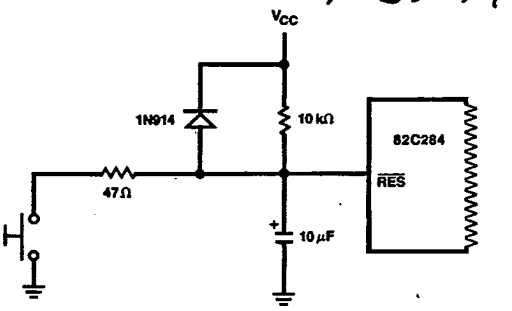

Figure 2. Typical RC $\overline{RES}$ Timing Circuit

Ready Operation

The 82C284 accepts two ready sources for the system-ready signal which terminates the current bus cycle. Either a synchronous ready ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW) if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0, or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0, when sampled by the 82C284 $\overline{READY}$-generation logic. $\overline{READY}$ will remain active for at least two CLK cycles, except when RESET overrides it.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire OR'ed with it, as shown in Figure 1. The $\overline{READY}$ signal of an iAPX 286 system requires an external 910-ohm, ±5% pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see Switching Waveforms).

Figure 3 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 4 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs to have been LOW, $\overline{READY}$ becomes LOW. When both $\overline{ARDY}$ and $\overline{ARDYEN}$ have been resolved as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S (see Figure 4).

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ are sampled LOW, or the ready inputs are sampled as inactive.

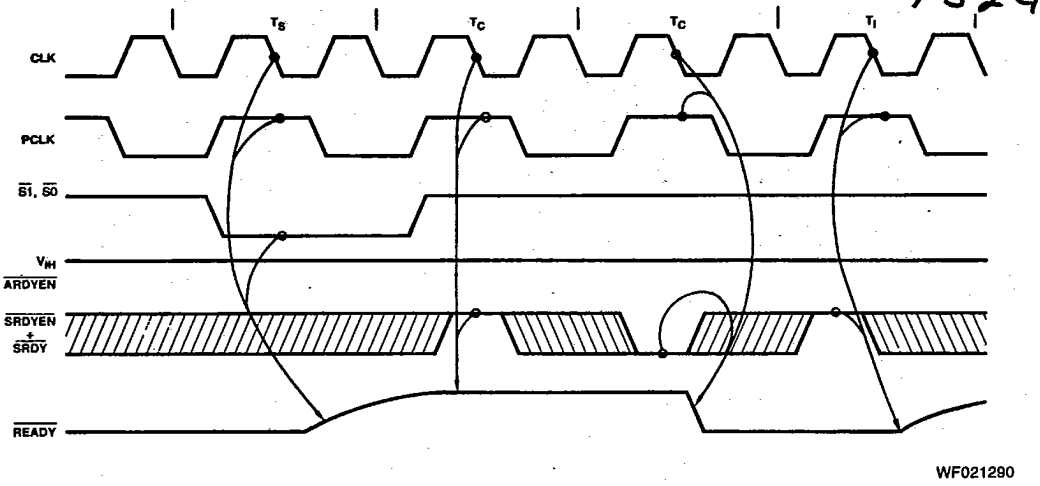

Figure 3. Synchronous Ready Operation

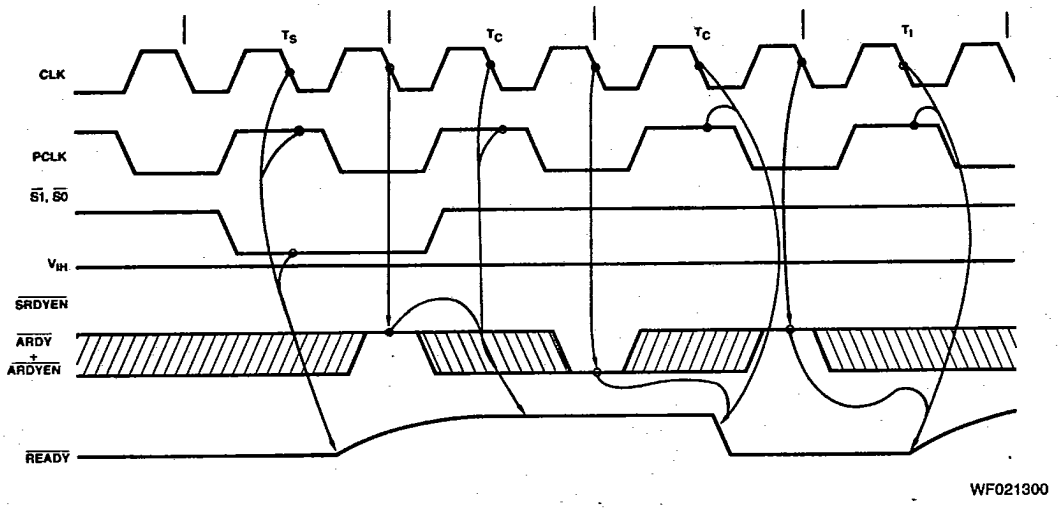

Figure 4. Asynchronous Ready Operation

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
DC Supply Voltage
with Respect to Ground ..... −0.3 to +7.0 V
DC Voltage
with Respect to Ground (Any Pin) ..... −0.3 to +7.0 V
DC Output Current
Into Output (Note 1) ..... +10 mA per pin
Out Of Output (Note 2) ..... −10 mA per pin
DC Input Current ..... ±10 mA per pin

Notes: 1. Except when powered up with outputs LOW.
2. Except when powered up with outputs HIGH.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

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DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage on RESET and PCLK	$I_{OH} = -1$ mA	2.4		V
V_{OL}	Output LOW Voltage on RESET and PCLK	$I_{OL} = 5$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_{IL}	Input LOW Current	$V_F = .45$ V		−0.5	mA
I_{IH}	Input HIGH Current	$V_R = V_{CC}$ Max.		50.0	µA
V_{IHR}	Input HIGH Voltage on $\overline{RES}$		2.6		V
V_{HYS}	Input Hysteresis on $\overline{RES}$		0.25		V
V_{OLR}	Output LOW Voltage on $\overline{READY}$	$I_{OL} = 7$ mA		0.45	V
V_{OLC}	Output LOW Voltage on CLK	$I_{OL} = 5$ mA		0.45	V
V_{OHC}	Output HIGH Voltage on CLK	$I_{OH} = -800$ µA	4.0		V
I_{CCSB}	Standby Power Supply Current	$V_{CC} = 5.5$ V, $V_{IN} = V_{CC}$ or GND; Outputs open			µA
I_{CCOP}	Operating Power Supply Current	$V_{CC} = 5.5$ V, Outputs open			mA/MHz

CAPACITANCE* ($T_A = 25°C$, $V_{CC} = GND = 0$ V, $V_{IN} = +5$ V or GND)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I	Input Capacitance (Note 1)	$F_C = 1$ MHz		10.0	pF

Notes: 1. This specification is provided for reference only.
* Parameters are not "Tested."

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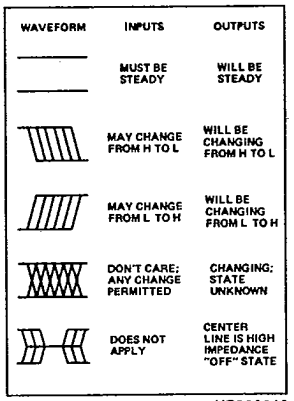
KEY TO SWITCHING WAVEFORMS



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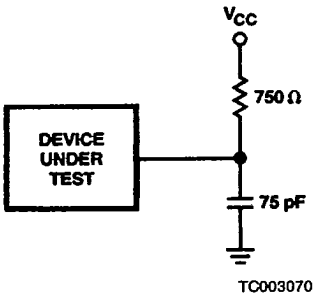
SWITCHING TEST CIRCUITS



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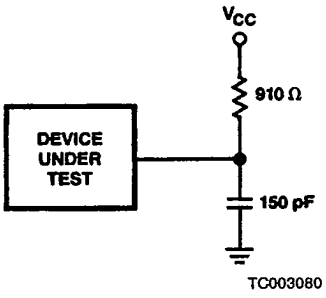
A. PCLK Output



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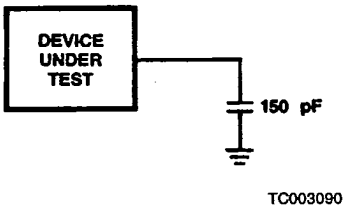
B. $\overline{\text{READY}}$ Output



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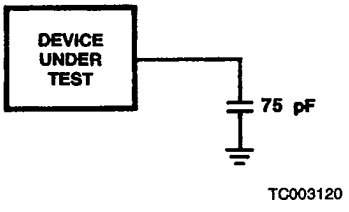
C. CLK Outputs



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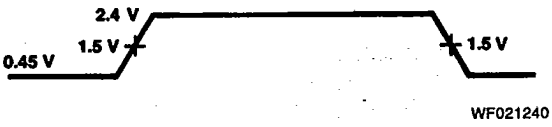
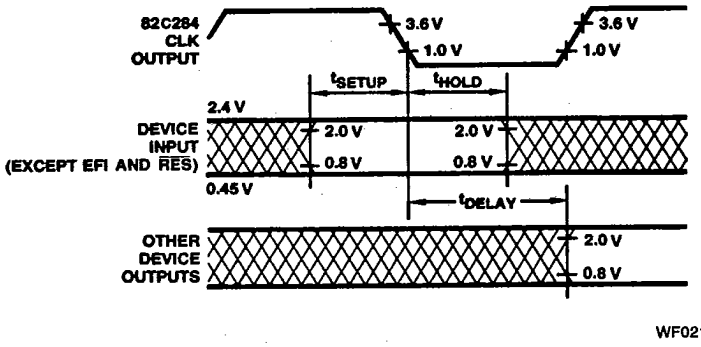
D. RESET Output

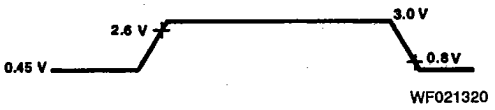
SWITCHING TEST WAVEFORMS



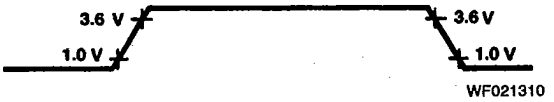
A. EFI Drive and Measurement Points



B. Setup, Hold, and Delay Time Measurement — General



C. $\overline{\text{RES}}$ Drive and Measurement Points



D. CLK Output Measurement Points

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Test Conditions	6 MHz		8 MHz		10 MHz		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_1	EFI-to-CLK Delay	At 1.5 V (Note 1)		35		30			ns
2	t_2	EFI LOW Time	At 1.5 V (Notes 1 & 7)	40		25				ns
3	t_3	EFI HIGH Time	At 1.5 V (Notes 1 & 7)	35		25				ns
4	t_4	CLK Period		83	500	62	500			ns
5	t_5	CLK LOW Time	At 1.0 V (Notes 1, 2 & 8)	20		15				ns
6	t_6	CLK HIGH Time	At 3.6 V (Notes 1, 2 & 8)	25		25				ns
7	t_7	CLK Rise Time	1.0 to 3.6 V (Note 1)		10		10			ns
8	t_8	CLK Fall Time	3.6 to 1.0 V (Note 1)		10		10			ns
9	t_9	Status Setup Time	(Note 1)	28		22				ns
10	t_{10}	Status Hold Time	(Note 1)	1		1				ns
11	t_{11}	$\overline{SRDY}$ or $\overline{SRDYEN}$ Setup Time	(Note 1)	25		17				ns
12	t_{12}	$\overline{SRDY}$ or $\overline{SRDYEN}$ Hold Time	(Note 1)	0		0				ns
13	t_{13}	$\overline{ARDY}$ or $\overline{ARDYEN}$ Setup Time	(Notes 1 & 3)	5		0				ns
14	t_{14}	$\overline{ARDY}$ or $\overline{ARDYEN}$ Hold Time	(Notes 1 & 3)	30		30				ns
15	t_{15}	$\overline{RES}$ Setup Time	(Notes 1 & 3)	25		20				ns
16	t_{16}	$\overline{RES}$ Hold Time	(Notes 1 & 3)	10		10				ns
17	t_{17}	$\overline{READY}$ Inactive Delay	At 0.8 V (Note 4)	5		5				ns
18	t_{18}	$\overline{READY}$ Active Delay	At 0.8 V (Note 4)	0	33	0	24			ns
19	t_{19}	PCLK Delay	(Note 5)	0	45	0	45			ns
20	t_{20}	RESET Delay	(Note 5)	5	50	5	34			ns
21	t_{21}	PCLK LOW Time	(Notes 5 & 6)	$t_4 - 20$		$t_4 - 20$				ns
22	t_{22}	PCLK HIGH Time	(Notes 5 & 6)	$t_4 - 20$		$t_4 - 20$				ns

Notes:
1. CLK loading: C_L = 150 pF.
2. With the internal crystal oscillator using recommended crystal and capacitive loading, or with the EFI input meeting specifications t_2 and t_3. Use a parallel-resonant, fundamental-mode crystal. The recommended crystal loading for CLK frequencies of 8-16 MHz are 25 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.
4. $\overline{READY}$ loading: I_{OL} = 7 mA, C_L = 150 pF. In system application, use 910-ohm ±5% pull-up resistor to meet 80286 timing requirements. For systems which operate faster than 10 MHz, care should be taken to minimize capacitive loading on $\overline{READY}$. The user must insure the RC time constant allows this pin to be pulled HIGH in two clock cycles.
5. PCLK and RESET loading: C_L = 75 pF. PCLK also has 750-ohm pull-up resistor.
6. t_4 refers to any allowable CLK period.
7. When driving the 82C284 with EFI, provide minimum EFI HIGH and LOW times as follows:

CLK Output Frequency	8 MHz CLK	12 MHz CLK	16 MHz CLK*
Minimum required EFI HIGH Time	52 ns	35 ns	25 ns
Minimum required EFI LOW Time		40 ns	

*At CLK frequencies above 12 MHz, CLK output HIGH and LOW times are guaranteed only when using a crystal with recommended capacitive loading per Table 1, not when driving component from EFI. All features of the 82C284 remain functional whether EFI or a crystal is used to drive the 82C284.

8. When using a crystal (with recommended loading capacitance per Table 1) appropriate for the speed of the 80286, CLK output HIGH and LOW times are guaranteed to meet 80286 requirements.

SWITCHING WAVEFORMS

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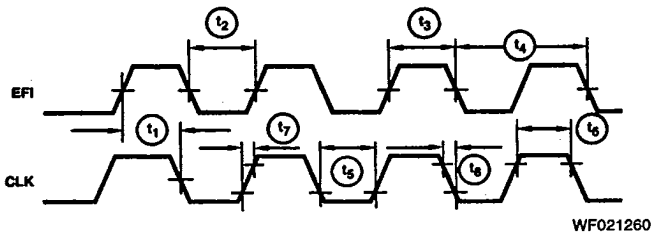

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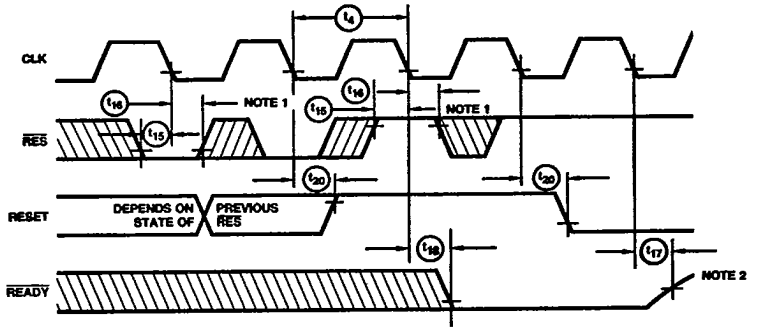
CLK as a Function of EFI

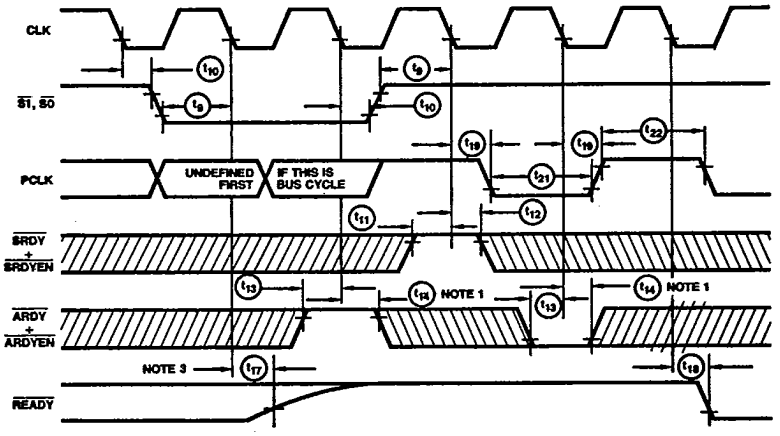
Note: The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.



WF021270

RESET and READY Timing as a Function of RES with S1 and S0 HIGH

Notes: 1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. Tie 910-ohm ±5% pull-up resistor to the READY output. This LOW-to-HIGH transition depends on the state of ARDY, ARDYEN, SRDY, and SRDYEN.



WF021280

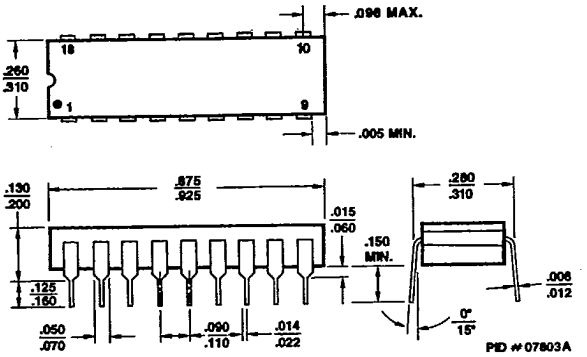
READY and PCLK Timing with RES HIGH

Notes: 1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. Tie 910-ohm ±5% pull-up resistor to the READY output.

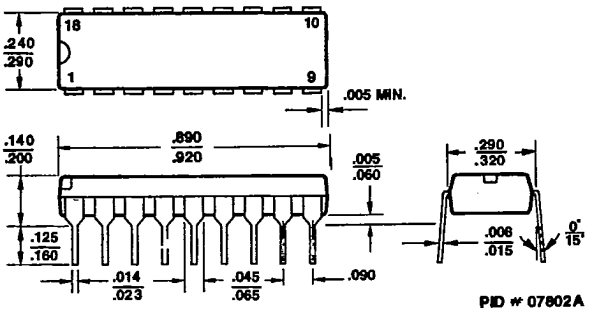
T-52-19

PHYSICAL DIMENSIONS

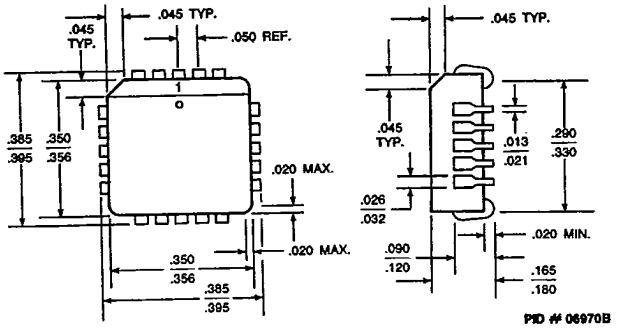
CD 018



PD 018



PL 020*



* Preliminary. Subject to Change.

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