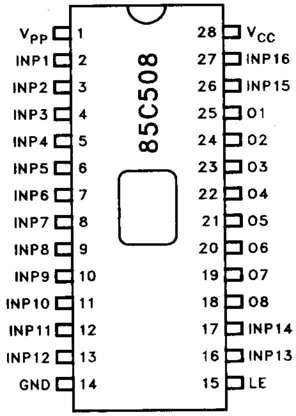
85C508
FAST 1-MICRON CHMOS DECODER/LATCH μPLD

- **High-Performance Programmable Logic Device for High-Speed Microprocessor-to-Memory Decode**
- **Supports Intel386™, i468™, i860™, 80960 Series and Other High-Performance Systems**
- **Extremely High Speed—t_{PD} 7.5 ns (max), 133.3 MHz (max), t_{EO} 4.5 ns (max)**
- **Upgrade Alternative to Fast Bipolar PLDs and Fast MSI Logic**
- **16 Dedicated Inputs for Address/Data Bus Decoding; 8 Latched Outputs; 1 Global Latch Enable**
- **I_{CC} 15 mA Typ., 48 mA Max. @ 50 MHz**
- **100% Generically Testable Logic Array**
- **Available in 28-Pin 300-mil CerDIP/PDIP and PLCC Packages**
  (See Packaging Specifications, Order Number 240800, Package Type D, P, and N)



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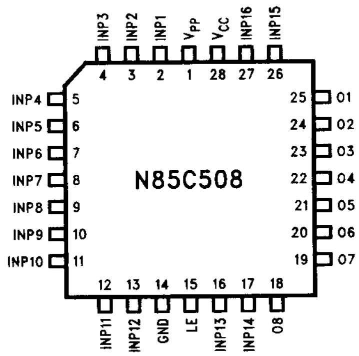

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Figure 1. Pinout Diagrams

September 1991
Order Number: 290175-005

INTRODUCTION

The 85C508 is a member of Intel's μPLD (Microcomputer Programmable Logic Device) family of devices. Produced on Intel's 1-micron CHMOS process, this device is designed to support the speeds required in fast microprocessor to memory paths. The sixteen inputs, p-term array, and eight output latches in the device provides address and data bus decoding and latching. The device takes full advantage of the lightning speed of Intel's 1-micron CHMOS technology. The device can be used as an upgrade to fast bipolar PLDs, and to fast AS, ALS, HC, or HCT SSI and MSI logic devices.

The 85C508 uses advanced EPROM cells as architecture and logic array memory elements instead of poly-silicon fuses. Coupled with Intel's proprietary CHMOS technology, the result is a device that offers a fast 7.5 ns t_{PD} in flow-through mode and a t_{EO} of 4.5 ns in latch mode. The inherent speed of the device makes it ideally suited for bus decoding applications with Intel386™, i486™, i860™, and 80960 systems. Output buffers on the device are designed to optimize signal transitions in high-speed applications (reduced overshoot and undershoot).

ARCHITECTURE DESCRIPTION

The architecture of the device is designed for high-speed performance, with dedicated inputs feeding a logic array. Outputs from the logic array feed the fast output latches. All output latches are controlled by the global LE (Latch Enable) signal. Figure 2 shows the global architecture of the 85C508.

The input to each latch is a single NAND (85C508) p-term that can be connected to the true or complement state of the dedicated inputs. All input signals are available to all eight macrocells.

Each intersecting point in the logic array is connected or not connected based on the value programmed in the EPROM array. Initially (EPROM erased state), no connections exist between any p-term and any input. Connections can be made by programming the appropriate EPROM cells. Since p-terms are implemented as NANDs. A true condition on a p-term drives the output low.

ERASURE CHARACTERISTICS

Erasure time for the 85C508 is 20 minutes at 12,000 μWsec/cm^2 with a 2537Å UV lamp.

Erasure characteristics of the device is such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000Å. It should be noted that sunlight and certain types of flourescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room level flourescent lighting could erase the typical device in approximately three years, while it would take approximately one week to erase the device when exposed to direct sunlight. If the device is to be exposed to these lighting conditions for extended periods of time, conductive opaque labels should be placed over the device window to prevent unintentional erasure.

The recommended erasure procedure for the 85C508 is exposure to shortwave ultraviolet light with a wavelength of 2537Å. The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of fifteen (15) Wsec/cm^2. The erasure time with this dosage is approximately 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during exposure. The maximum integrated dose the devices can be exposed to without damage is 7258 Wsec/cm^2 (1 week at 12,000 μW/cm^2). Exposure to high intensity UV light for longer periods may cause permanent damage to the device.

POWER-UP

Internal power-up circuits ensure that the device will respond to inputs 1000 ns (max.) after V_{CC} reaches 4.75V. V_{CC} rise must be monotonic.

LATCH-UP IMMUNITY

All of the input, output, and clock pins of the device have been designed to resist latch-up, which is inherent in inferior CMOS structures. The device is designed with Intel's proprietary 1-micron CHMOS EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from −0.5V to (V_{CC} + 0.5V). The programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. All unused inputs should be tied high or low to minimize power consumption (do not leave them floating). A power supply decoupling capacitor of at least 0.1 μF must be connected directly between each V_{CC} and GND pin. V_{PP} must be tied to GND.

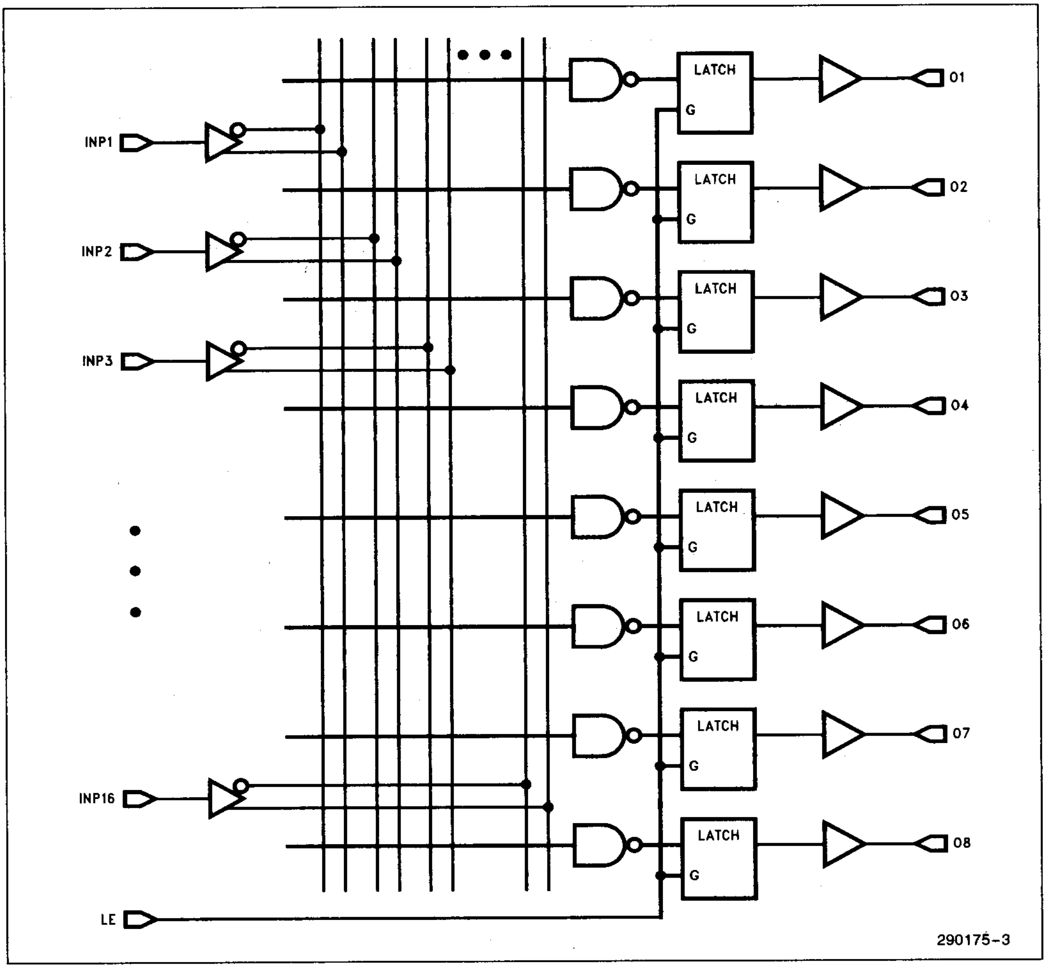

Figure 2. 85C508 Global Architecture

As with all CMOS devices, ESD handling procedures should be used with the 85C508 to prevent damage to the device during programming, assembly, and test.

FUNCTIONAL TESTING

Since the logical operation of the 85C508 is controlled by EPROM elements, the device is completely testable during the manufacturing process. Each programmable EPROM bit controlling the internal logic is tested using application independent test patterns. EPROM cells in the device are 100% tested for programming and erasure. After testing, the devices are erased before shipments to the customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology.

Fuse-based programmable logic devices require a user to perform post-programming tests to insure device functionality. During the manufacturing process, tests on fuse-based parts can only be performed in very restricted ways in order to avoid preprogramming the array.

IN-CIRCUIT CONFIGURATION CHANGE

The 85C508 allows in-circuit configuration changes after the device has powered up. At power-up, the device is configured according to the information programmed into the EPROM cells. After power-up, new information can be shifted in on select pins to alter device configuration. The new configuration is retained until the device is powered down or until the information is overwritten by another configuration change.

Note that in-circuit configuration changes allow "on-the-fly" changes to be made but do not alter EPROM cell data. At the next power-up, the device will be configured according to the original data programmed into the EPROM cells. For details on in-circuit configuration changes, refer to AP-337, *In-Circuit Reconfiguration of 85C960 and 85C508 MPLDs,* order number: 292072.

SOFTWARE SUPPORT

Full logic compilation and functional simulation for the 85C508 is supported by PLDshell Plus™ software. The GUPI 85EPLD28 provides programming support on Intel programmers.

PLDshell Plus design software is Intel's new, user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm™ logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error messsage information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the 85C508 are available. Support under iPLS II is still available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

The 85C508 is also supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

ORDERING INFORMATION

t_{PD} (ns)	t_{EO} (ns)	f_{max} (MHz)	Order Code	Package	Operating Range
7.5	4.5	133.3	N85C508-7	PLCC	Commercial
			*D85C508-7	CERDIP	
			P85C508-7	PDIP	
10	6	100	N85C508-10	PLCC	Commercial
			*D85C508-10	CERDIP	
			P85C508-10	PDIP	

*Windowed package allows UV erase.

PLDshell Plus™ is a trademark of Intel Corporation.
*ABEL is a trademark of Data I/O, Corp.
CUPL is a trademark of Logical Devices, Inc.
PLDesigner is a trademark of MINC, Inc.
Log/IC is a trademark of ISDATA, Inc.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) .... −2.0V to +7.0V

Programming Supply Voltage (V_{PP})(1) .... −2.0V to +13.5V

D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V

Storage Temperature (T_{stg}) ..... −65°C to +150°C

Ambient Temperature (T_{amb})(3) ... −10°C to +85°C

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

PACKAGE/TECHNOLOGY SPECIFICATIONS

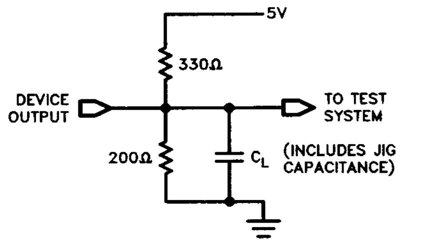
Description	Specification
θ_{JA}—Junction-to-Ambient Thermal Resistance	83°C/W—CerDIP 100°C/W—PDIP 100°C/W—PLCC
θ_{JA}—Junction-to-Case Thermal Resistance	18°C/W—CerDIP 23°C/W—PDIP 23°C/W—PLCC
I_{CC} Hot—Ambient @70°C	15 mA
I_{CC} Typical—Ambient @25°C	15 mA
Process	CHMOS IIIE, PX29.5

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}(4)	High Level Input Voltage		2.0		V_{CC} + 0.3	V
V_{IL}(4)	Low Level Input Voltage		−0.3		0.8	V
V_{OH}	High Level Output Voltage	I_O = −4.0 mA D.C., V_{CC} = min	2.4			V
V_{OL}(5)	Low Level Output Voltage	I_O = 12.0 mA D.C., V_{CC} = min			0.45	V
I_I	Input Leakage Current	V_{CC} = max., GND < V_{IN} < V_{CC}			±10	µA
I_{SC}(6)	Output Short Circuit Current	V_{CC} = max., V_{OUT} = 0.5V	−30		−120	mA
I_{SB}(7)	Standby (Quiescent) Current	V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 0 MHz			10	µA
I_{CC}	Power Supply Current	V_{CC} = max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 50 MHz, Device Prog. as 16-Bit Address Decoder		15	48	mA

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included. Do not attempt to test these values without suitable equipment.
5. Maximum DC I_{OL} for the device (all outputs) is 64 mA.
6. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.
7. Standby current is higher when true and complement p-terms for the same input are both programmed.

A.C. TESTING LOAD CIRCUIT



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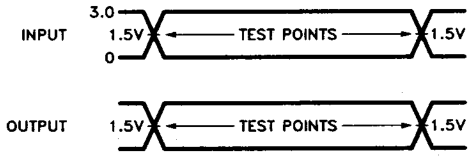
C_L = 30 pF

A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V for inputs and outputs. Device input rise and fall times are less than 3 ns.

CAPACITANCE T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz		6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz		6	10	pF
C_{CLK}	LE Capacitance	V_{IN} = 0V, f = 1.0 MHz		6	10	pF
C_{VPP}	V_{PP} Pin Capacitance	V_{PP} on Pin 1, f = 1.0 MHz		20	40	pF

A.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	85C508-7			85C508-10			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}(8)	Propagation Delay (Flow-Through Mode)	3	6	7.5	3	8	10	ns
f_{max}	Maximum Frequency ($1/t_{CW}$)		166	133.3		112	100	MHz
t_{EO}(8)	Output Valid from LE ↑	0.5	4	4.5	0.5	5	6	ns
t_{SU}	Input Setup Time to LE ↓	5.5	4		7	5		ns
t_H	Input Hold from LE ↓	−2	−3		−3	−5		ns
t_{CH}	LE High Time	4			5			ns
t_{CW}	LE ↑ to LE ↑	7.5			10			ns

NOTE:
8. One output going active; one output going inactive.

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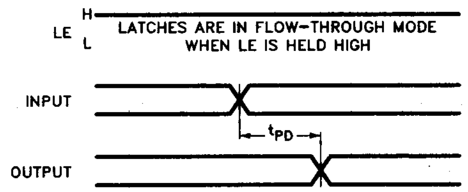
FLOW-THROUGH MODE



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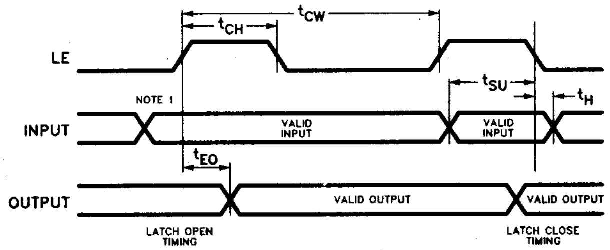
LATCH MODE



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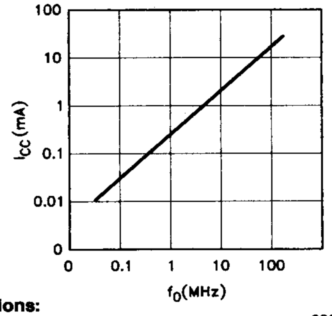
NOTE:
1. t_{EO} assumes a system setup min. of (t_{PD}−t_{EO}); e.g. 3 ns setup for a 85C508-7.

85C508 I_{CC} vs Frequency



Conditions:
$T_A = 25°C$
$V_{CC} = 5.0V$
$C_L = 30$ pF

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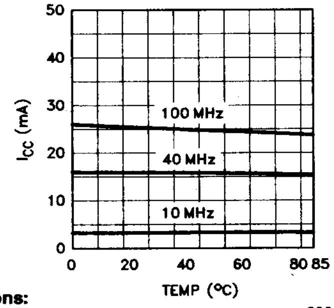
85C508 I_{CC} vs Temperature



Conditions:
$V_{CC} = 5.0V$
$C_L = 30$ pF

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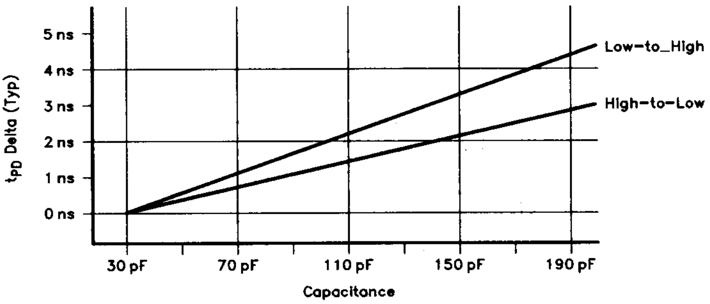
85C508 t_{PD} Derating vs Capacitive Loading



Conditions:
$T_A = 25°C$
$V_{CC} = 5.0V$

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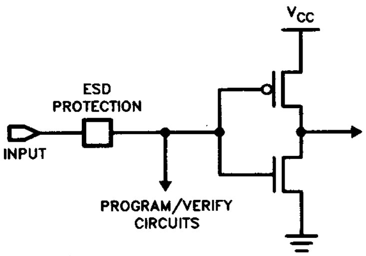
Input/Output Equivalent Schematics



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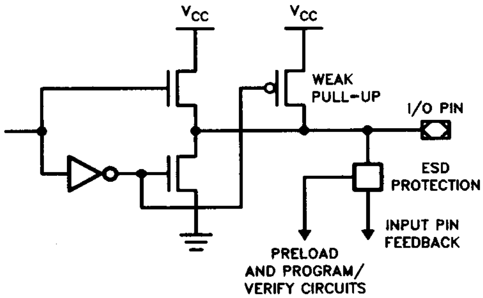

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