National Semiconductor

PRELIMINARY

LH4105/LH4105C Precision Fast Settling High Current Operational Amplifier

General Description

The LH4105 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4105 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

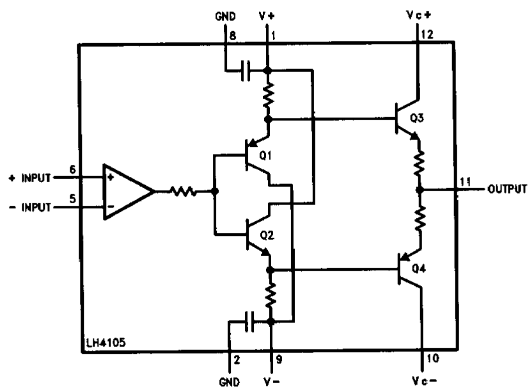
Features

- 500 μV offset voltage
- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- Internal supply bypassing
- Unity gain stable

Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

Schematic Diagram



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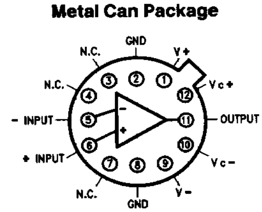
Pins #2 & #8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally, do not connect to these pins

Connection Diagram

Metal Can Package



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Top View

Note: 2 and 8 are internally connected. Case is electrically isolated. Pins 3 and 8 are used internally. Do not connect to these pins.

Order Number LH4105G or LH4105CG

See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±18V
Steady State Output Current, I_o	100 mA
Power Dissipation at, P_D	
T_A = 25°C, derate linearly at 100°C/W	2.5W
T_C = 25°C, derate linearly at 50°C/W	1.5W
Differential Input Voltage, V_{IN}	±30V but ≤ ±2V_s
Input Voltage Range, V_{CM}	±18V but ≤ ±V_s
Operating Temperature Range, T_A	
LH4105	−55°C to +125°C
LH4105C	−25°C to +85°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering < 10 sec.)	300°C

ESD rating is to be determined.

DC Electrical Characteristics V_S = ±15V, T_A = 25°C unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4105C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	R_S = 50Ω	0.2	0.5	**2**	mV
$V_{OS}/\Delta T$	Offset Voltage Drift	R_S = 50Ω	20			μV/°C
I_B	Input Bias Current	T_j = 25°C, (Note 4) V_{CM} = 0V	200	600		pA
					250	nA
I_{OS}	Input Offset Current	T_j = 25°C, V_{CM} = 0V	20	400		pA
					200	nA
R_{IN}	Input Resistance	T_j = 25°C	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 100Ω	106	87		dB (Min)
		R_L = 1 kΩ	106	87	**80**	
V_O	Output Voltage Swing	R_L = 100Ω (Note 5)		±10		V (Min)
		R_L = 1 kΩ	±13	±10	**±10**	
V_{CM}	Input Common Mode Range		±12	±11	**±10**	V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} = −11V to +11V	100	80	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	V_{CC} = ±10V to ±15V	100	80	**70**	dB (Min)
I_S	Supply Current		20	25		mA

AC Electrical Characteristics V_S = ±15V, T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	LH4105C			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	A_V = −1, V_{IN} = −5V to +5V, R_L = 100Ω	500	800		ns
S_R	Slew Rate	V_{IN} = −10V to +10V, R_L = 100Ω	40		32	V/μs(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	A_V = 1, R_L = 100Ω	10		20	ns

DC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted (Notes 1 and 6)

Symbol	Parameter	Conditions	LH4105			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	0.2	**2**		mV
$V_{OS}/\Delta T$	Offset Voltage Drift	$R_S = 50\Omega$	20			$\mu V/°C$
I_B	Input Bias Current	$T_j = 25°C$, (Note 4) $V_{CM} = 0V$	200	600		pA
				350		nA
I_{OS}	Input Offset Current	$T_j = 25°C$, $V_{CM} = 0V$	20	400		pA
				250		nA
R_{IN}	Input Resistance	$T_j = 25°C$	10^{11}			Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$	106	87		dB (Min)
		$R_L = 1\ k\Omega$	106	87		
				80		
V_O	Output Voltage Swing	$R_L = 100\Omega$ (Note 5)		± 10		V (Min)
		$R_L = 1\ k\Omega$	± 13	**±10**		
V_{CM}	Input Common Mode Range		± 12	**±10**		V (Min)
CMRR	Common Mode Rejection Ratio	V_{IN} −11V to +11V	100	80		dB (Min)
				70		
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10V$ to $\pm 15V$	100	80		dB (Min)
				70		
I_S	Supply Current		20	25		mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions	LH4105			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	$A_V = -1$, $V_{IN} = -5V$ to $+5V$, $R_L = 100\Omega$	500	800		ns
S_R	Slew Rate	$V_{IN} = -10V$ to $+10V$, $R_L = 100\Omega$	40		32	$V/\mu s$(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	$A_V = 1$, $R_L = 100\Omega$	10		20	ns

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4105C is −25°C to +85°C, and LH4105 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not production tested). These limits are not used to calculate outgoing quality levels.

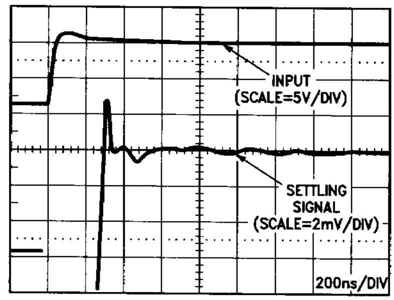
Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at $T_j = 25°C$.

Note 5: The output swing is limited by the maximum output current of ±100 mA when $R_L = 100\Omega$.

Note 6: When the LH4105 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_{CC} of ±15V is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

Typical Performance Characteristics

Settling Signal



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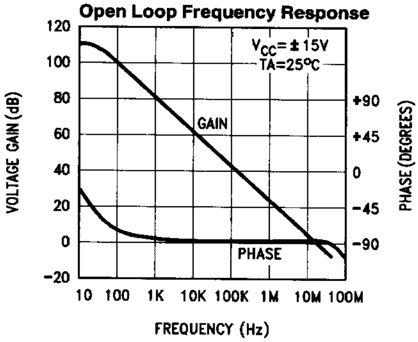
Open Loop Frequency Response



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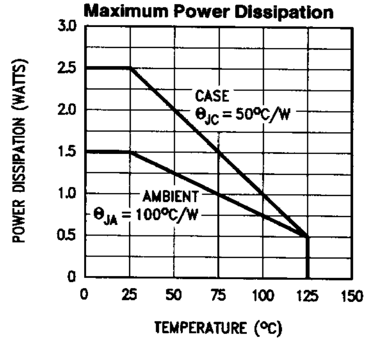
Maximum Power Dissipation



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Applications Information

POWER SUPPLY BYPASSING

The LH4105 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 μF disc ceramic capacitor and 1 μF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

COMPENSATION

To minimize the effects of input capacitance at the LH4105's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias (I_B) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. I_B will normally double with each 11°C rise in junction temperature.

LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4105. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4105, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4105. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4105 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4105 without impacting settling time. In addition, bypassing offset adjust pins 3 and 7 with 0.1 μF capacitors will minimize noise pickup and preserve the settling time.

PROTECTION SCHEMES FOR THE LH4104

The LH4105 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4105's input stage shares its topology with the LF400.)

NEVER LEAVE AN INPUT UNATTENDED

If an input to the LH4105 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance (<10 pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4105 is capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

To avoid this condition in circuits where the LH4105 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor appears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can damage the device. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.

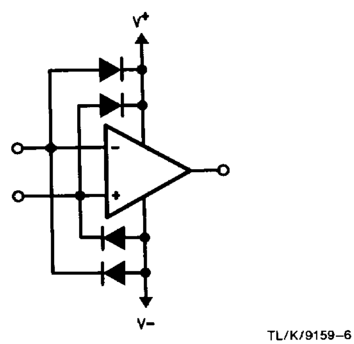

FIGURE 1. Clamping Inputs of Op Amp

Test Circuit for Pulse Response

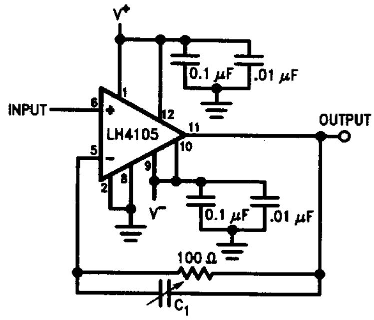

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FIGURE 2

Typical Applications

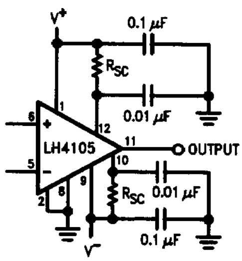

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FIGURE 3. Using Resistor Current Limiting

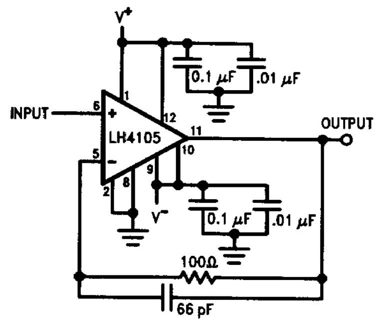

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FIGURE 4. Unity Gain Follower

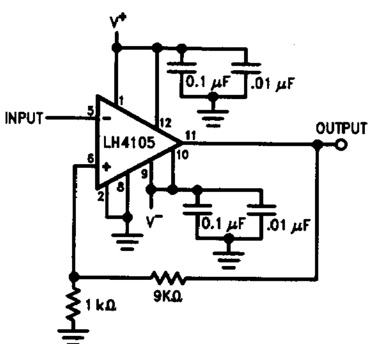

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FIGURE 5. 10X Buffer Amplifier

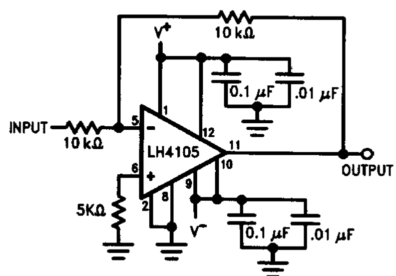

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FIGURE 6. Unity Gain Inverter

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