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LH5003/LH5004

LCD Character Display **Driver LSI**

Description

The LH5003/LH5004 is an LCD character display driver CMOS LSI which provides 128 kinds of alphanumeric and symbolic character display function.

The LH5003 is a master driver used to control and drive a 30-segment and an 8-common, and the LH5004 is a slave driver used to driver a 40-

They can be applied to dot matrix LCD systems with a minimal external parts count, controlled by a 4-bit or an 8-bit microcomputer.

Features

- 1. CMOS process
- 2. 5 × 7 dot-matrix LCD controller/driver
- 3. Display data RAM

240 bits (LH5003) 320 bits (LH5004)

- 4. Character Generator 128 patterns
- 5. Driving system

Duty: 1/8 duty

Bias: Controlled by an external resistor

6. Character configuration is 5×7 dots plus cursor

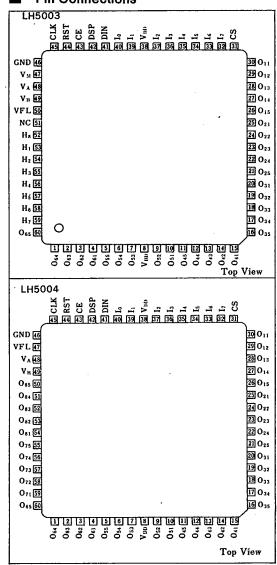
> LH5003 (Master) 6 digits LH5004 (Slave) 8 digits

7. LCD drive circuit

LH5003: Common signal 8 bits Segment signal 30 bits

- LH5004: Segment signal 40 bits 8. Single power supply: -5V (TYP)
- 9. 60-pin quad-flat package

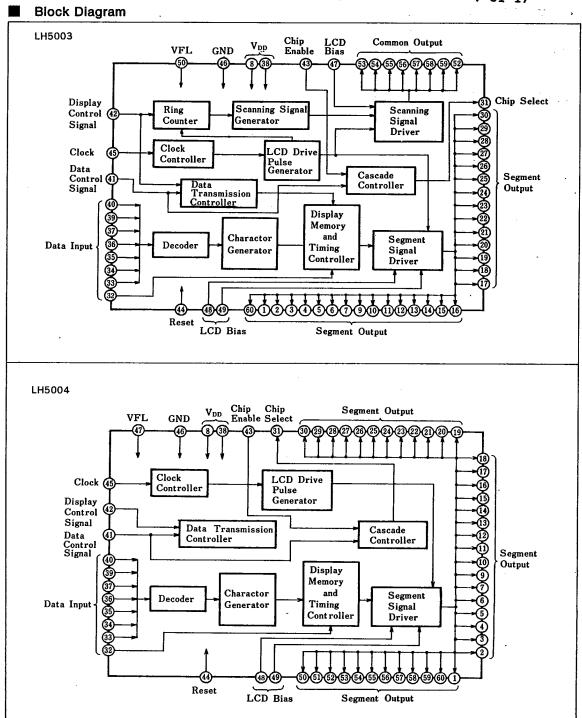
Pin Connections



SHARP

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	
	V_{DD}	-0.3 to $+8.0$	V	
Pin voltage	V _{IN}	-0.3 to $V_{DD} + 0.3$	V	
Operating temperature	Topr	-10 to +60	С	
Storage temperature	T _{stg}	-55 to +150	ဗ	

Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	- 4.2 to 6.3	V
Oscillator frequency	f _{CLK}	32 to 320	kHz

Electrical Characteristics

$(V_{DD} = 5V, GND = 0V, Ta = -10 \text{ to } +60\%$	$(V_{DD}=5V_{c})$	GND = 0V.	$T_a = -10 \text{ to}$	+60℃
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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
	V _{IL}				1		1
	V _{IH}		4				1
Input voltage	V _M			2.5		V	2
	VA		3.5	5 4 5	5		3
•			0	1	1.5	•	4
•	IIL	$V_{IN}=0V$			1	4	1
Input current	I _{IH}	$V_{IN}=5V$			1	μΑ	
, Output voltage	V _{OL1}	N 1 - 1		V_{B}	$V_B + 0.2$		5
	V _{OH1}	No-load condition	$V_A - 0.2$	VA			
	$V_{\rm OL2}$	$ I_{OL} = 50 \ \mu A$			0.8	v	6
	V _{OH2}	$I_{OH} = 50 \mu A$	4.2				L
	V _{OL3}			0	0.2		
	V _{om}	No-load condition	$V_{M}-0.2$	V _M	$V_{M} + 0.2$		7
	V _{OH3}		4,8	5			
Current consumption	I _{D1}	f _{CLK} =32kHz		28	50	μΑ	8
	I _{D2}	f _{CLK} =64kHz		60	100		
	I_{D3}	f _{CLK} =320kHz		220	400		

Note 1: Applied to pins
Note 2: Applied to pin
Note 3: Applied to pin
Note 4: Applied to pin
Note 4: Applied to pin
Note 4: Applied to pin
Note 6: Applied to pin
Note 6: Applied to pin
Note 6: Applied to pin
Note 7: Applied to pin
Note 8: Applied to pin
Note 9: Applied to pi

Note 4. Applied to pins V_B Note 5: Applied to pins O_{11} - O_{85} Note 6: Applied to pin CSNote 7: Applied to pins H_1 - H_8 Note 8: Output pin is opened and input pin set to GND level.

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Functions

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Pin description

Pin name	No. of pins	I/O	Connect to	Functions
V _{DD} , GND	3			Power supply for logic circuit
		•		Power supply $V_M = V_{DD}/2$
V_A , V_B , V_M	3		Power supply	for liquid $V_A = V_M + \Delta V$
				crystal drive $V_B = V_M - \Delta V (\Delta V = 1.0 \text{ to } V_M)$
	8			Character code input (I ₀ -I ₆) from MPU
I ₀ -I ₇	°			Cursor display data input (I ₇)
DIN	,			High: character data read
DIN	· 1	I		one character shift in display memory
•				"High": Display mode
DSP	1		MPU	"Low": Blank mode
				(reset of cascade control data
				transfer control circuit)
CLK	1			Clock pulse input
				"High" : Operation start signal
RST	1			(reset of cascade controller, cascade control
		•		data transfer control circuit, ring counter, etc.)
CE	1		Power	Chin anabla nin
CE	1		supply (CS)*	Chip enable pin
CS	1		CE	Chip select pin
				LCD frame frequency swithcing signal
VFL	1	0	MPU	"High: 1/1024 of clock frequency
				"Low": 1/512 of clock frequency
H ₁ -H ₈	8(0)*		Liquid crystal	LCD common signal drive signal
011-086	30(40)*		Liquid Crystai	LCD segment signal drive signal



- CLK signal The clock signal is a clock pulse used to operate LH5003 and LH5004 and is continually applied while the power is on. For the CLK signal, apply the clock pulse made in the microcomputer system or a pulse made by dividing this clock pulse and in sync with the microcomputer system.
- DIN signal The DIN signal is used to set the data in the display memories of LH5003 and LH5004. Each time the DIN signal rises, it reads display data corresponding to the character code applied to pins I_0 through I_7 into the display memory and shifts the existing contents of the display memory one character. Set the pulse width of the DIN signal to at least two cycles of the clock pulse (a pulse width of $2T_{CK}$ or greater when the clock pulse period is T_{CK} .)
- DSP signal The DSP signal determines the display condition. When it is high, the display mode is set and when it is low, the blank mode is set and the cascade controller and data transfer control circuit are reset. Normally, the DSP signal is made high after setting the data in the display memories of the LH5003 and LH5004.

- RST signal The RST signal is used to initialize the internal control circuits of the LH5003 and LH5004 by applying the pulse of the RST signal to this pin immediately after the power is turned on. Synchronize the fall of the RST pulse with the rise of the clock pulse, and set the pulse width of the RST pulse to at least four times that of the normal clock pulse width ($4T_{CK}$.)
- I_0 - I_7 signal The I_0 - I_7 signal is an 8-bit parallel signal that determines the characters and symbols to be displayed. Select the desired characters using the data of pins I_0 - I_6 (see the table relating input codes with displayed characters and symbols). When the I_7 signal is high, the cursor is displayed, and when it is low, the cursor is displayed, and when it is low, the cursor is blanked out. LH5003 and LH5004 are controlled from the microcomputer system by the following procedure.
- The clock pulse is applied continually to the CLK pin during the period from immediately after the power is turned on until it is turned off.
- (2) Immediately after the power is turned on, the RST pulse is applied to the RST pin.



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- The DSP and DIN pins are made low. (Not necessary if they are already low.)
- (4) The character code of the character to be displayed is output to pins I₀-I₇.
- (5) The DIN pin becomes high level and then low level again. (Apply one pulse to the DIN pin.)
- (6) Steps 4 and 5 are repeated for each display position.
- (7) The DSP pin is made high level. (This condition sets the display mode.)
- (8) The contents of the display are changed by repeating steps 3 through 7.

Input Codes and Displayed Characters and Symbols

(LH5003/LH5004)

Data Data I ₅ ~ I ₄ I ₃ ~ I ₆	0	1	2	3	4	5	6	7
0								
1								
2								
3								
4								
5								
6								
7								
8								
9								
A		Ž						
В								
С								
D								
E								
F	垄							

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System Configuration Example

