T-52-33-03

LH5040/LH5041 CMOS I/O Expander LSI

■ Description

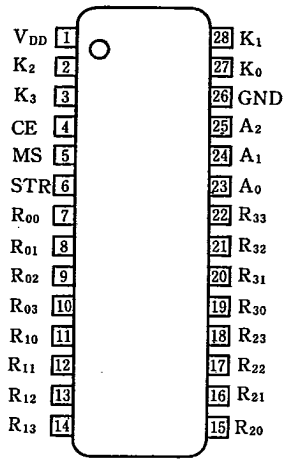
The LH5040/LH5041 are CMOS I/O expander LSIs designed to expand 4-bit input/output of a 1-chip microcomputer to 4-bit×4 (LH5040) or 4-bit×7 (LH5041) configuration.

■ Features

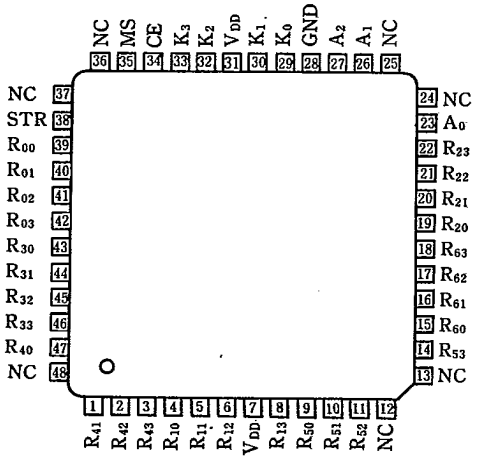
1. Output latch mode or input multiplexer mode selectable.
2. Multi-connections are possible by CE control and STR control.
3. Applicable to 3V system or 5V system power supply.
4. Number of expansion pins: 16 (LH5040) 28 (LH5041).
5. Low power consumption.
6. 28-pin dual-in-line package (LH5040)
   48-pin quad-flat package (LH5041)

■ Pin Connections

LH5040



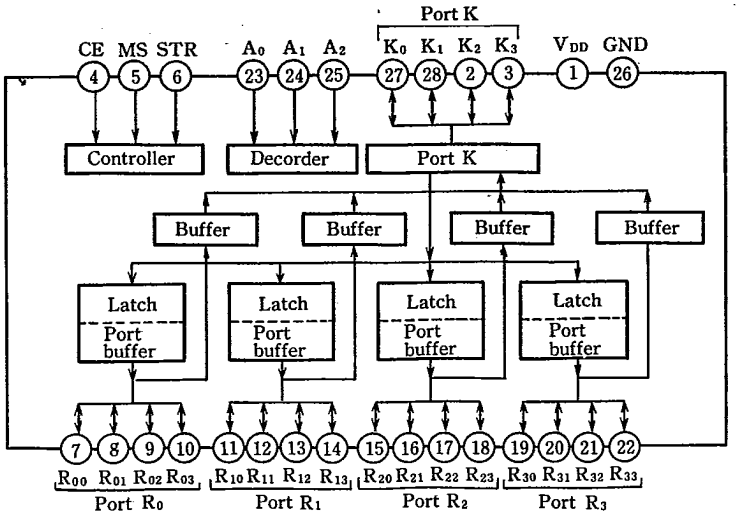
LH5041



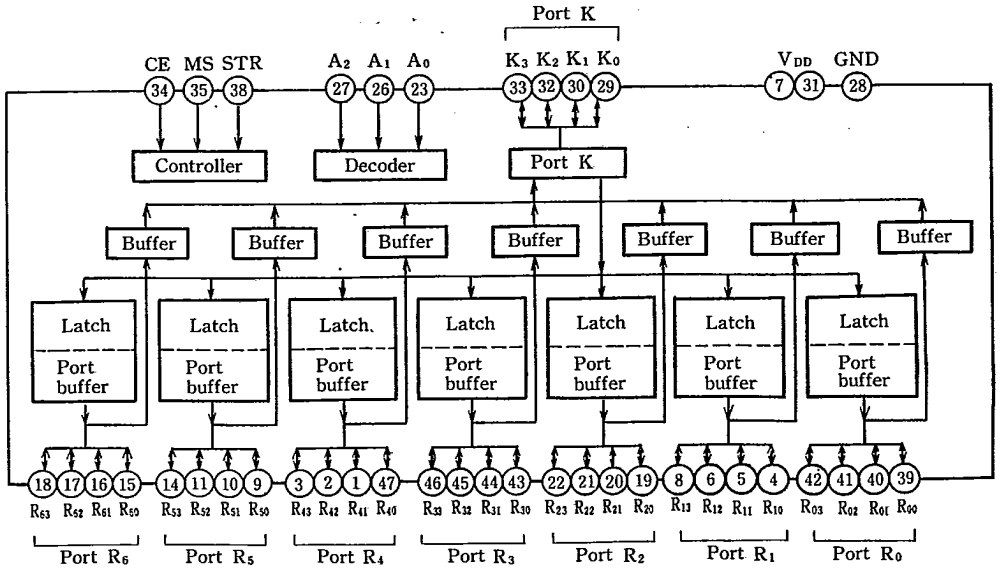
Top View

Block Diagrams

LH5040



LH5041



Pin Description

Symbol	Pin name	Function
MS	Mode select input	This input becomes latch mode with "High" and becomes multiplexer mode with "Low".
STR	Strobe input	This input becomes valid in latch mode. When a pulse is applied, the data of input port K is latched and output to the output R at falling.
CE	Chip enable input	This input becomes valid in multiplexer mode. When the CE pin is active, K pin becomes active. When this pin is inactive, it becomes high impedance.
K_0-K_3	Input/Output K	The K_0 to K_3 pins are 4-bit bi-directional input/output. They become inputs in latch mode and become outputs in multiplexer mode.
R	Input/Output R	LH5040: (R_{00}-R_{03})-(R_{30}-R_{33}) LH5041: (R_{00}-R_{03})-(R_{60}-R_{63}) The R pins are 4-bit bi-directional input/output. They become outputs in latch mode and become inputs in multiplexer mode.
A_0-A_2	Select input	In latch mode, one set of output is selected. In multiplexer mode, one set of input is selected. In the case where A_0 through A_2 are of "Low", it becomes reset mode. In multiplexer mode. K output becomes high impedance. When a pulse is applied to STR in latch mode, "Low" is written into every latch of R output regardless of the content of K input.

LH5040

Pin select input			Pins to be selected
A_2	A_1	A_0	
H	L	L	R_{00}-R_{03}
H	L	H	R_{10}-R_{13}
H	H	L	R_{20}-R_{23}
H	H	H	R_{30}-R_{33}

V_{DD}: H, GND: L

LH5041

Pin select input			Pins to be selected
A_2	A_1	A_0	
L	L	H	R_{00}-R_{03}
L	H	L	R_{10}-R_{13}
L	H	H	R_{20}-R_{23}
H	L	L	R_{30}-R_{33}
H	L	H	R_{40}-R_{43}
H	H	L	R_{50}-R_{53}
H	H	H	R_{60}-R_{63}

■ Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	Referenced to GND	−0.3 to +70	V
Input voltage	V_{IN}	Referenced to GND	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Referenced to GND	−0.3 to V_{DD}+0.3	V
Power dissipation	P_D	Ta=25℃	250	mW
Operating temperature	T_{opr}		−10 to +70	℃
Storage temperature	T_{stg}		−55 to +150	℃

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	Reference to GND	2.5	5.0	5.5	V
Input voltage	V_{IN}	Reference to GND	0		V_{DD}	V

■ DC Characteristics

(Unless otherwise specified: V_{DD}=5.0V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage 1	V_{IH}	V_{DD}<3.0V	V_{DD}−0.4		V_{DD}	V
	V_{IL}		0		0.4	
Input voltage 2	V_{IH}	V_{DD}≧3.0V	0.7 V_{DD}		V_{DD}	V
	V_{IL}		0		0.3V_{DD}	
Input current 1 (R pin)	I_{IH}	V_{IH}=5.0V			10	μA
	$-I_{IL}$	V_{IL}=0V			10	
Input current 2 (except R pin)	I_{IH}	V_{IH}=5.0V			1	μA
	$-I_{IL}$	V_{IL}=0V			1	
Output voltage 1 (K pin)	V_{OH}	V_{DD}=3.0V, I_{OH}=−50μA	2.7			V
		V_{DD}=5.0V, I_{OH}=−200μA	4.6			
	V_{OL}	V_{DD}=3.0V, I_{OL}=50μA			0.2	
		V_{DD}=5.0V, I_{OL}=250μA			0.4	
Output voltage 2 (R pin)	V_{OH}	V_{DD}=3.0V, I_{OH}=−0.5mA	2.0			V
		V_{DD}=5.0V, I_{OH}=−2.0mA	2.5			
	V_{OL1}	V_{DD}=3.0V, I_{OL}=0.25mA			0.2	
		V_{DD}=5.0V, I_{OL}=1.0mA			0.4	
	V_{OL2}	V_{DD}=3.0V, I_{OL}=1.0mA			1.0	
		V_{DD}=5.0V, I_{OL}=4.0mA			1.8	
Current consumption	I_{DD}	Output pin open			30	μA

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■ AC Characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data setup time to STR input K-STR	t_{SU1}	V_{DD}=3.0V		0.2			μs
		V_{DD}=5.0V		0.2			
Data setup time to STR input select A-STR	t_{SU2}	V_{DD}=3.0V		1.0			μs
		V_{DD}=5.0V		1.0			
Data hold time to STR input K-STR	t_{H1}	V_{DD}=3.0V		0.4			μs
		V_{DD}=5.0V		0.4			
Data hold time to STR input select A-STR	t_{H2}	V_{DD}=3.0V		1.0			μs
		V_{DD}=5.0V		1.0			
STR input pulse width	t_W	V_{DD}=3.0V		0.5			μs
		V_{DD}=5.0V		0.5			
Effective output delay time CE-K	t_{PZX1}	R_L=10kΩ C_L=50pF (Note)	V_{DD}=3.0V			1.2	μs
			V_{DD}=5.0V			0.6	
Effective output delay time MS-R	t_{PZX2}		V_{DD}=3.0V			1.4	μs
			V_{DD}=5.0V			0.8	
Output floating delay time CE-K	t_{PXZ1}		V_{DD}=3.0V			1.2	μs
			V_{DD}=5.0V			0.6	
Output floating delay time MS-R	t_{PXZ2}		V_{DD}=3.0V			1.4	μs
			V_{DD}=5.0V			0.8	
Data output "High" delay time select A-K	t_{PLH1}	R_L=200kΩ C_L=50pF (Note)	V_{DD}=3.0V			3.0	μs
			V_{DD}=5.0V			3.0	
Data output "High" delay time R-K	t_{PLH2}		V_{DD}=3.0V			1.8	μs
			V_{DD}=5.0V			1.8	
Data output "High" delay time STR-R	t_{PLH3}		V_{DD}=3.0V			1.2	μs
			V_{DD}=5.0V			1.2	
Data output "Low" delay time Select A-K	t_{PHL1}		V_{DD}=3.0V			3.0	μs
			V_{DD}=5.0V			3.0	
Data output "Low" delay time R-K	t_{PHL2}		V_{DD}=3.0V			1.8	μs
			V_{DD}=5.0V			1.8	
Data output "Low" delay time STR-R	t_{PHL3}		V_{DD}=3.0V			1.2	μs
			V_{DD}=5.0V			1.2	

Note : C_L is connected to GND.

■ Functional Description

(1) Typical Timing

In latch mode, a pulse is applied to STR after select inputs A_0 through A_2 and K input have been set as shown in Fig. 1.

When operating on 5V, STR is turned to "High" more than 1.0 μs after A_0 through A_2 have been set or more than 0.2 μs after K pin has been set.

Pulse width of STR should be taken for more than 0.5 μs. After STR has been put into "Low", hold the data for more than 1.0 μs for A_0-A_2 and more than 0.4 μs for K pin.

Unless the foregoing conditions are met, the data may not be latched correctly.

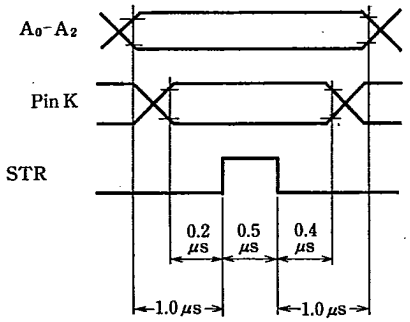


Fig. 1

(2) Switching characteristics

As for switching characteristics, the R output varies at STR falling as shown in Fig. 2, and its delay time is less 1.2 μs.

In multiplexer mode, delay time of K output while select inputs A_0-A_2 are changed is less than 3.0 μs as shown in Fig. 3.

Delay time of K output while R input is changed is less than 1.8 μs as shown in Fig. 4.

The foregoing explanation is intended for use in 5V. As for other switching characteristics or when operating on 3V, see AC characteristics shown separately.

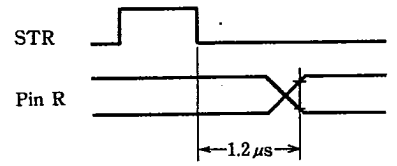


Fig. 2

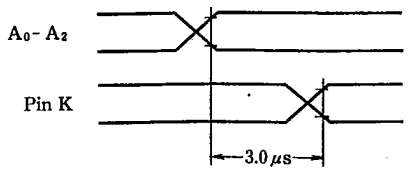


Fig. 3

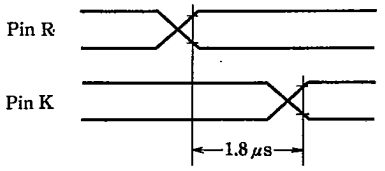
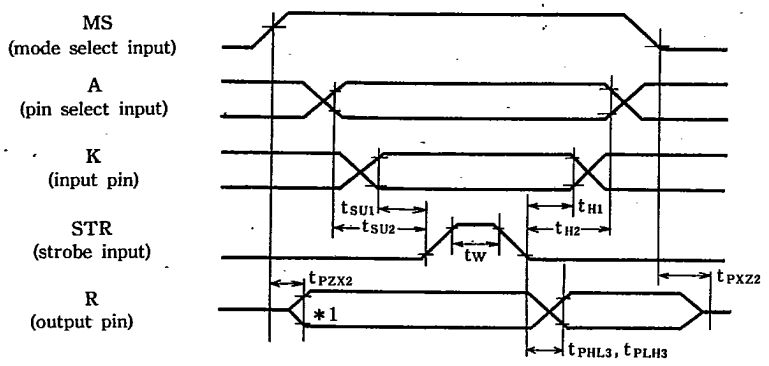


Fig. 4

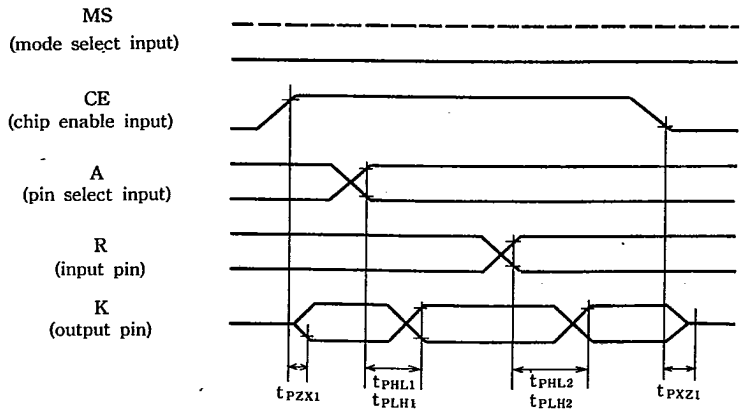
■ Timing Diagram

(1) Latch mode



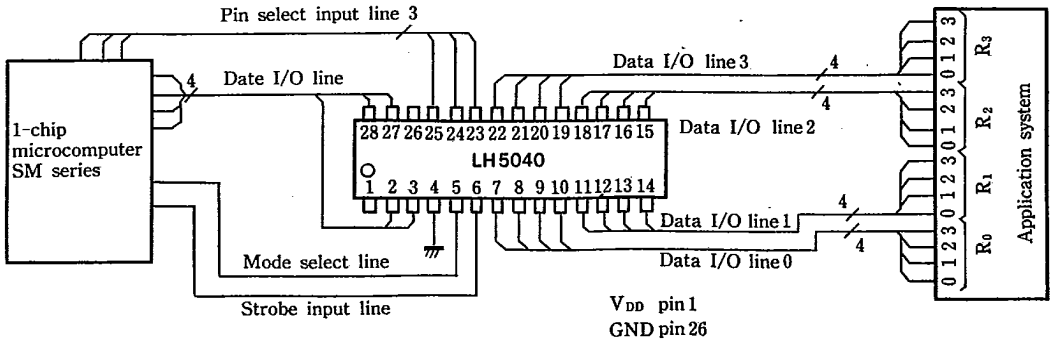
*1 The output (R) immediately after mode switching is invalid irrespective of the input (K) until STR signal is input.

(2) Multiplexer mode



■ Application Circuit Example

(1) LH5040



(2) LH5041